Reliable Electronic Devices, Circuits, and Systems

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innovations
for high
performance
microelectronics

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ELICSIR Online Summer School

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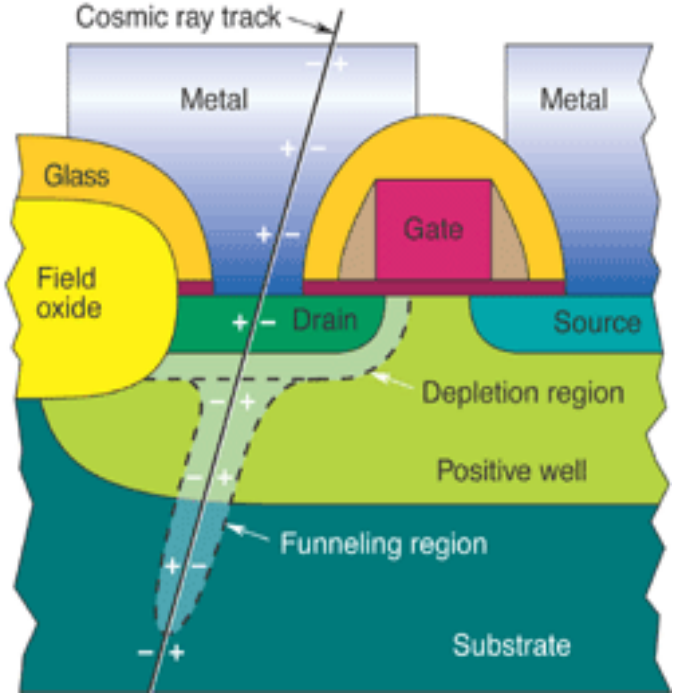
Agenda

1. Radiation Effects
2. Radiation-Hard Devices
3. Fault-Tolerant Circuits and Systems
4. SET Modeling and Characterization
5. Middleware Switch Processor

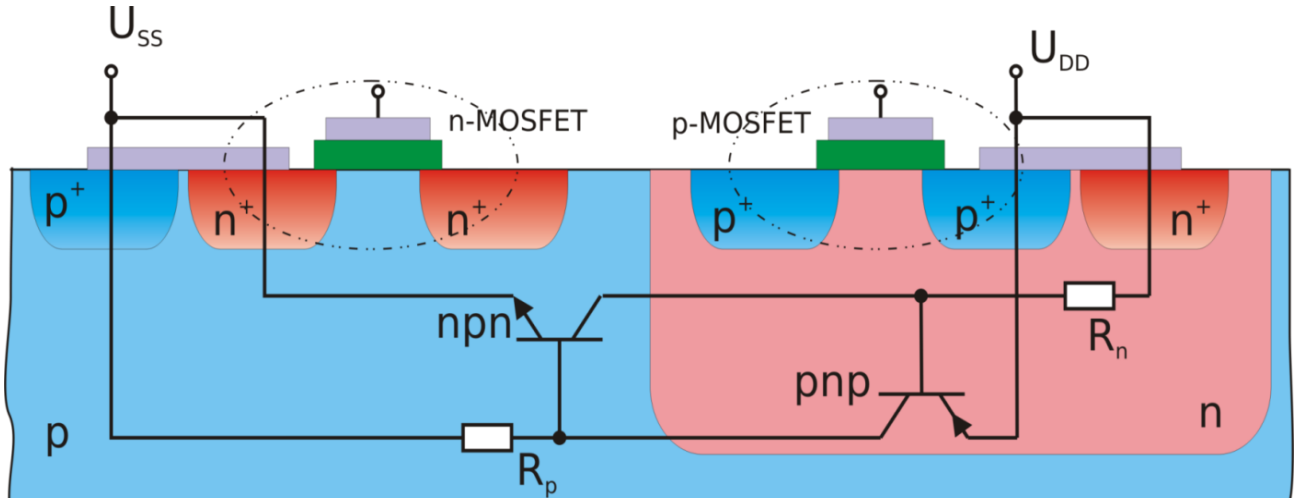
Radiation Effects in Semiconductor Devices

- Natural space radiation (high-energy ionizing particles) may induce electrical noise (single event effect) in many types of semiconductor devices
  - Data corruption, transient disturbance, and high-current conditions
- Each particle produces an ionization track (and electrical charge)
  - Prompt component
    - Funneling in high-field regions
  - Delayed component
    - Diffusion in low-field regions
- Non-destructive effects
  - Single event upset (SEU)
  - Single event transient (SET)
- Destructive effect in CMOS technology
  - Single event latchup (SEL)



Radiation Effects in Integrated Circuits

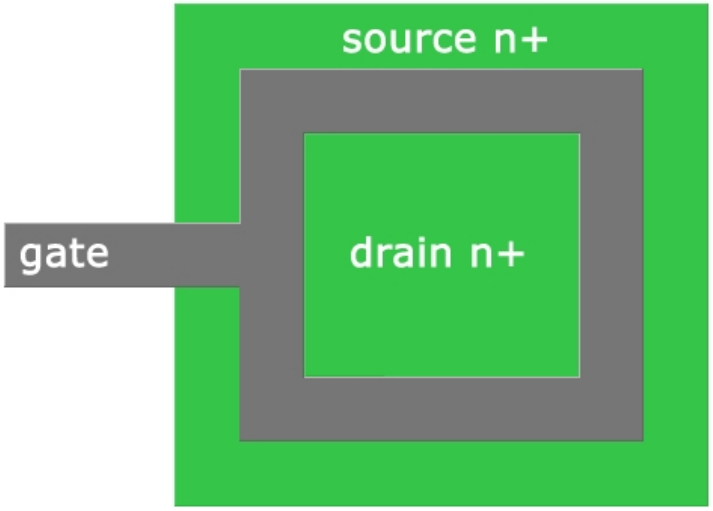
- SEU causes the change of state in storage element
  - Memory cells and registers affected
- SET causes a high-voltage impulse on interconnection lines
  - Combinational logic affected
- SEL causes an excessive current flow through the parasitic PNPN structure in CMOS transistor pair
  - Circuit design and technology dependent



Solutions for Fault-Tolerant Circuits and Systems

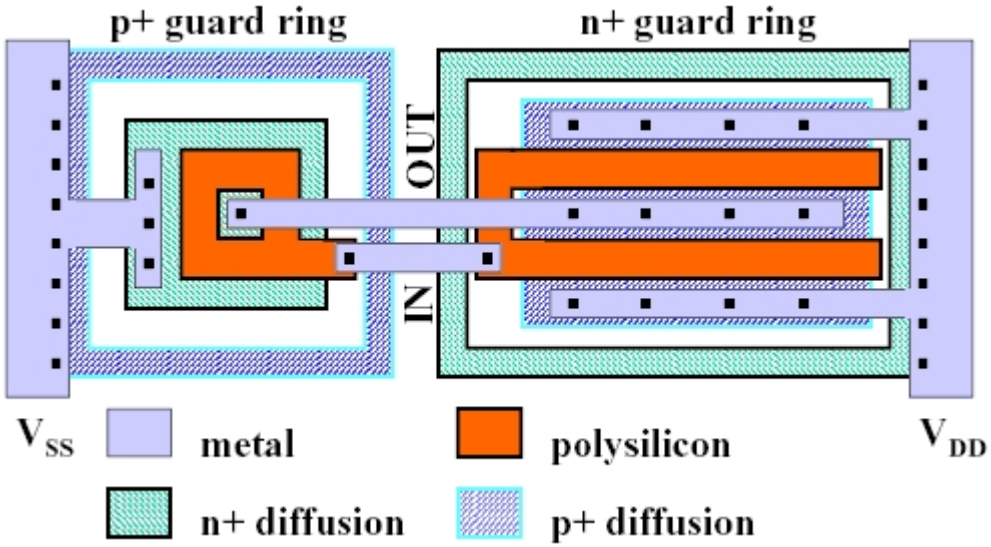
- Single event effect (fault) tolerant application specific integrated circuits
  - Device techniques
  - Circuit techniques
  - System techniques
- Circuit and design techniques are not as expensive as device techniques
  - SEU and SET tolerance
    - Triple modular redundancy (TMR)
    - Double modular redundancy (DMR)
  - SEL tolerance
    - Current sensing and power switching
  - SEU, SET, and SEL tolerance
    - Modification of net-list, placement, and routing

Enclosed Layout Transistors



Radiation tolerant MOS transistor designed according to the enclosed layout transistor topology

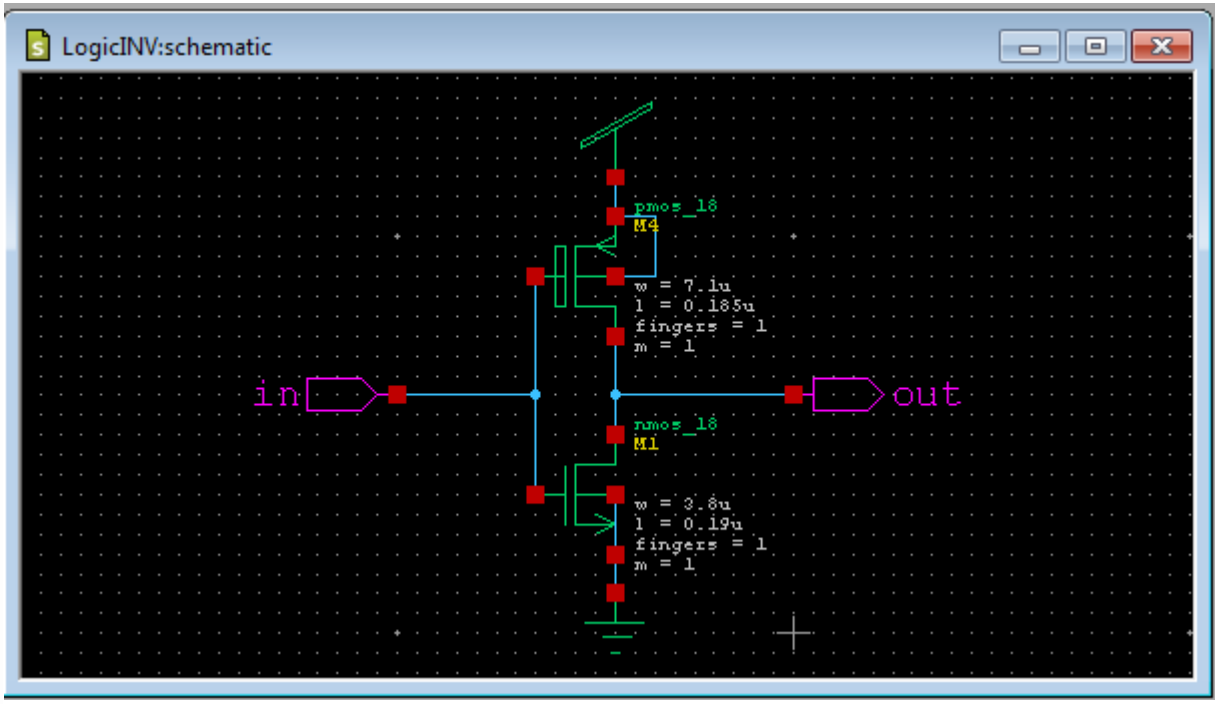
Enclosed layout transistors and guard rings in a radiation tolerant CMOS inverter

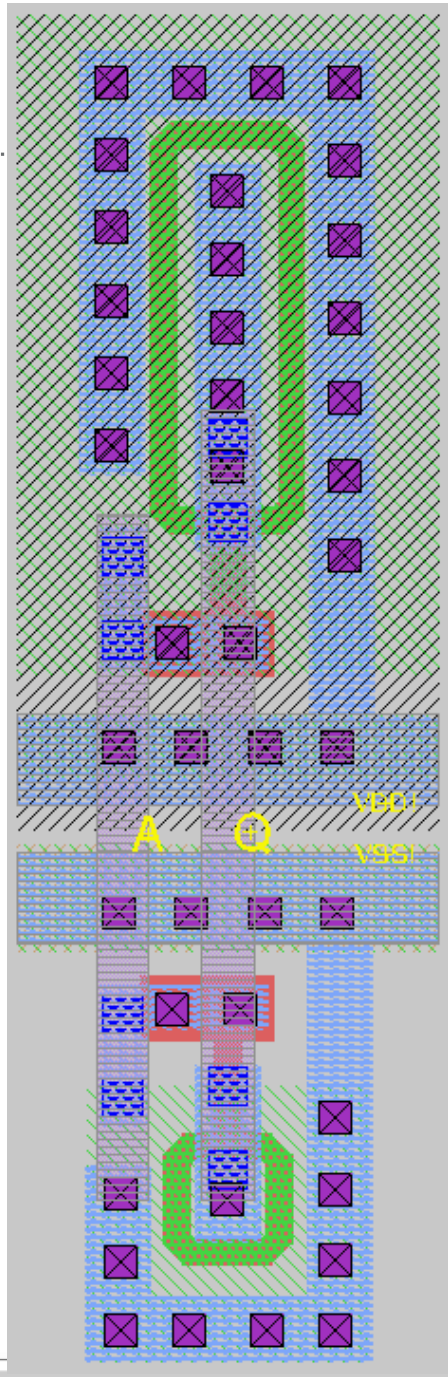


Rad-Hard Standard Cells

ELT n-mos and p-mos transistor to increase Total Ionizing Dose (TID)

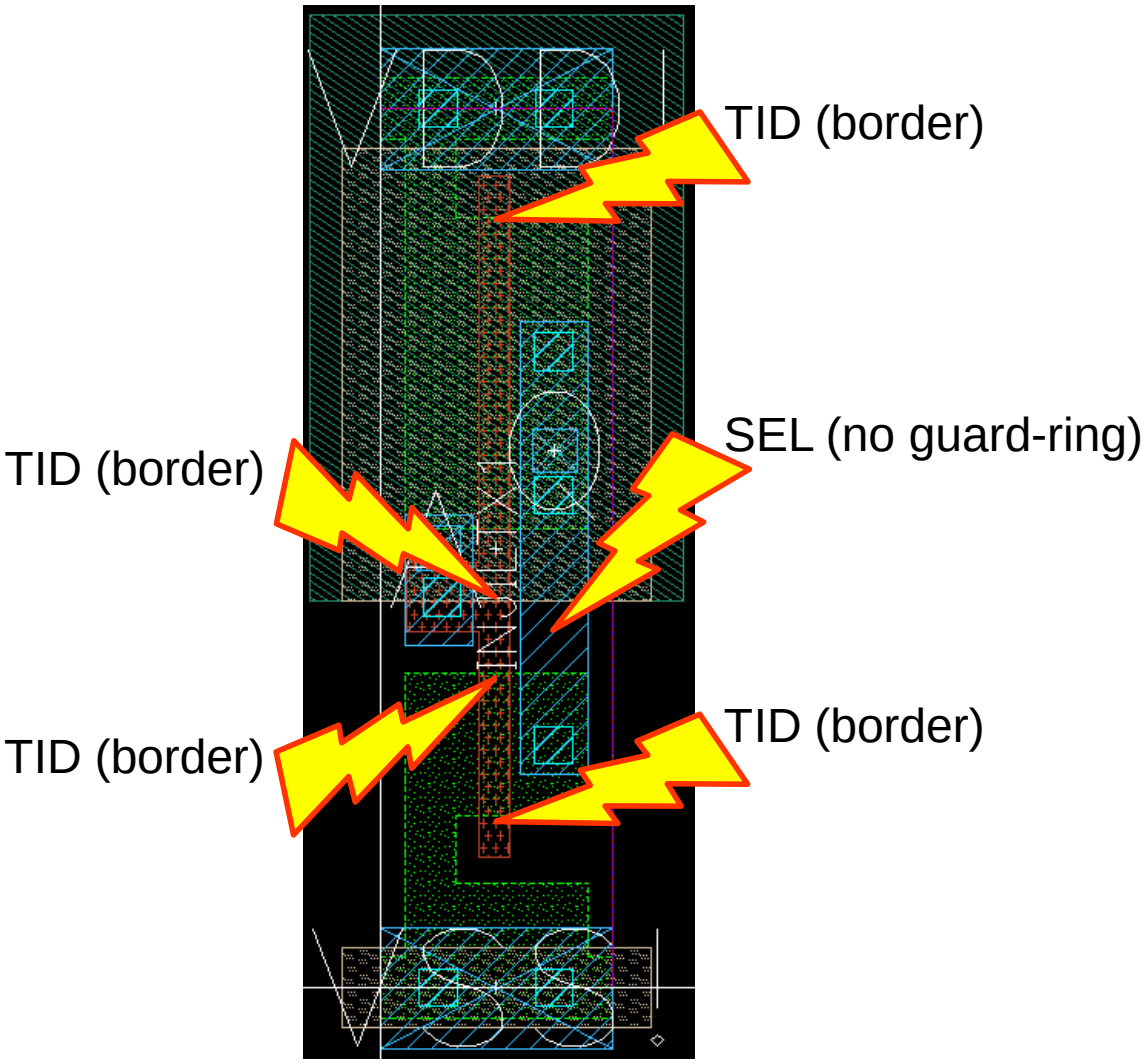
Enhanced guard-rings against Single-Event-Latchup (SEL)

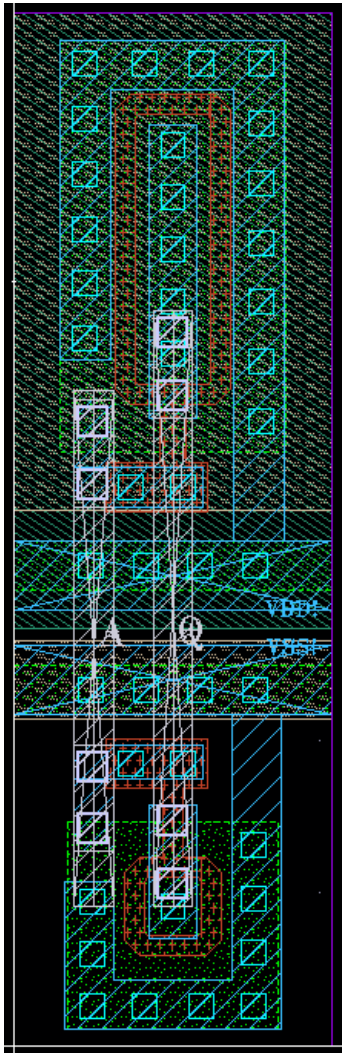




Courtesy of Cristiano Calligaro

Original and Rad-Hard Cells





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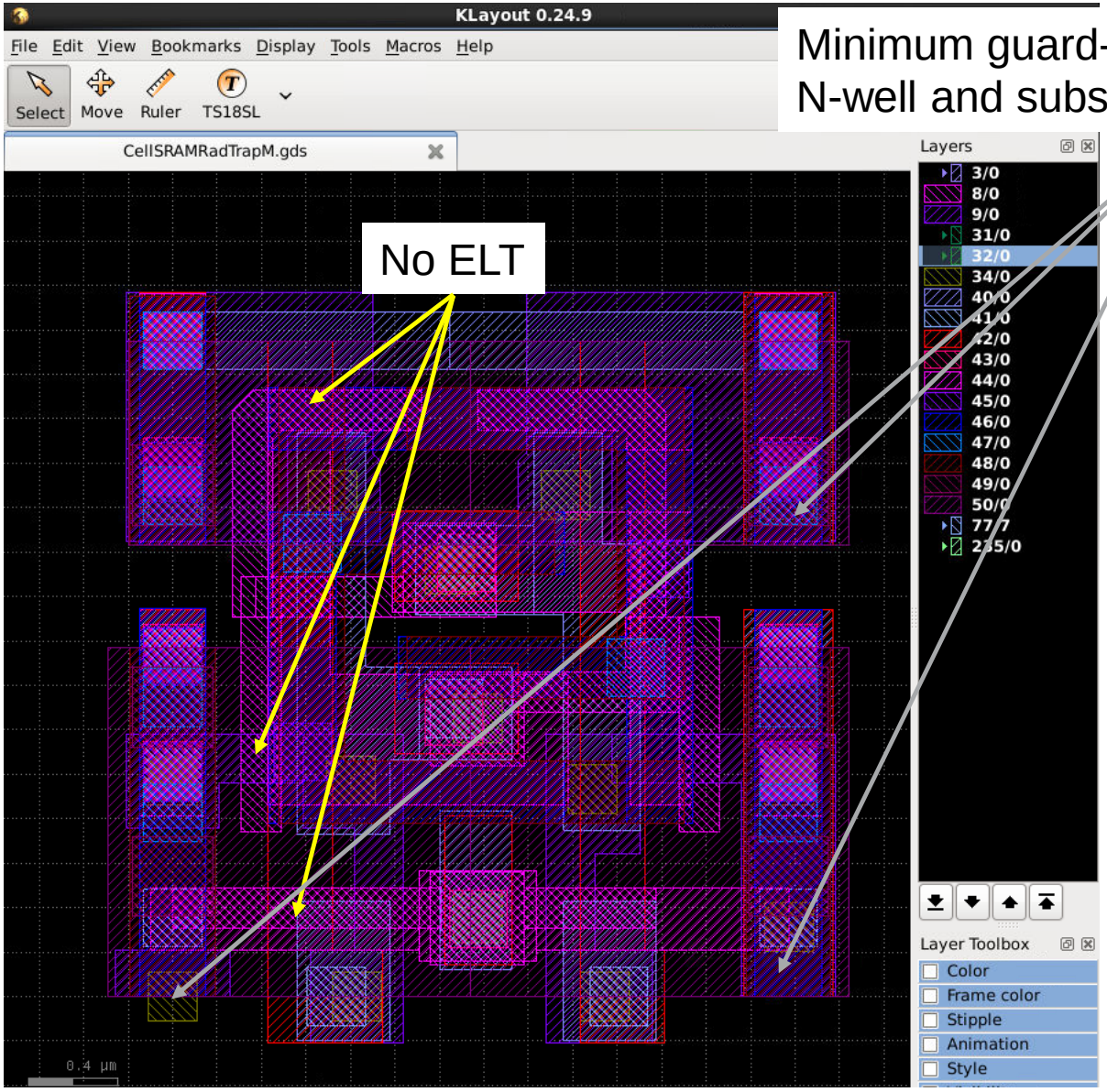
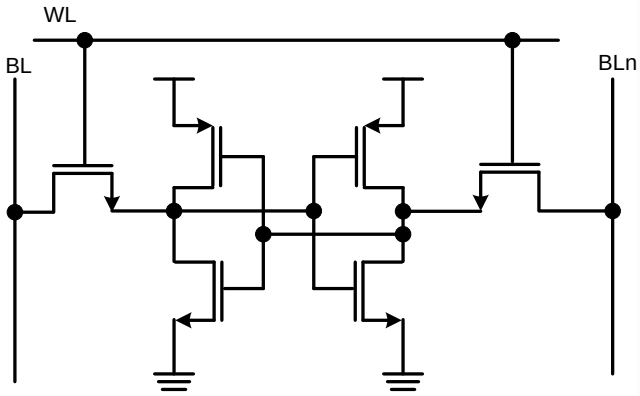
SRAM for Embedded Memories



Minimum guard-rings to avoid SEL → N-well and substrate biasing

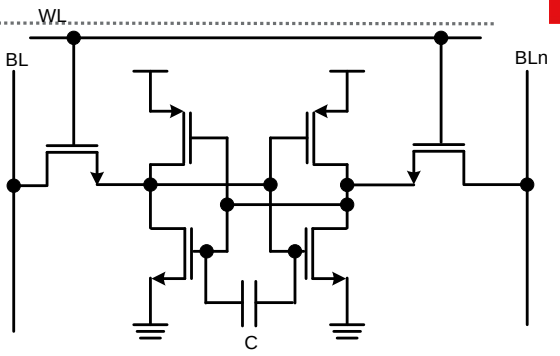


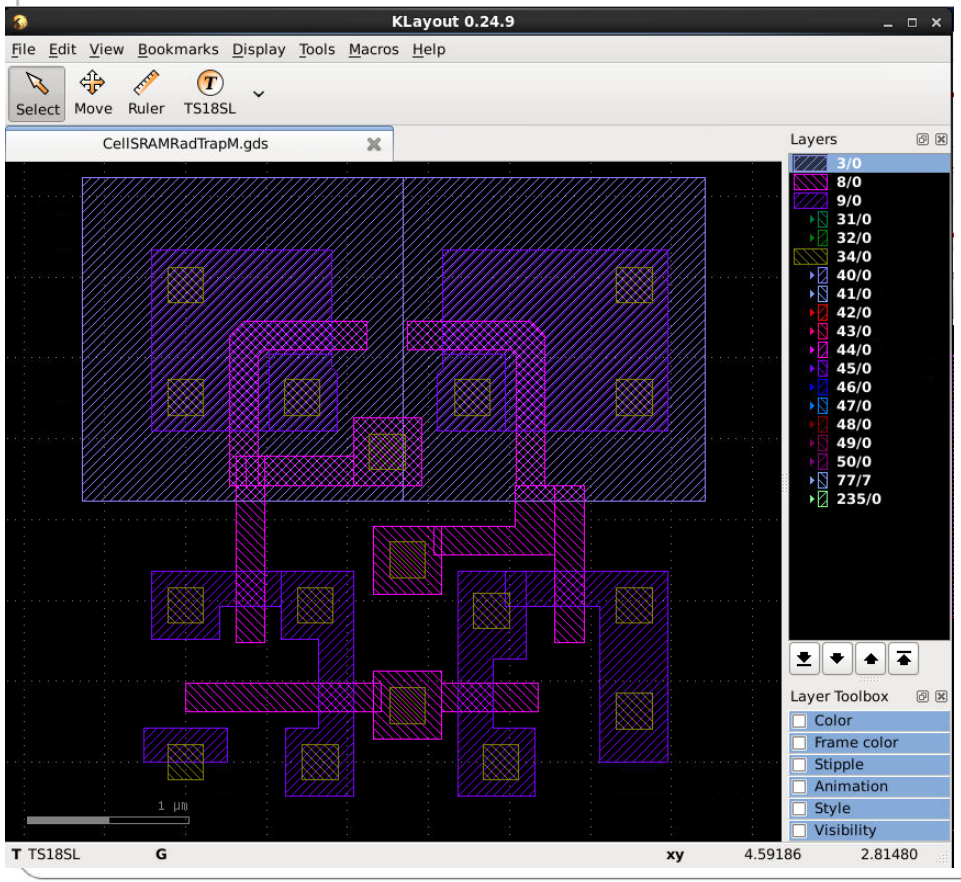
Courtesy of Cristiano Calligaro

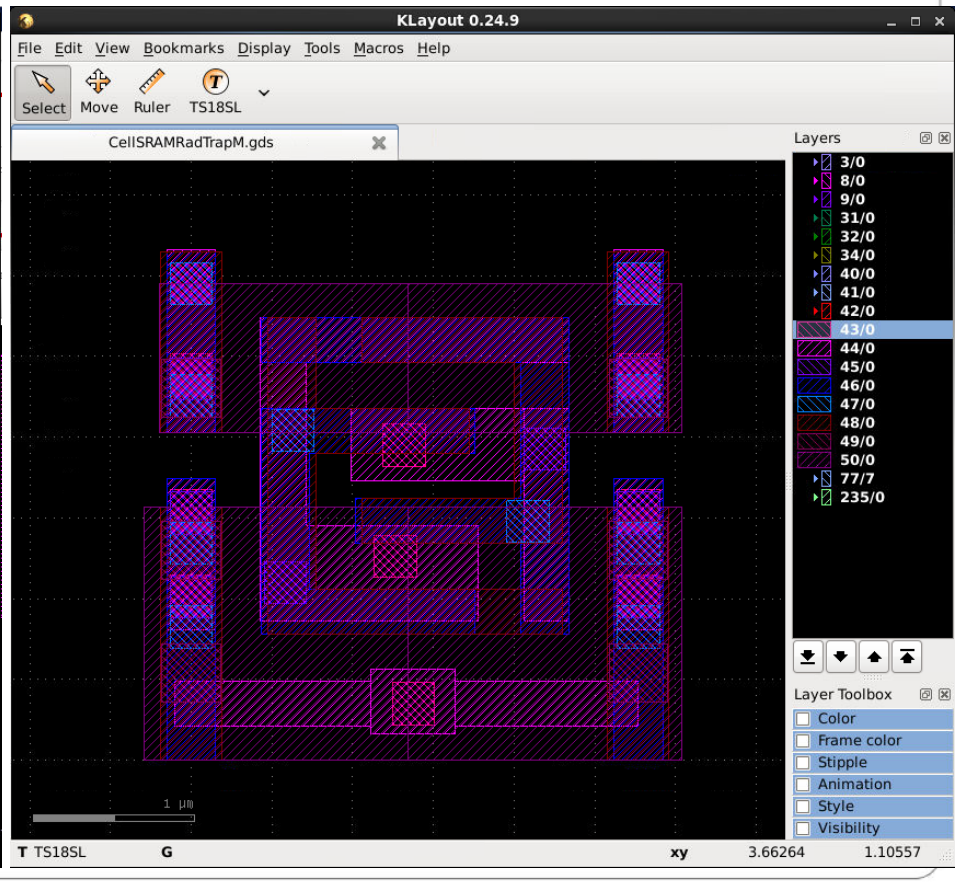
SRAM Cell Trade-off

Fringe capacitor (M3-M4-M5) to reduce SETs

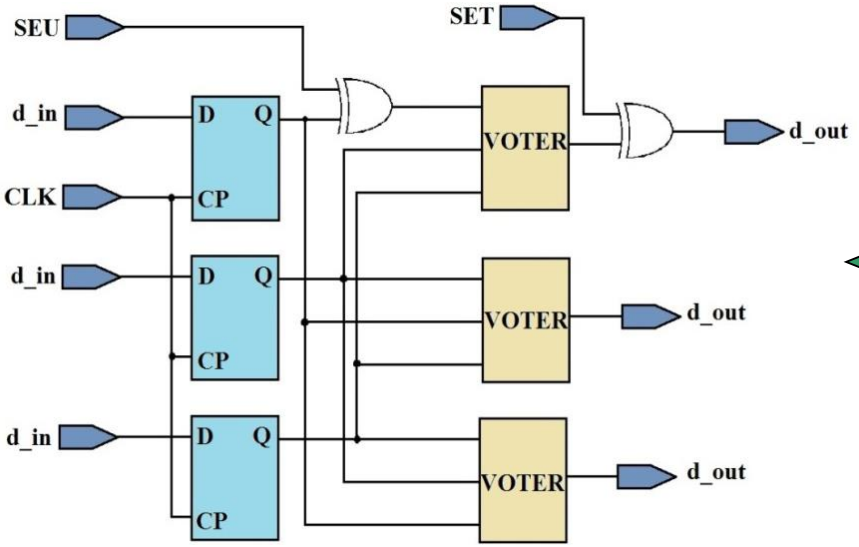
Courtesy of Cristiano Calligaro





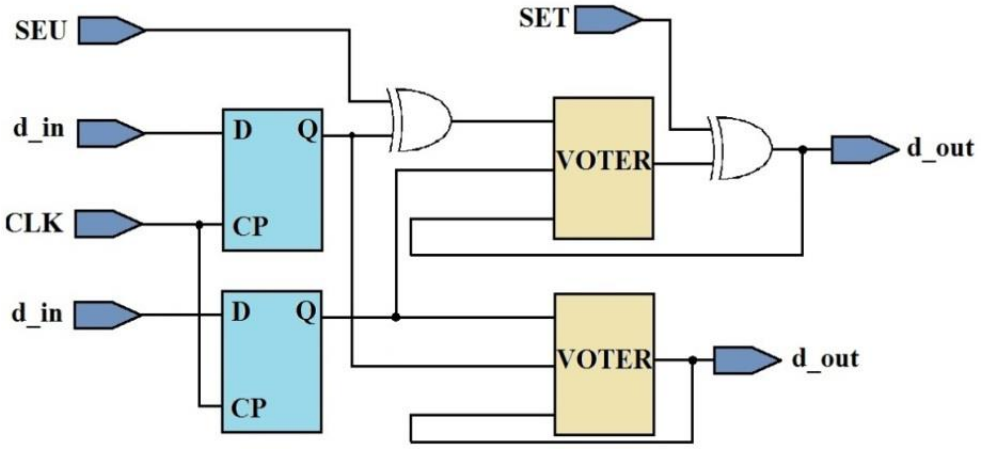


Fault-Tolerant Circuits



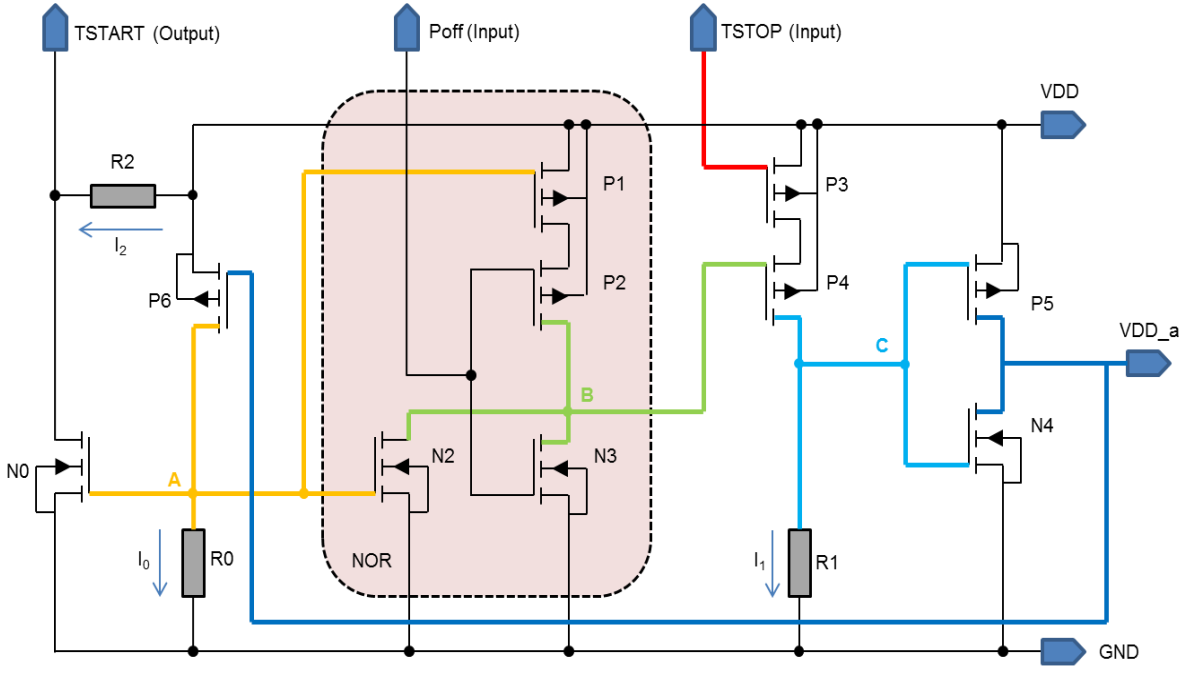
TMR provides a high fault protection but at the expense of increased chip area, power consumption, and cost

In order to reduce the chip area overhead and keep the design reliability high, a DMR approach is proposed



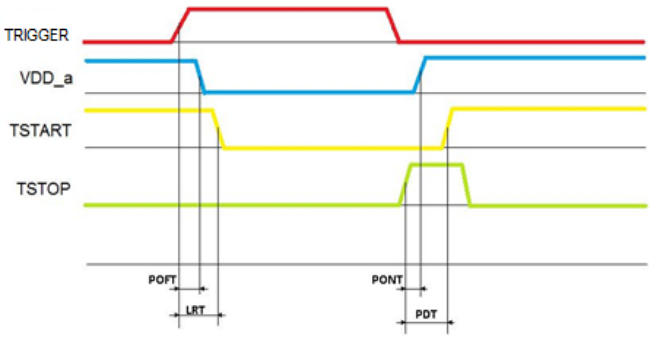
SEL Protection Switch (SPS)

- Current sensing and power switching
  - Transistor P5 senses the supply current (the higher current, the lower output voltage VDD_a)
  - Feedback activates transistor P6 when VDD_a is under the threshold voltage
  - Output TSTART of transistor N0 triggers a timer

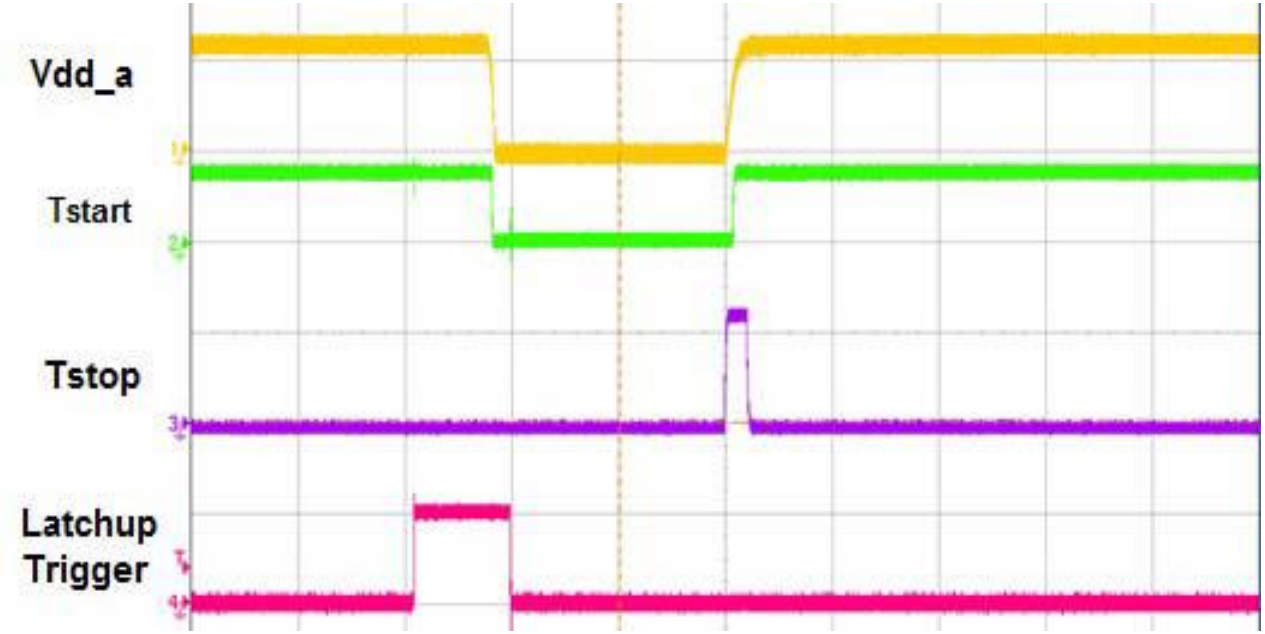


V. Petrovic et al., Microelectronics Reliability, 2014.

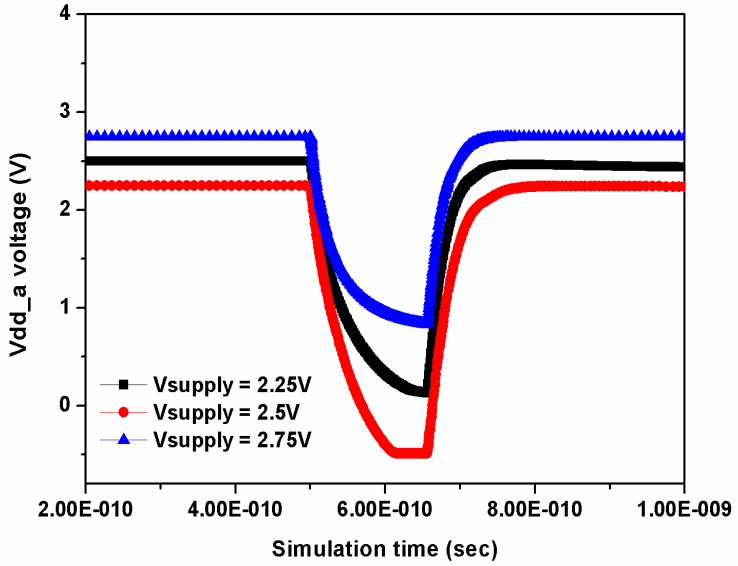
SPS Timing Diagram and Parameters

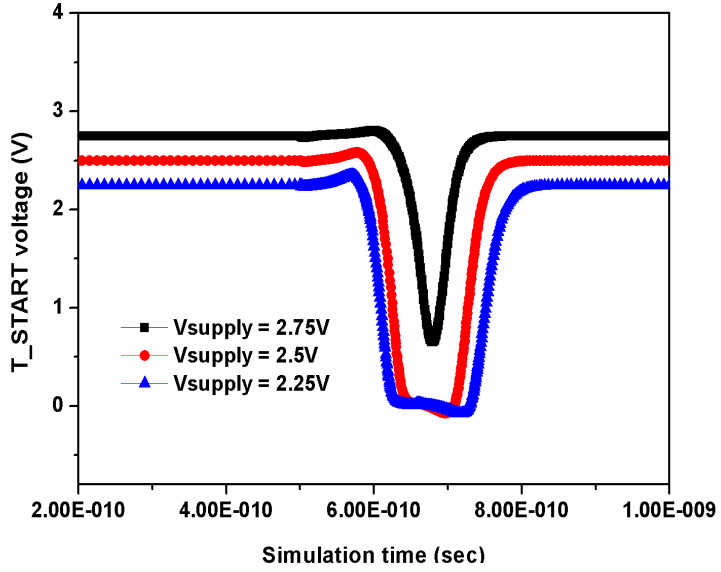


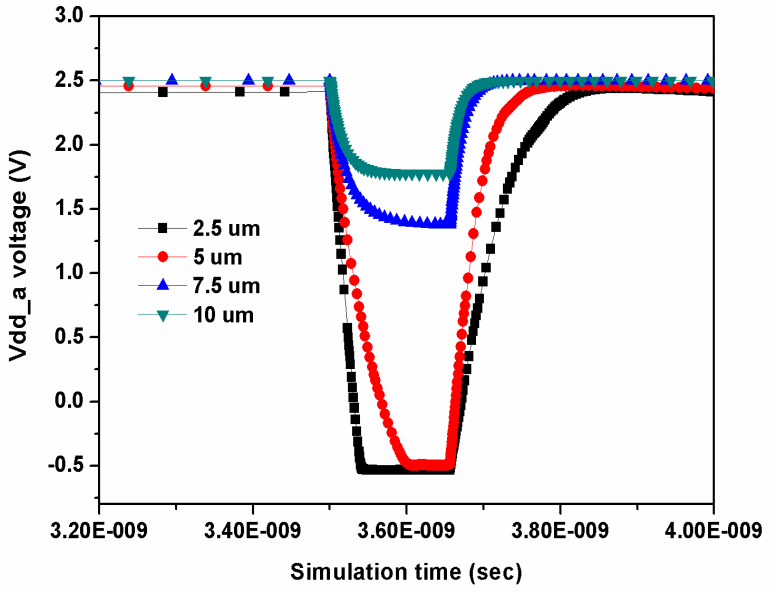
	POFT	LRT	PONT	PDT	MAT
Simulated	55.19 [ps]	76 [ps]	487 [ps]	786.5 [ps]	700 [ps]
Measured	120 [ps]	440 [ps]	1.42 [ns]	1.71 [ns]	2 [ns]

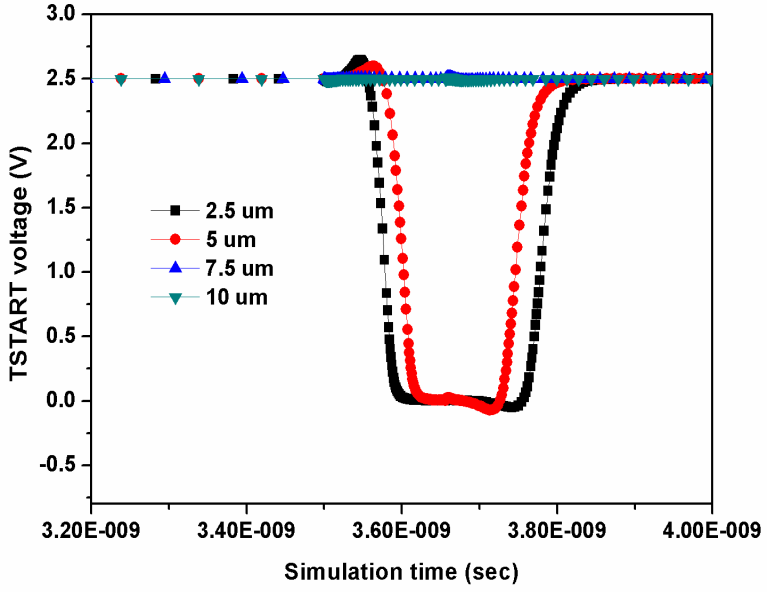


Supply Voltage and Channel Width Effects on SPS Response

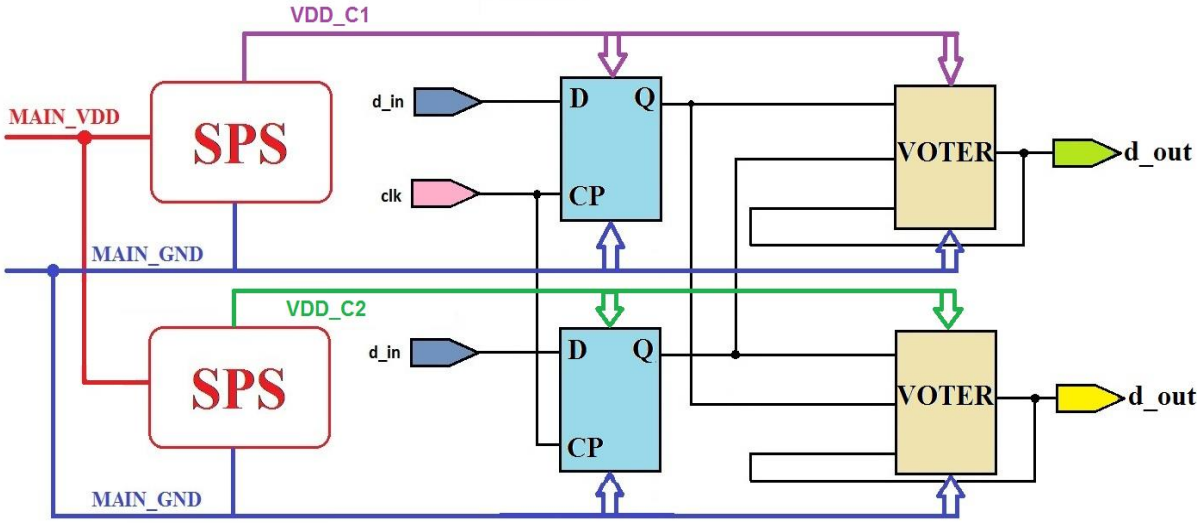


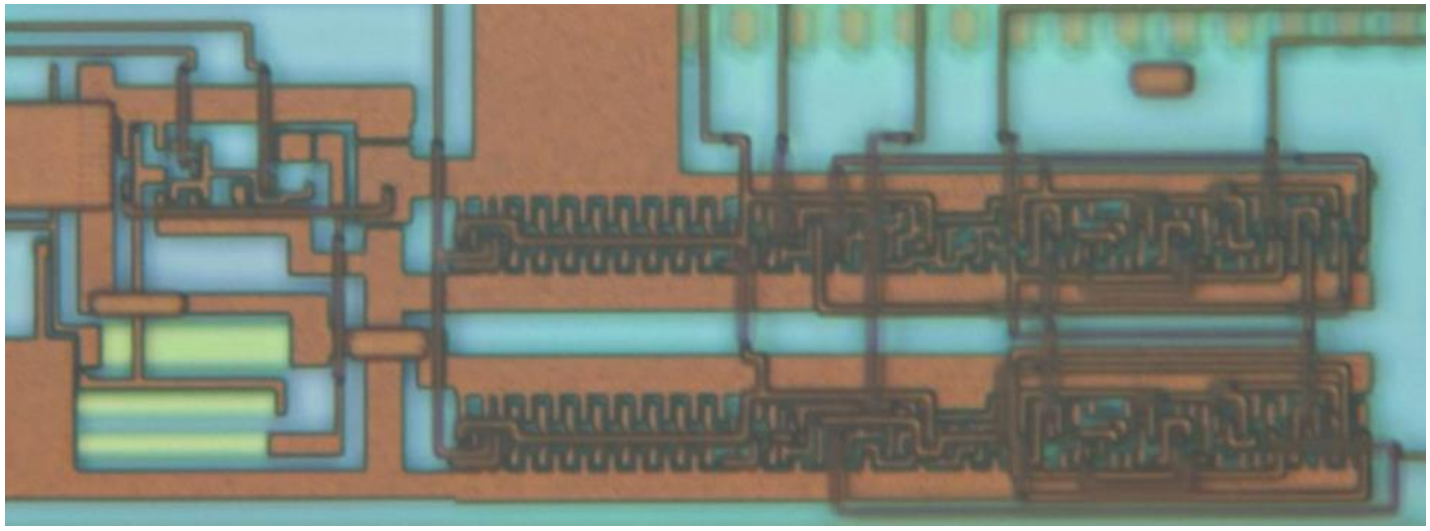




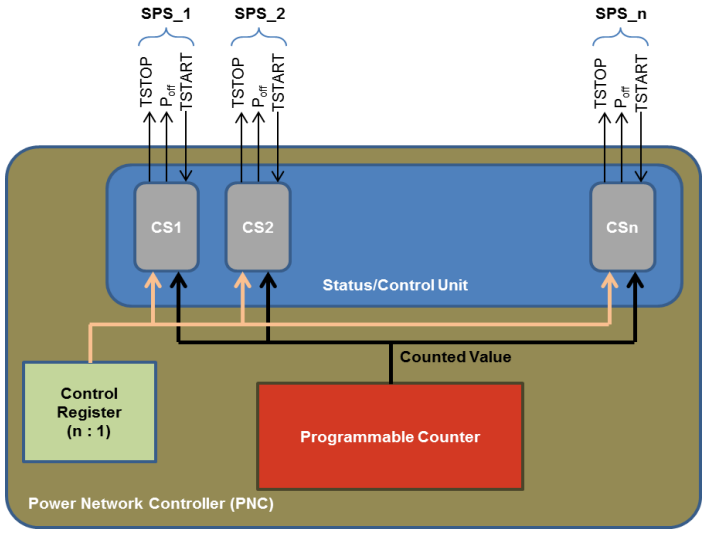


Integration of DMR and SPS



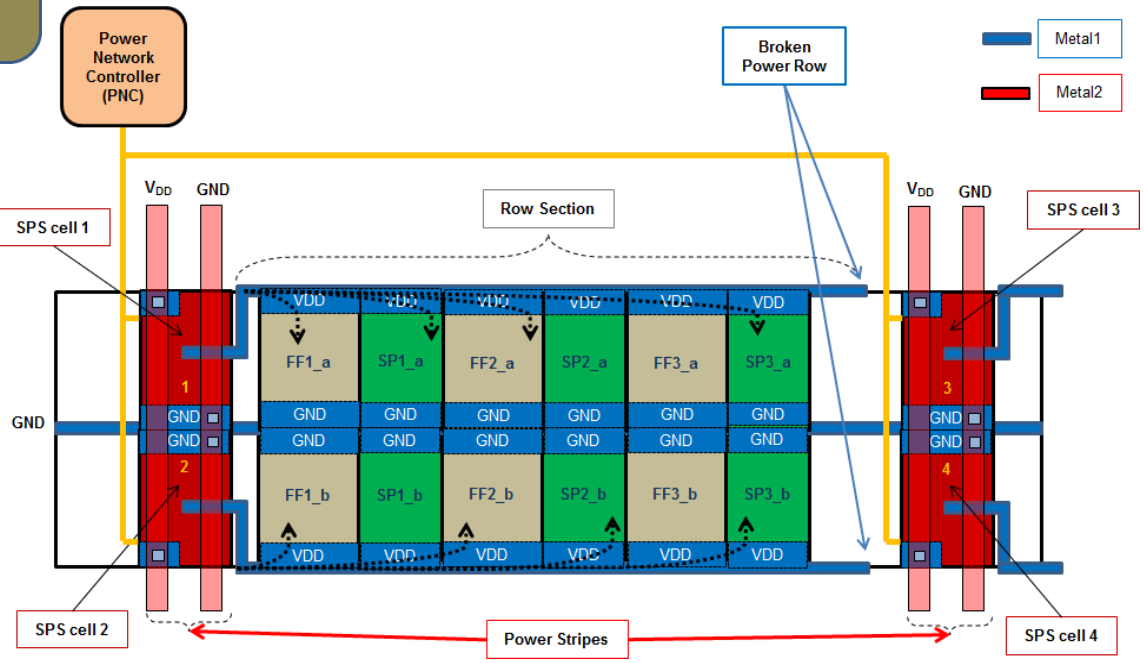


SPS Placement and Control

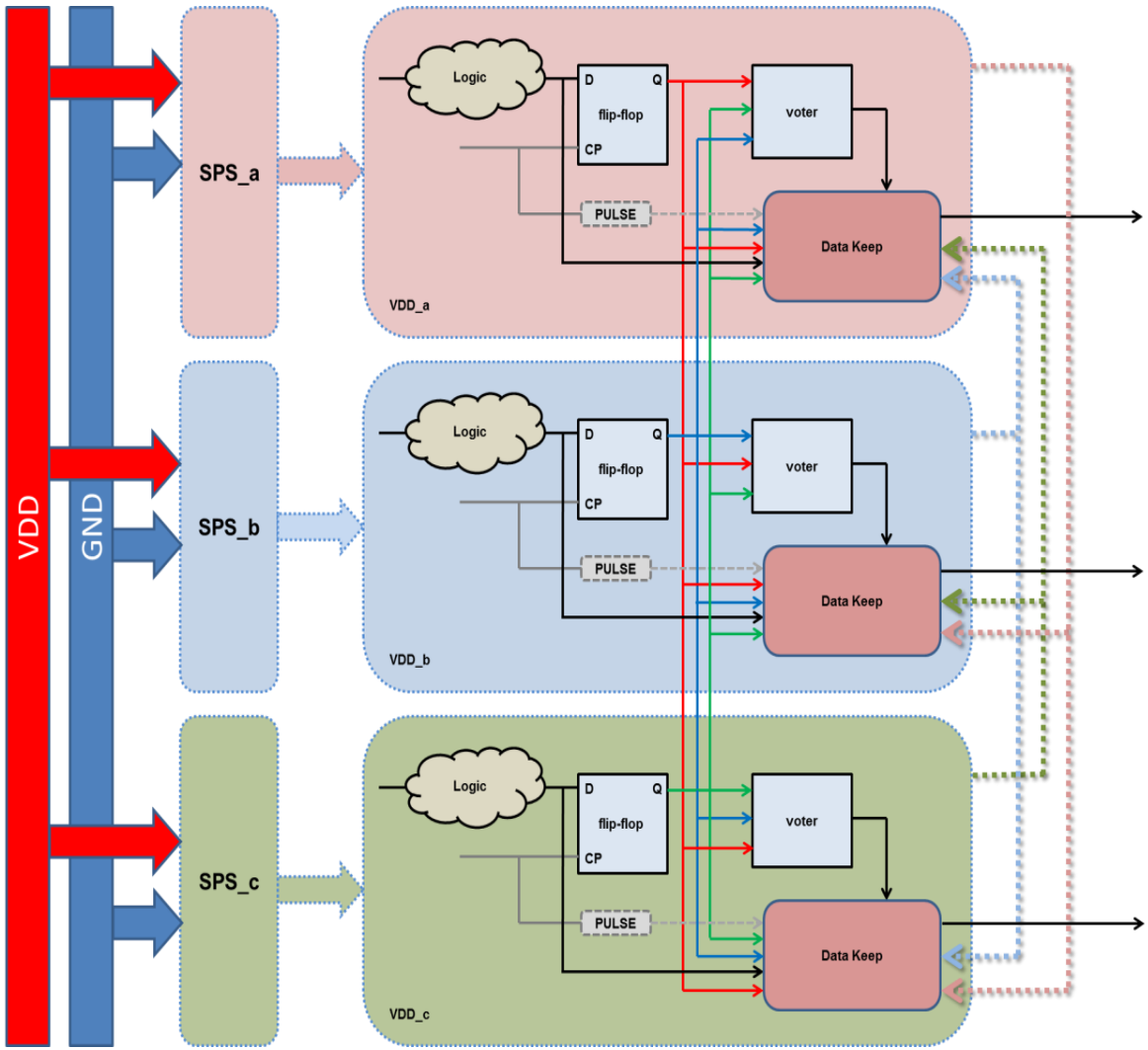


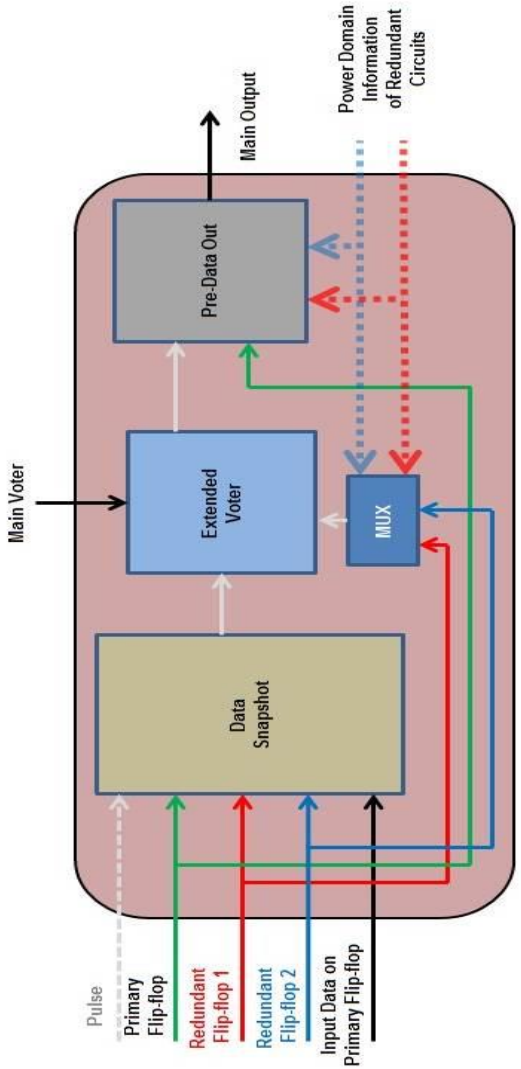
- PNC sets the period of latchup protection mode
- If the latchup occurs, TSTART activates the corresponding control interface which has to save the current counter value
- When the protection phase is over, the control interface activates the TSTOP signal

- It is possible to detect multiple latchup effects
- Control register generates the Poff signal and can be accessed by the system processor

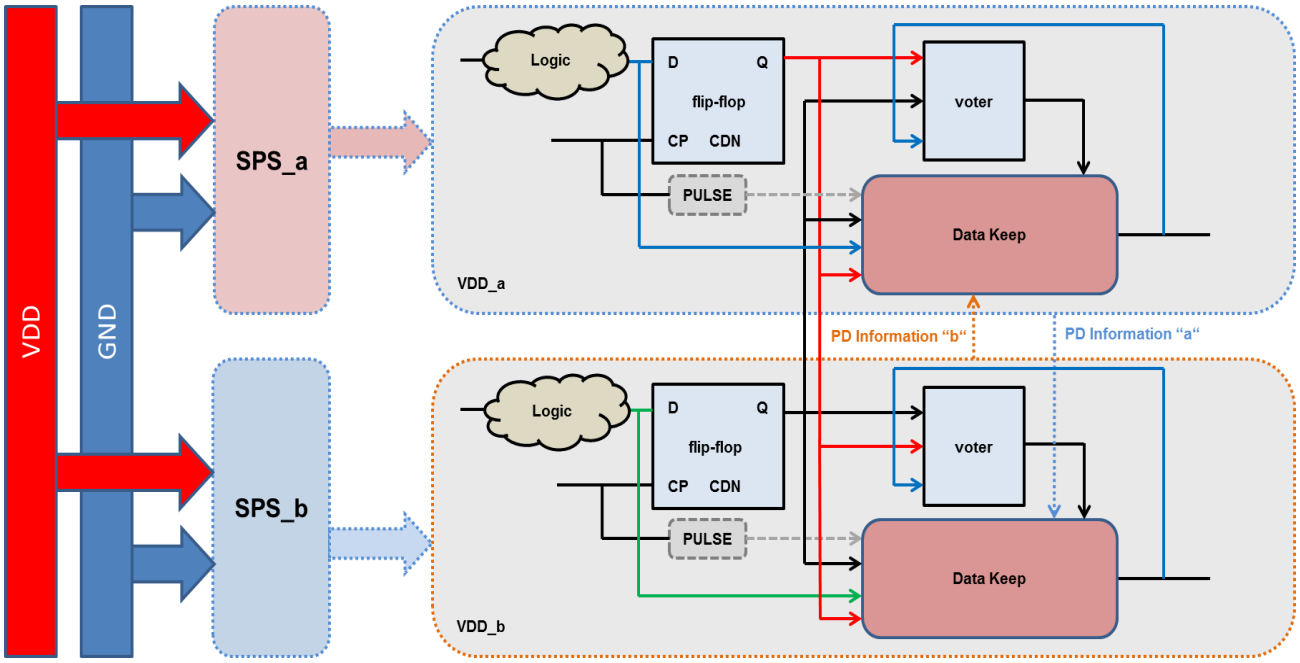


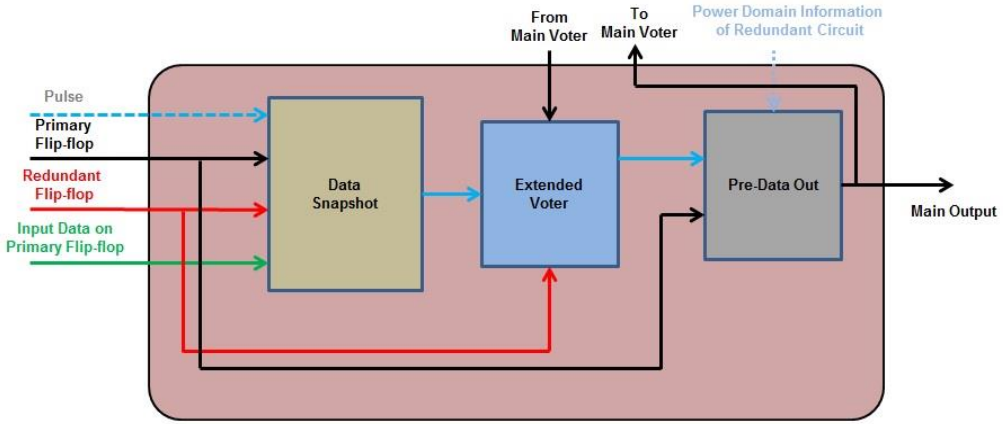
TMR Circuit with Latchup Protection



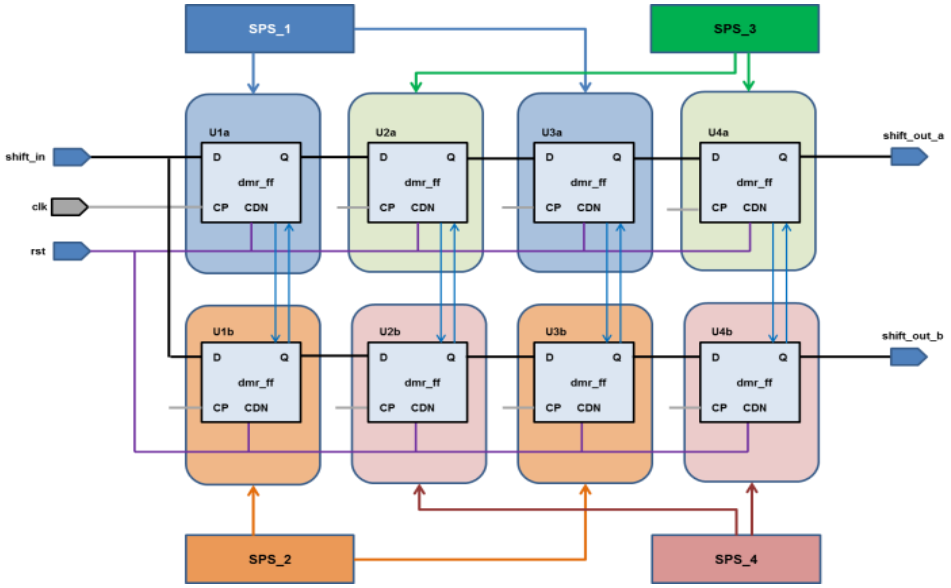


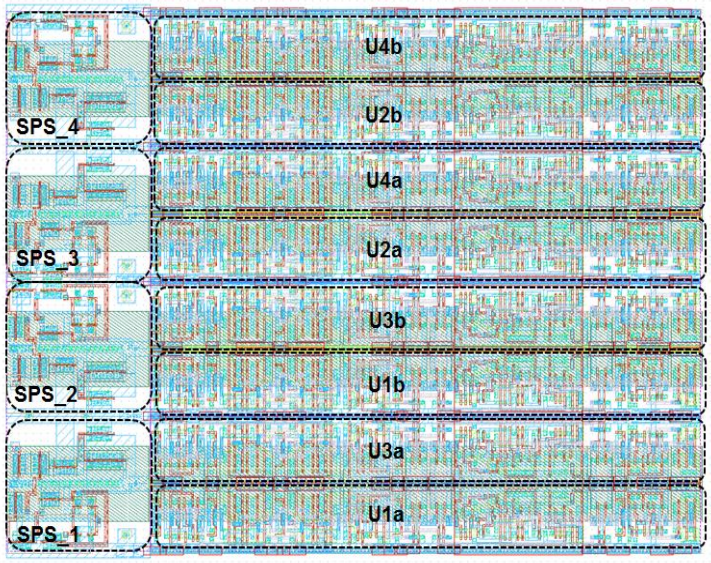
Self-voting DMR Circuit with Latchup Protection

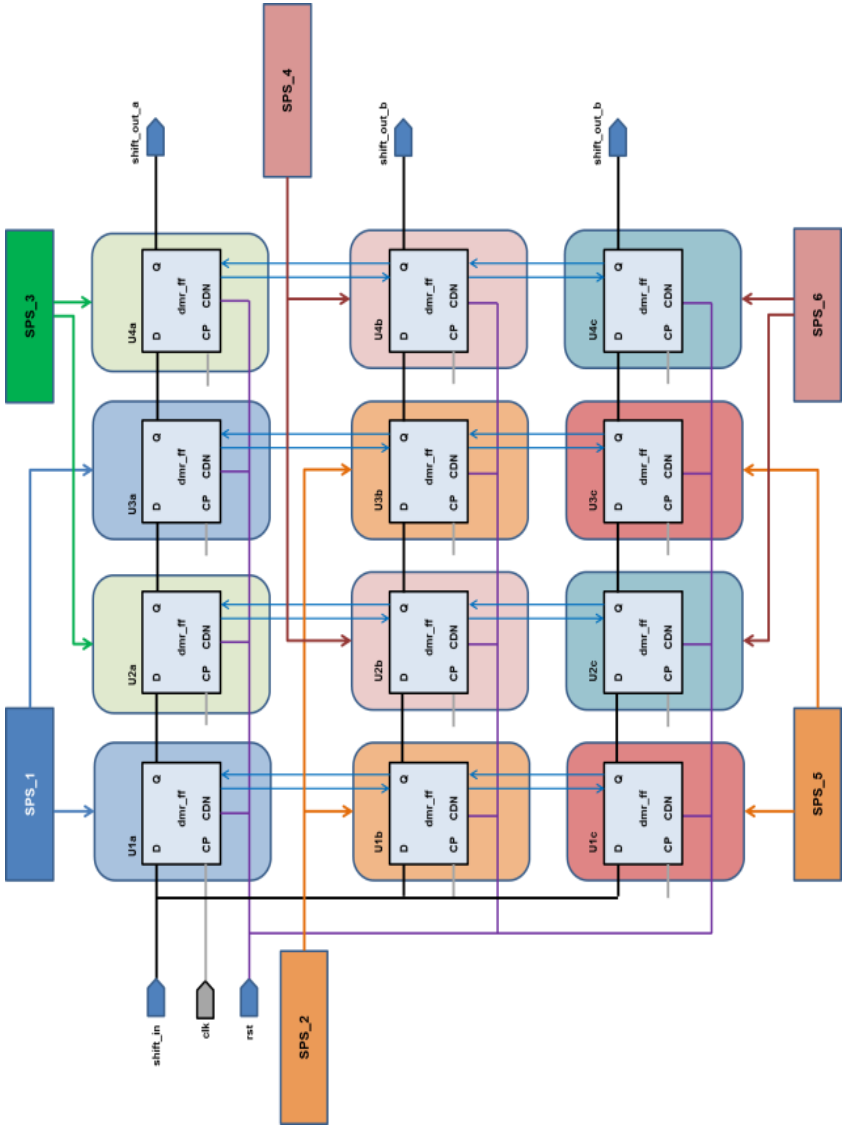




DMR and TMR Shift Registers (including SPS)

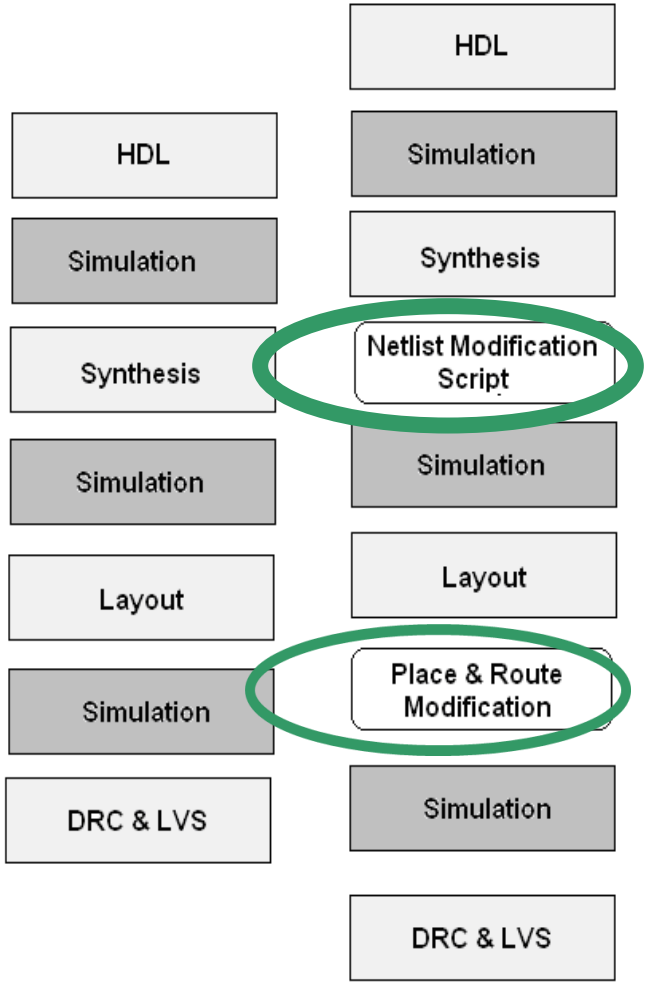






Design Flow Modifications

- Use of the standard design tools
- Flip-flops are replaced by TMR or DMR storage elements (FF and voter)
- Duplication of the original net-list
  - Power domains of the original and redundant net-lists are separated
- Memories include protection bits and EDAC logic
- SEL protection switches are placed in layout phase under the power stripes instead of filler cells
- SPS power network is connected in power routing phase to the main power network



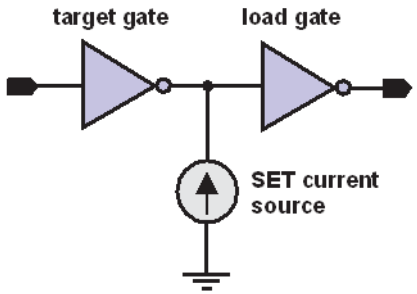
Fundamentals of SETs: Parameters and Modeling

- Irradiation parameters
  - Particle energy
  - Direction/location of particle strike
- Technological parameters
  - Channel length
  - Doping profiles
- Design parameters
  - Transistor size
  - Load capacitance
- Operating parameters
  - Supply voltage
  - Temperature

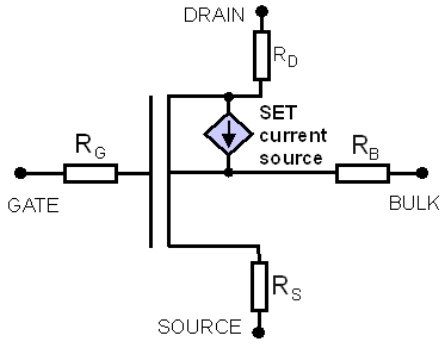
- SET modeling
  - SET current pulse generation
    - Current pulse source in the target gate of the circuit
  - SET voltage pulse generation
    - Current-induced voltage pulse at the gate output
  - SET voltage pulse propagation
    - If not electrically or logically masked, induced voltage pulse propagates through the combinational logic
  - SET voltage pulse latching
    - Voltage pulse arrives at the input of a sequential element within the latching window
  - Critical charge
    - Minimum charge (induced by irradiation) needed to cause a SET

Classification of SET Current Models

- Macro-modeling
  - Current source is implemented as a stand-alone module



- Micro-modeling
  - Current source is implemented within the target transistor
  - Transistor model is a necessity



- Voltage-independent current models
  - Rectangular current pulse model
  - Double-exponential current pulse model
  - Freeman's current model
  - Hu's current model
  - Diffusion current model
  - Roche's current model
- Dual voltage-independent current models
- Voltage-dependent current models
- Piecewise interpolation models
- Look-up table models
- Switch-based models

Voltage-Independent Current Models

$$I_{SET}(t) = \begin{cases} I_{AMP}, & \tau_1 < t < \tau_2 \\ 0, & \tau_1 > t > \tau_2 \end{cases}$$

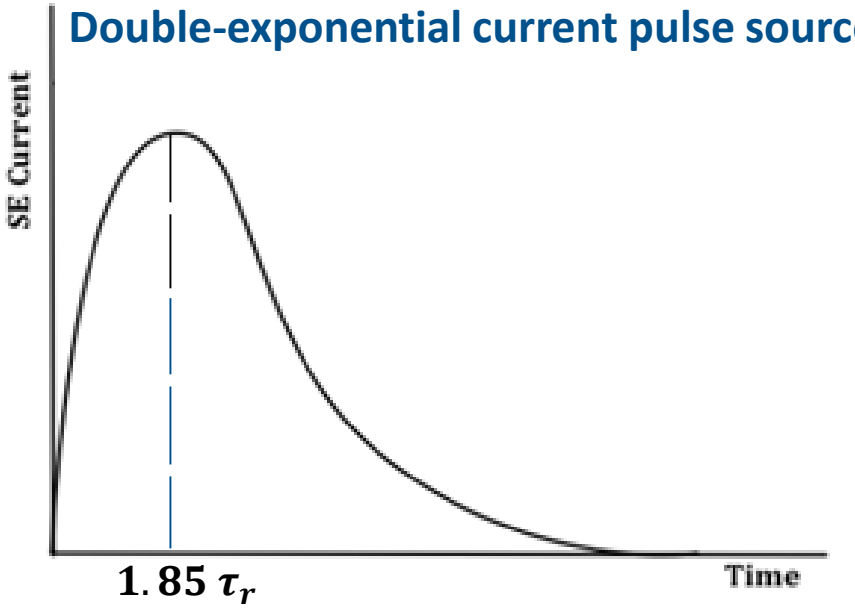
Rectangular current pulse source

Double-exponential current pulse source

$$I_{SET}(t) = \frac{Q_{COLL}}{\tau_f - \tau_r}\left(e^{-t/\tau_f} - e^{-t/\tau_r}\right)$$

$$\tau_f = \frac{k\varepsilon_0\varepsilon_r}{q\mu N_D}$$

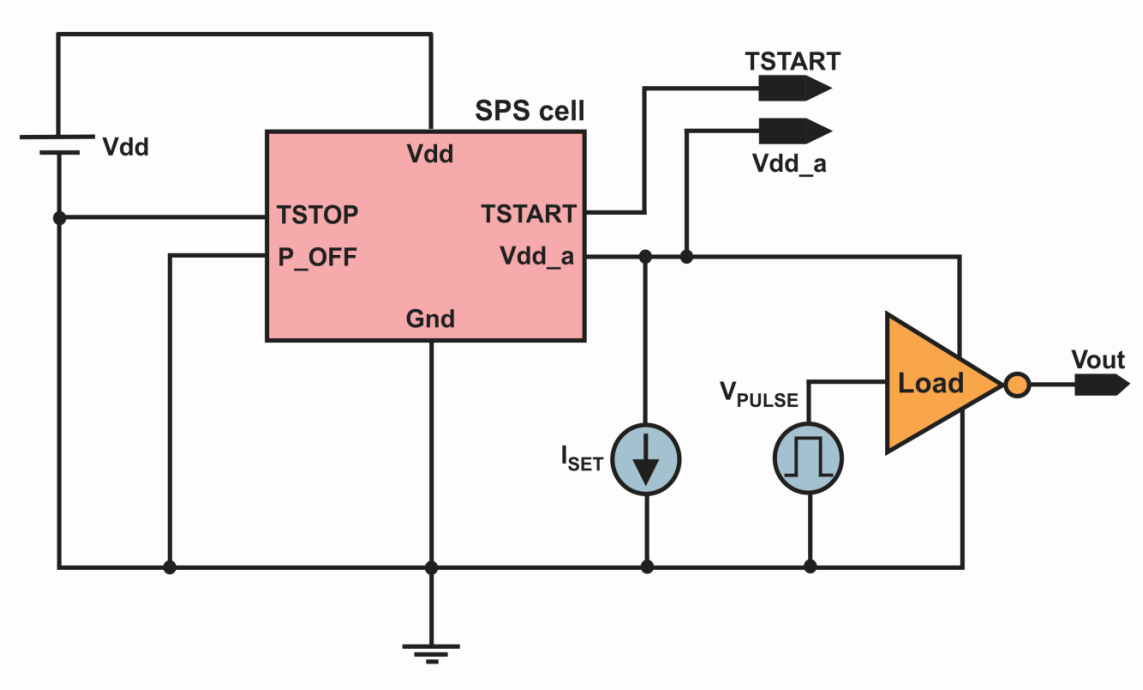
$$\tau_r = \frac{\tau_f}{4}$$



- Very simple for implementation in SPICE
- Neglect the dependence of the SET current on the node voltage

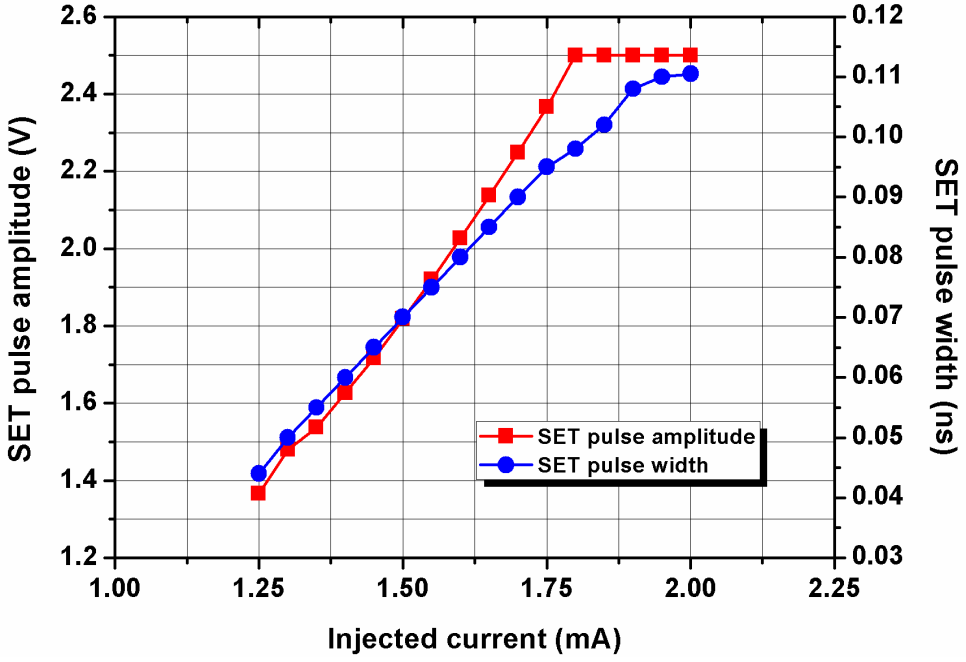
A Use Case: SEL Protection Switch

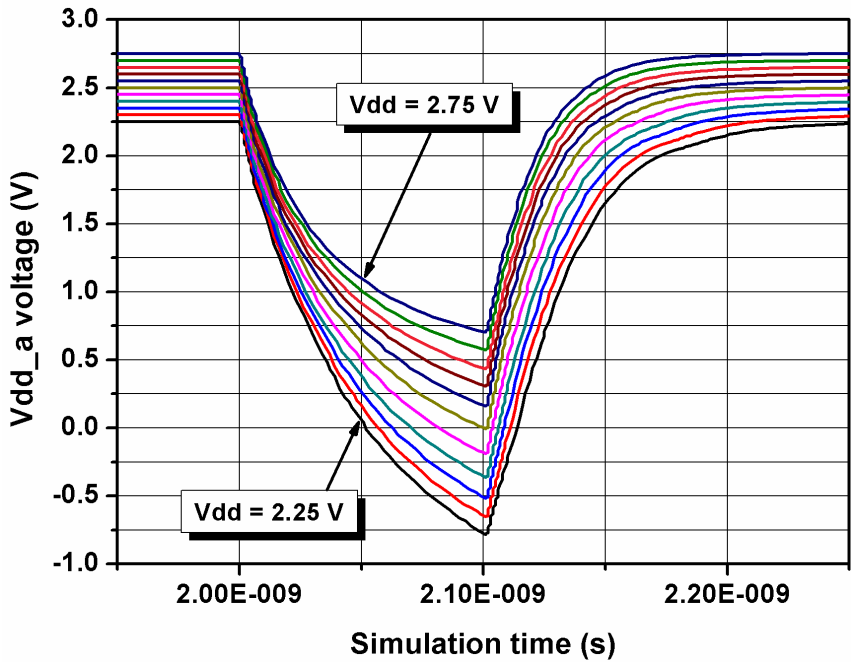
- SET pulses with an amplitude larger than Vdd/2 will result in triggering false SEL alarms
- SET pulses with an amplitude larger than 10 % of Vdd may result in malfunction of standard cells
- Rectangular and double-exponential current pulse sources have been used as a SET simulation model



SET Analysis with Rectangular Model (Current and Vdd)

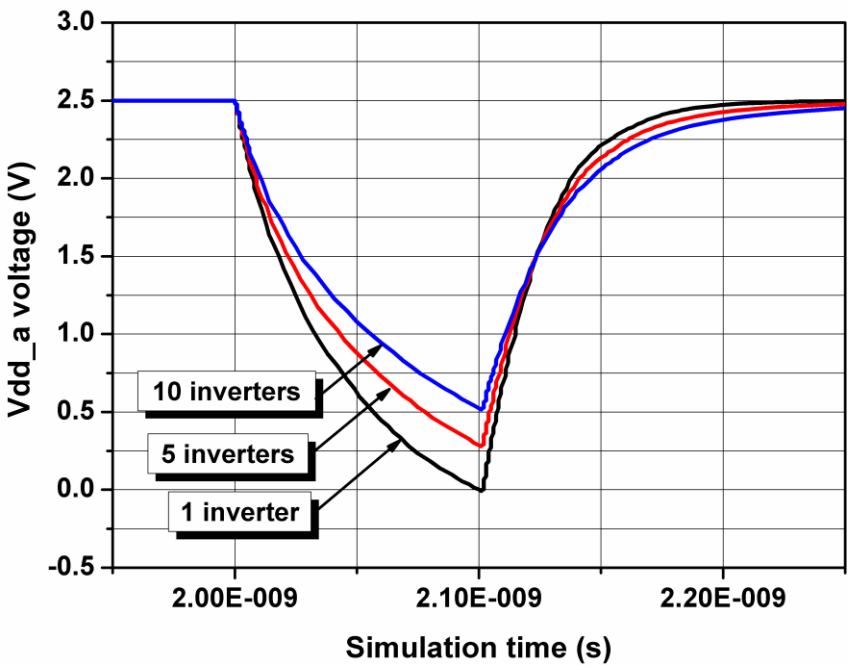
- SET-induced voltage pulse at the output of SEL protection switch was analyzed using a rectangular current model
- Amplitude and width of SET voltage pulse increased with the increase of the amplitude of rectangular current pulse
- Amplitude and width of the SET voltage pulse decreased as the supply voltage was increased

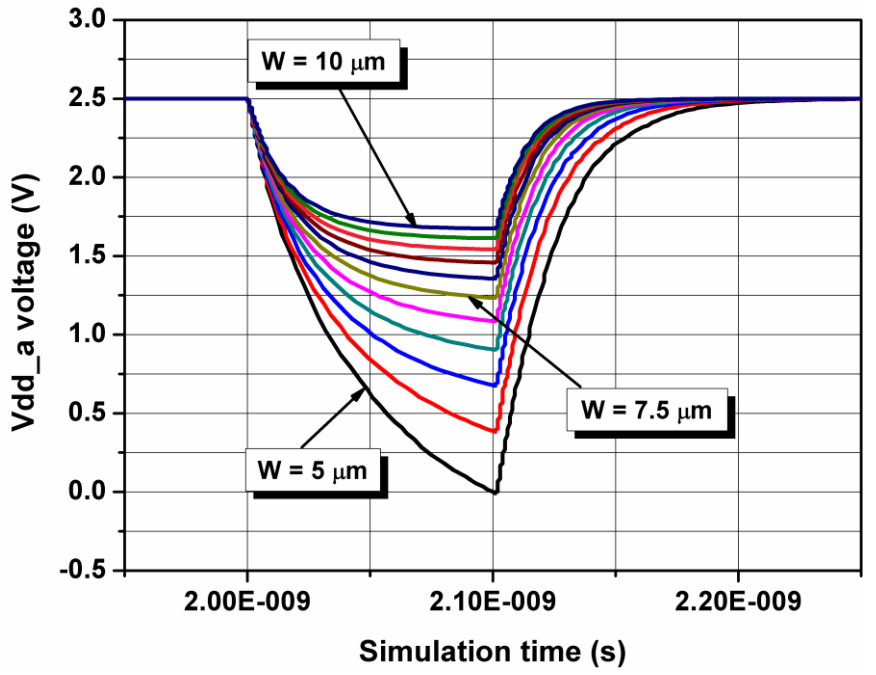




SET Analysis with Rectangular Model (Load and PMOS Width)

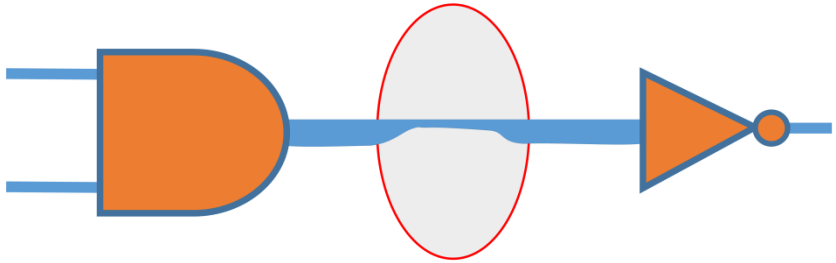
- Increasing the number of load inverters connected to the output of SPS cell resulted in the decrease of both amplitude and width of the SET voltage pulse
- Amplitude and width of the SET voltage pulse decreased as the width of PMOS sensor/driver transistor was increased
  - For a transistor width of 7.5 µm, the SPS cell was robust (SET voltage pulse was below Vdd/2) to SET-induced charge up to 180 fC



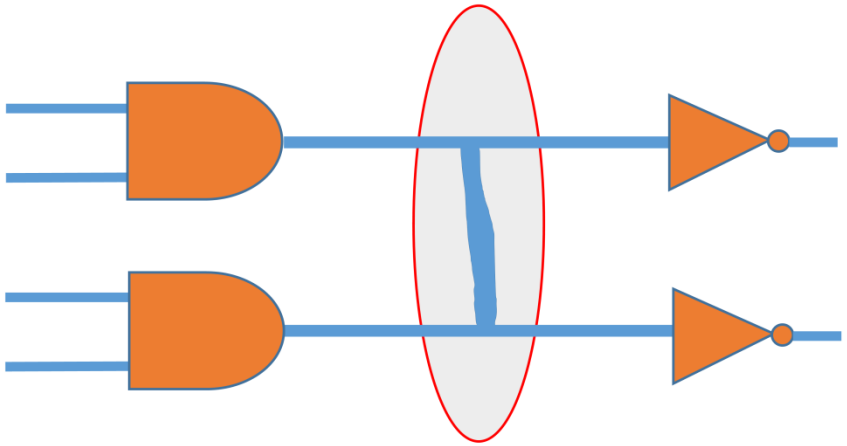


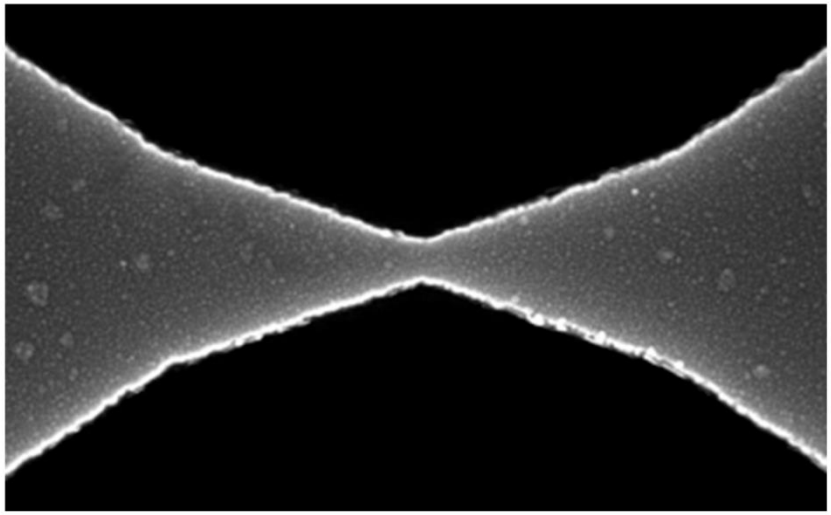
Manufacturing Defects

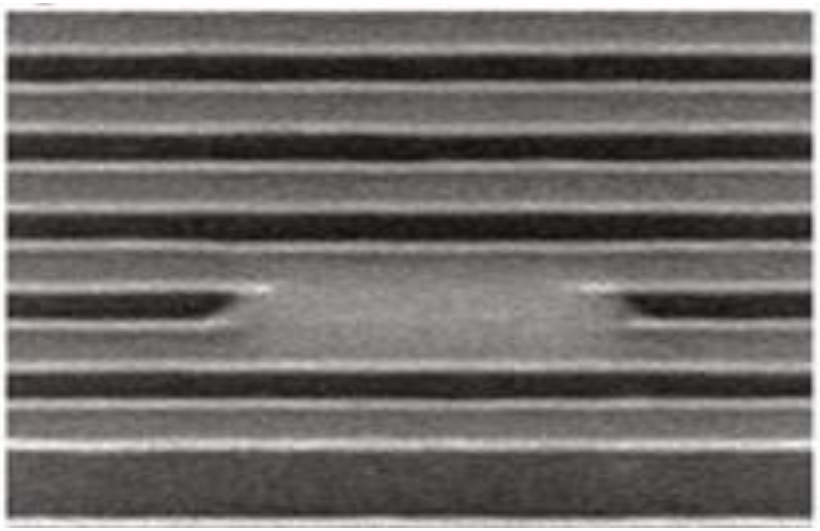
Resistive open defect



Resistive bridge defect

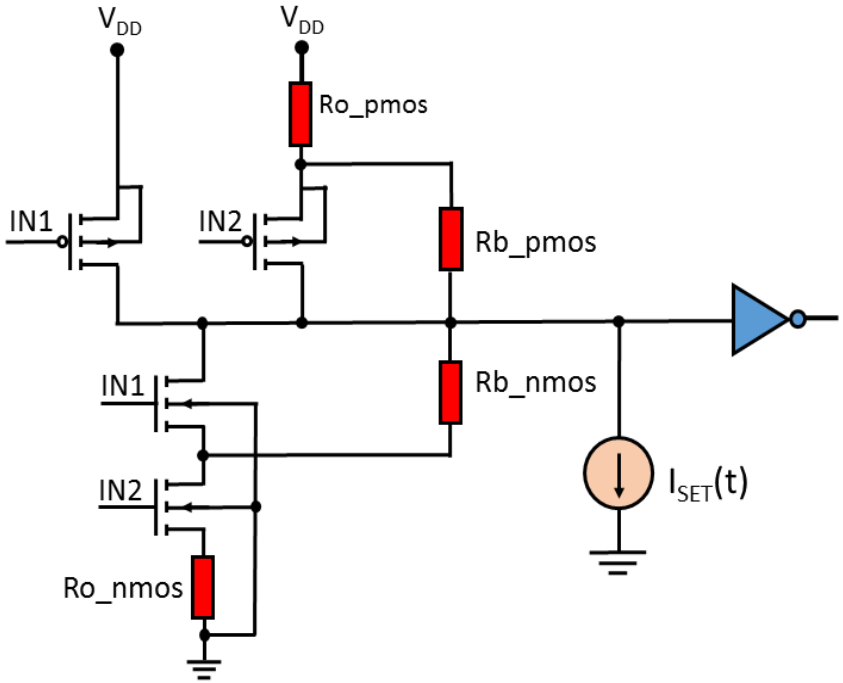






SET Response in Presence of Resistive Faults

- Goal: to evaluate SET response due to **intra-gate** faults
- 2-input NAND gate was used as a target circuit
- Analyzed faults:
  - *Resistive open faults Ro_pmos and Ro_nmos*
  - *Resistive bridge faults Rb_pmos and Rb_nmos*
- Resistance range – range of defect resistance for which the logic function of the circuit is not changed



Fault type	Resistance range (kΩ)
Ro_pmos	0.5 - 50
Ro_nmos	0.5 - 50
Rb_pmos	5 - 50
Rb_nmos	1 - 50

SET Model

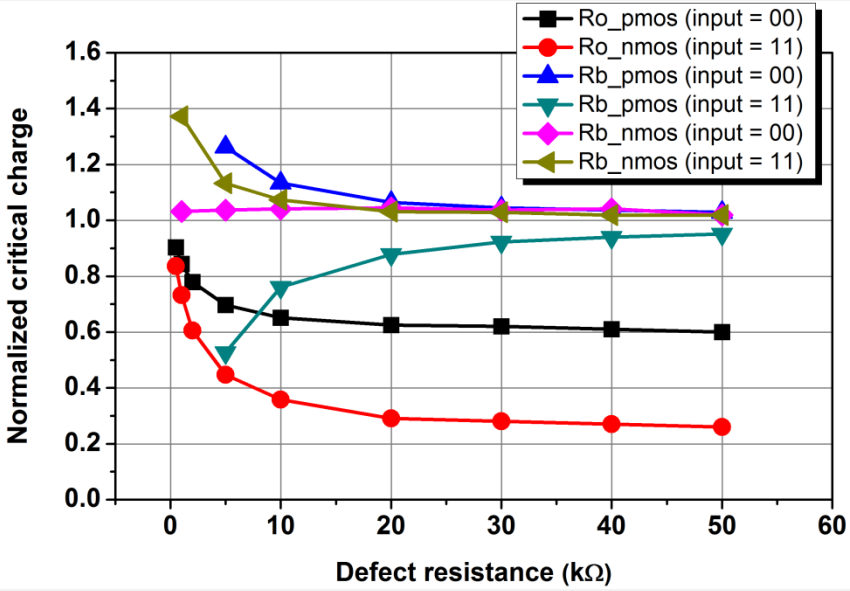
- SET effects were simulated with double-exponential current model,

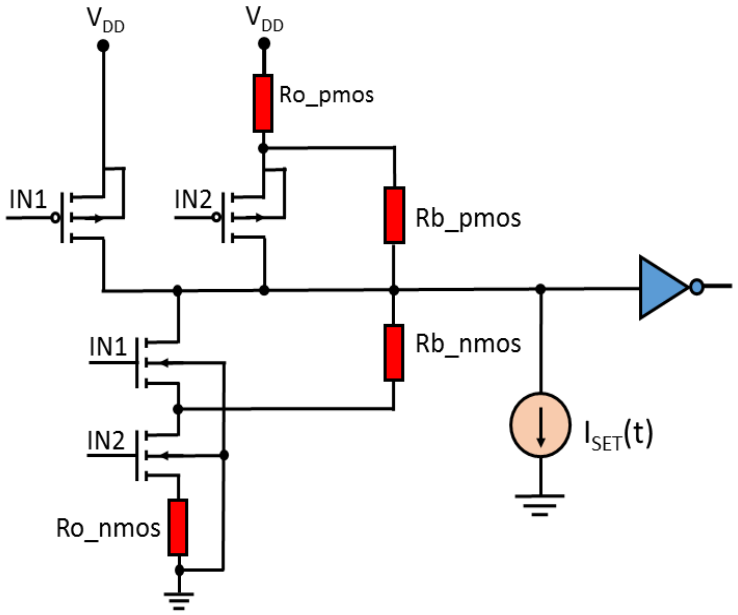
$$I_{SET}(t) = \frac{Q_{COLL}}{\tau_f - \tau_r}\left(e^{-t/\tau_f} - e^{-t/\tau_r}\right)$$

- Timing parameters of current pulse: τ_r= *10 ps and* τ_f= *50 ps*
- Critical charge (Q_{CRIT}): minimum value of Q_{COLL} causing the change of logic value at the output of circuit
- SET pulse width: determined for pulses with amplitude above Vdd/2
- SER was calculated as: ***SER = k · Flux · Area · exp(-Q_{CRIT}/Q_S)***

Q_{CRIT} Change due to Intra-Gate Faults

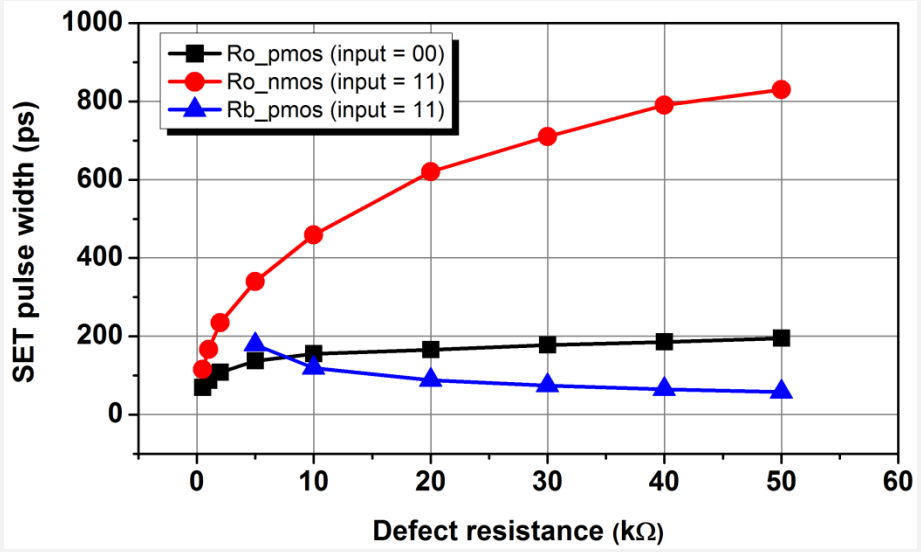
- Resistive open faults:
  - *Q_{CRIT} decreases by up to 80 % as defect resistance increases*
  - *SER increases by more than one order of magnitude*
- Resistive bridge faults have weaker impact on Q_{CRIT} and SER
- Response strongly depends on input logic levels

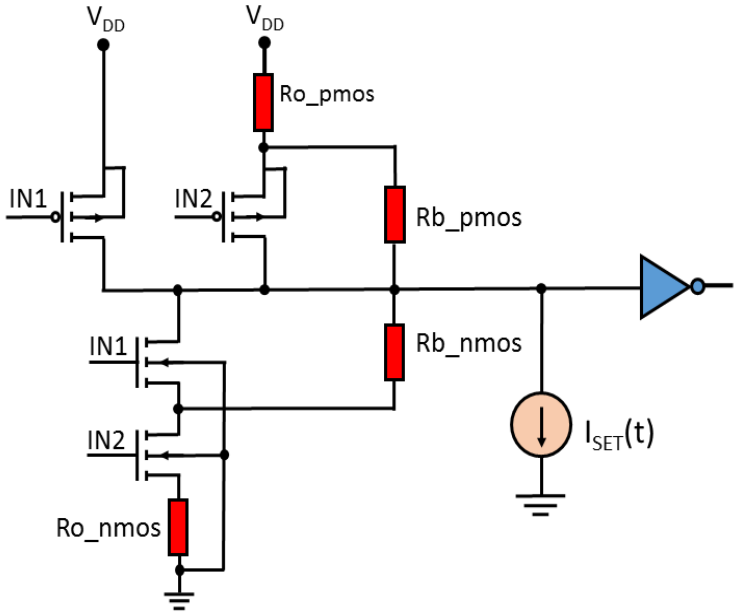




SET Pulse Width Change due to Intra-Gate Faults

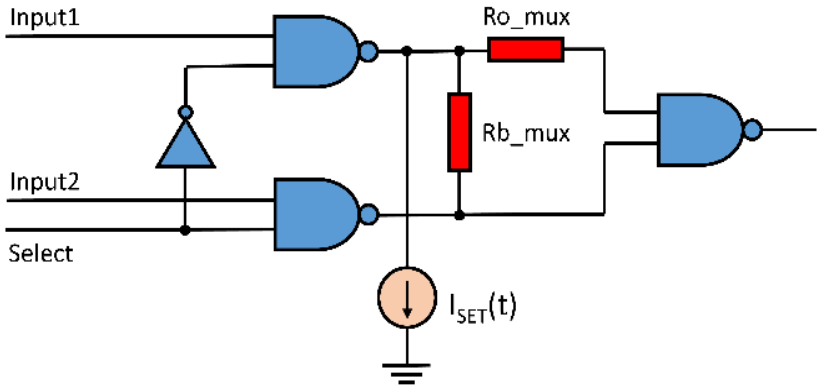
- Resistive open faults:
  - *SET pulse width increases as defect resistance increases*
  - *Input logic levels determine the sensitivity*
- Resistive bridge faults have negligible impact on SET pulse width

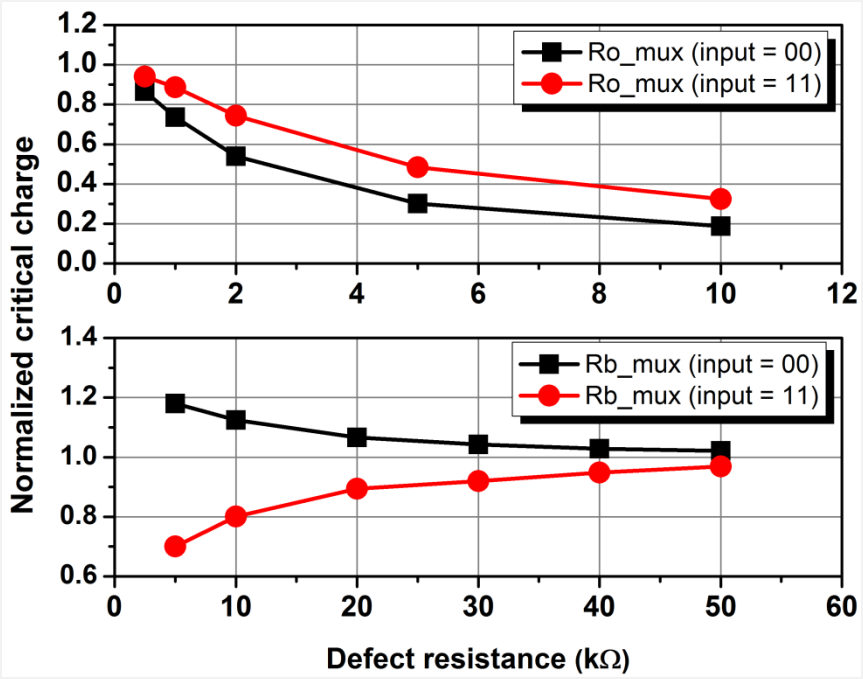




Q_{CRIT} Change due to Inter-Gate Faults

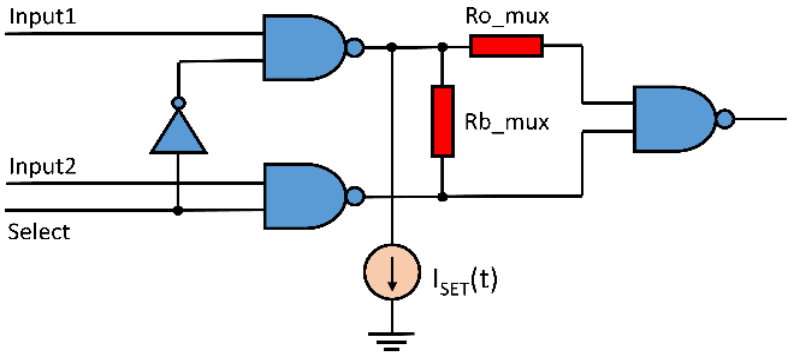
- Similar effects as for intra-gate faults:
  - *Q_{CRIT} decreases (SER increases) as defect resistance for open faults increases*
  - *Bridge faults may affect Q_{CRIT} and SER only for low defect resistance*

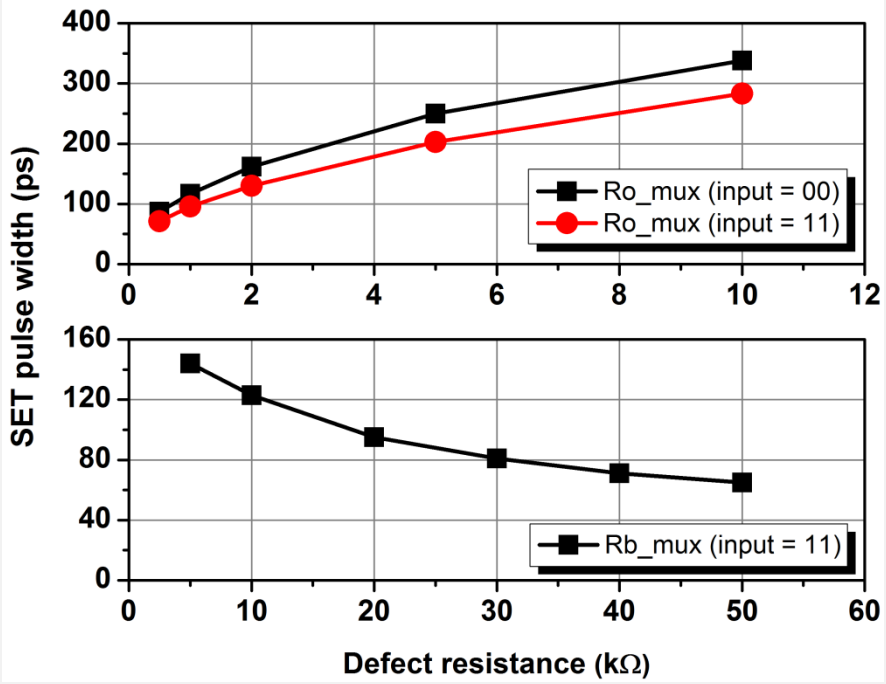




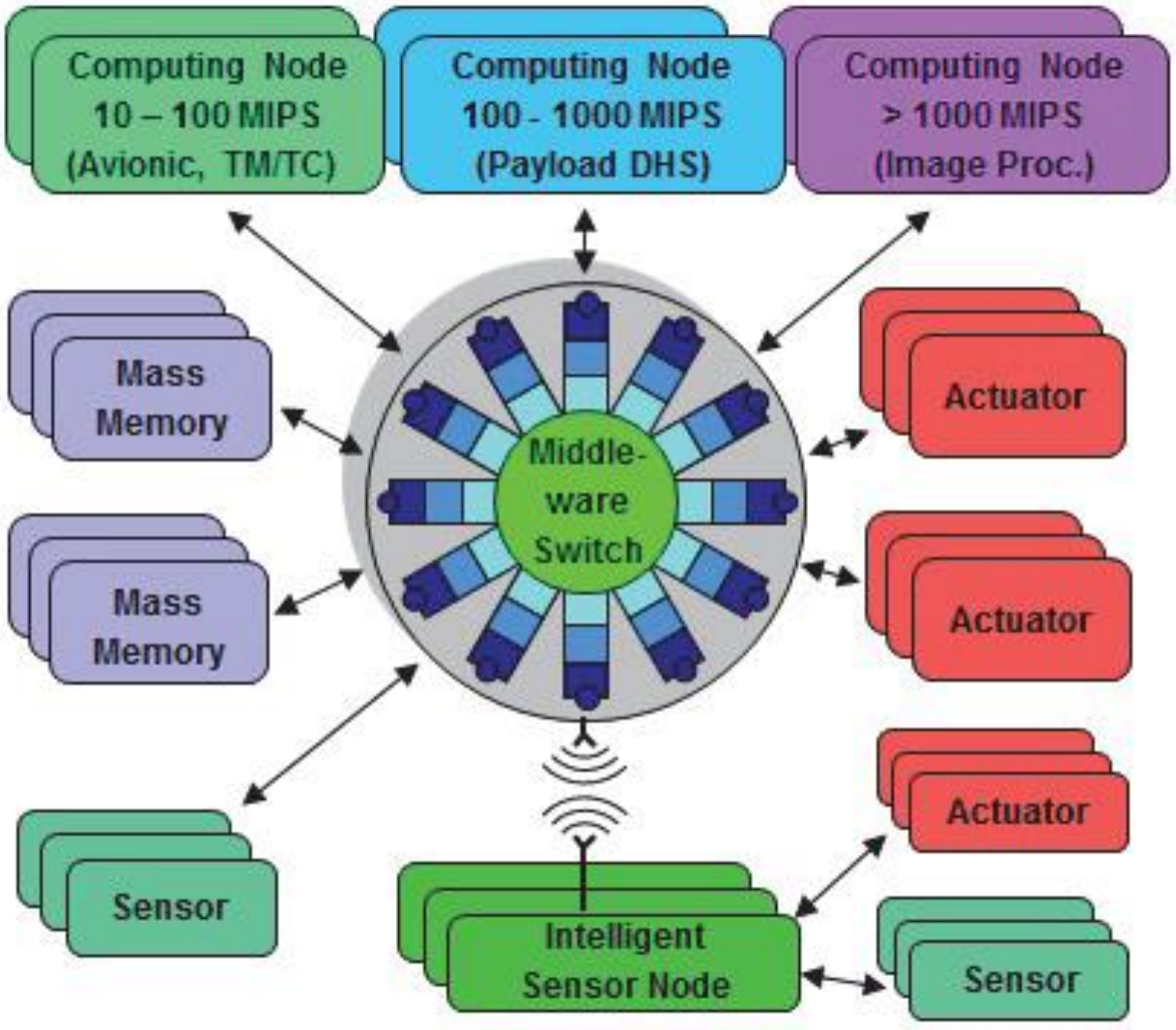
SET Pulse Width Change due to Inter-Gate Faults

- Similar effects as for intra-gate faults:
  - *SET pulse width increases significantly as defect resistance for open faults increases*
  - *Impact of bridge faults is weaker*

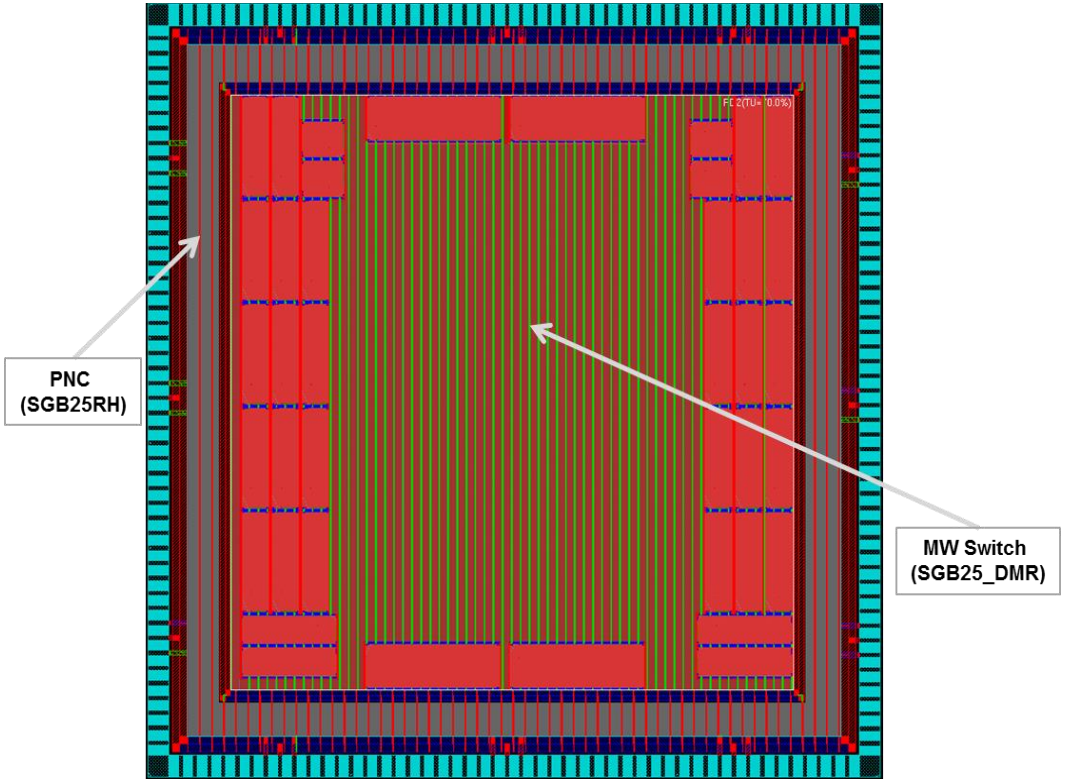




Spacecraft Area Network



Middleware Switch with DMR and SPS



Thank you for your attention!

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