ASICs for Space: Design Examples

Virtual ELICSIR Summer School
“Radiation Effects in Electronic Devices, Circuits and Systems”

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IHP – Leibniz-Institut für innovative Mikroelektronik

Outline

Receiver/Trasnsmitter ICs for intra-satellite optical links

- Developed within a research project
- Goal: investigate a way of increasing the raw datarate in the intra-satellite optical link from 12.5 Gbps (SES17) to 25 Gbps
- Potential application

SES17 developed by TAS

Parameter	Value
Power consumption	15 kW
Weight	6 000 kg
Lifetime	15 years
Orbit	GEO

Motivation

- Growing demand for high data throughput
  - Multimedia services (HDTV, video on demand, etc.)
- Space-based internet approach
  - OneWeb, Starlink, O3b, etc.
- Complex multi-beam antennas
  - Hundreds channels to receive, route, and transmit
- Large size and electrical power consumption of existing satellites

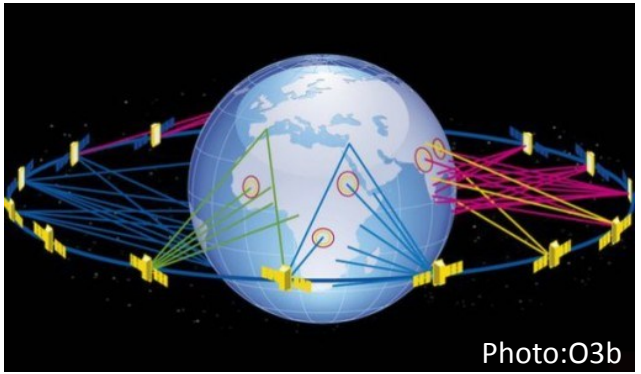


Photo:O3b

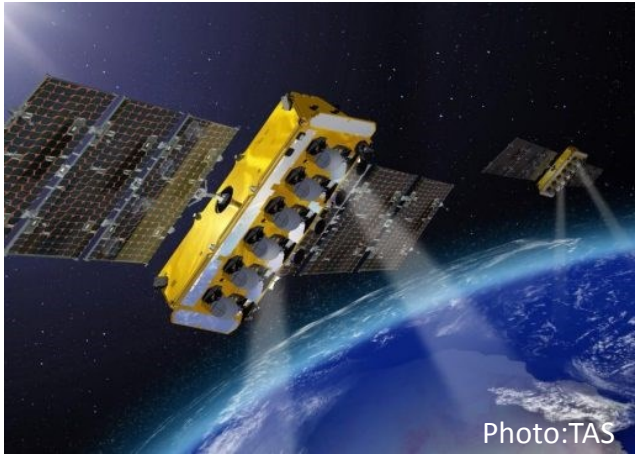
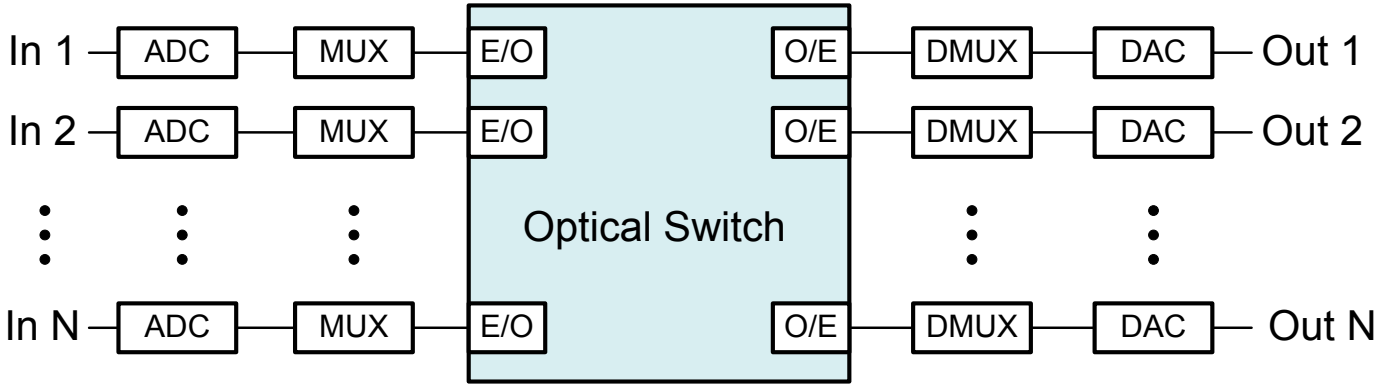


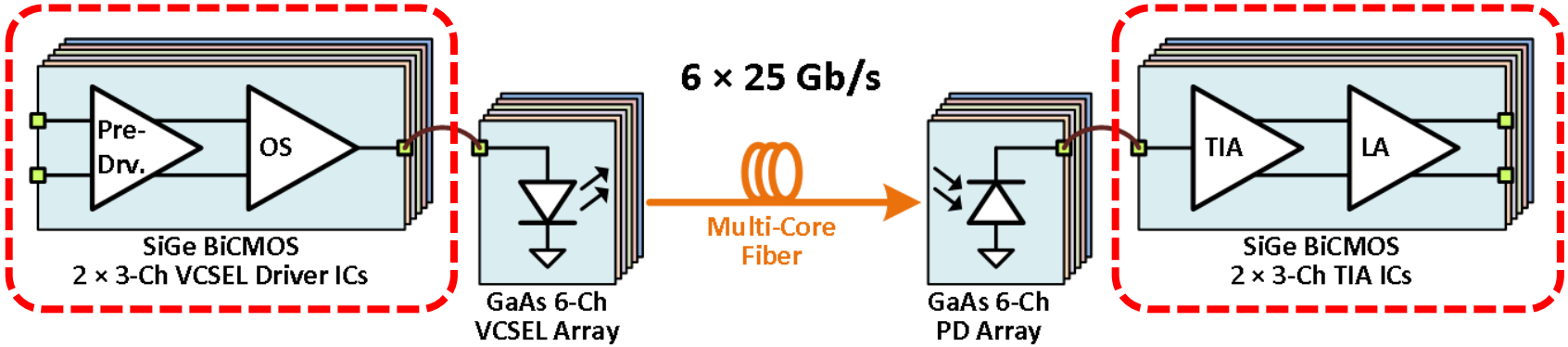
Photo:TAS

Requirements to optical transceiver for satellite interconnect



- Board capacity 150 – 200 links (3 GHz bandwidth per link)
- Data rates: 6 Gb/s – 25 Gb/s per link
- Total throughput 10 Tb/s

150 Gb/s optoelectronic module requirements

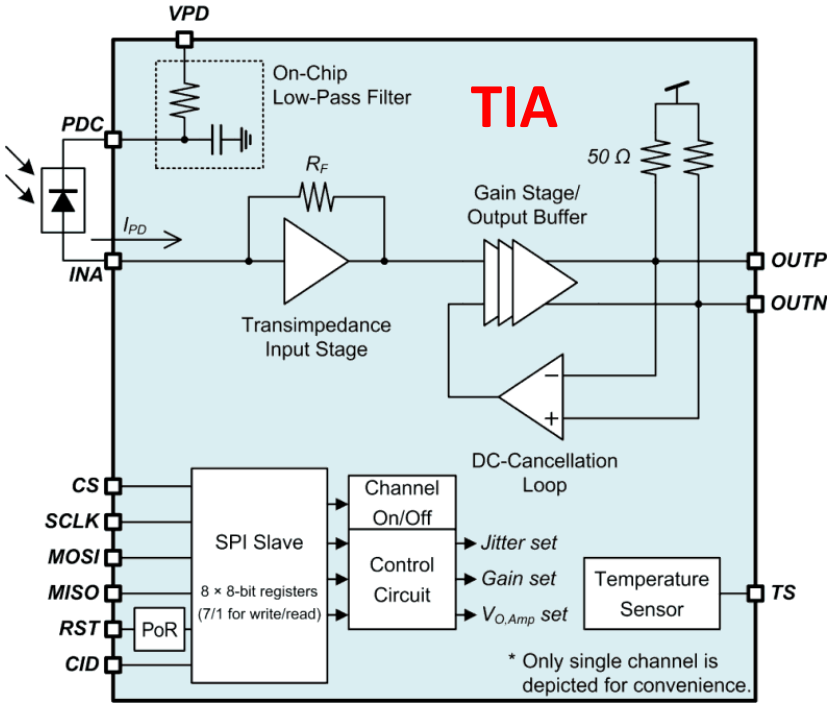


Key Requirements for ASICs – VCSEL Driver and Transimpedance Amplifier. (TIA)

- Number of Channels: 3
- Data rate: 25 Gb/s per channel
- Power consumption: <120 mW per channel (Tx + Rx) → 4.8 mW/Gb/s
- Operating temperature: −40 to +85 °C (100°C as a goal)
- Digital control and monitoring via serial interface

Transimpedance Amplifier Architecture

- 3-channel IC
  - npn-HBTs with f_T/f_{max} = 190/220 GHz
- High speed: 25 Gb/s error free
- Low power: 67.1 mW/channel
- Digital control
  - Noise, gain, output swing
- Wide temperature range till 120°C



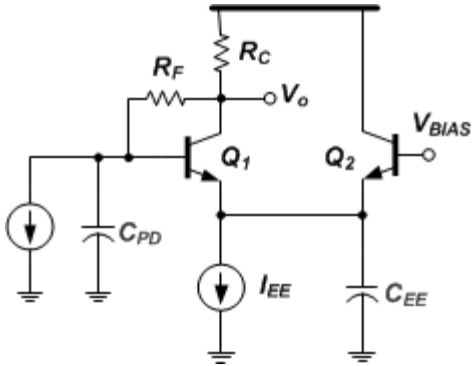
Transimpedance Amplifier Input Stage

- Maximize the bandwidth
  - Minimize the input RC
- Voltage-current feedback
  - Input impedance reduction
- Low noise
- Approximately 50% less power consumption than its differential counterpart
- Noise-bandwidth compromise

Input resistance

$$R_{IN} = \frac{R_F}{1 + g_{m1} R_C}$$

TIA input stage



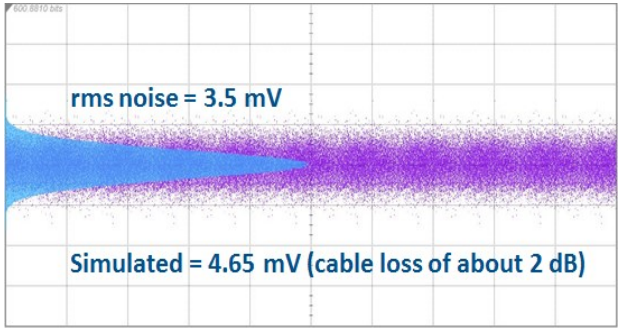
Transimpedance

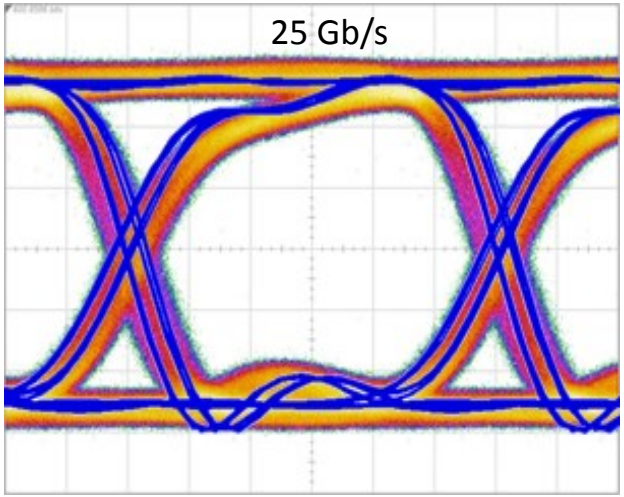
$$G = \frac{g_{m1} R_C R_F}{1 + g_{m1} R_C}$$

- B. Sedighi and J. C. Scheytt, “Low-power SiGe BiCMOS transimpedance amplifier for 25-GBaud optical links,” Aug. 2012.

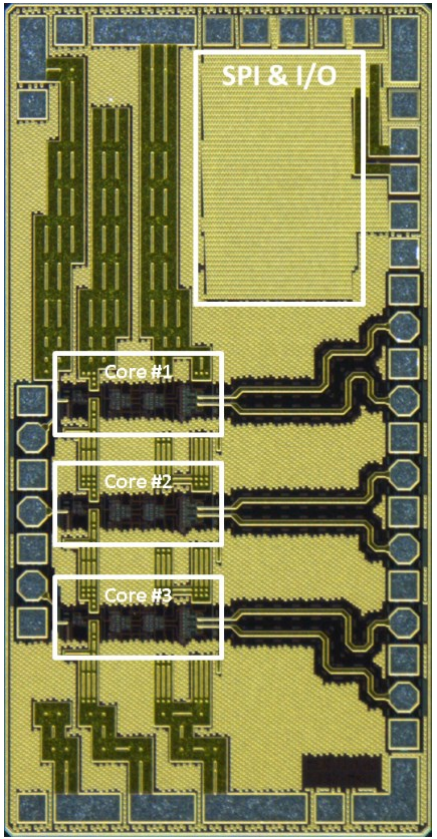
TIA Measurement Results

- Maximum data rate 25 Gb/s
- 3-dB bandwidth 18 GHz
- 67.1 mW/channel
- Chip size 1.3 x 2.4 mm^2



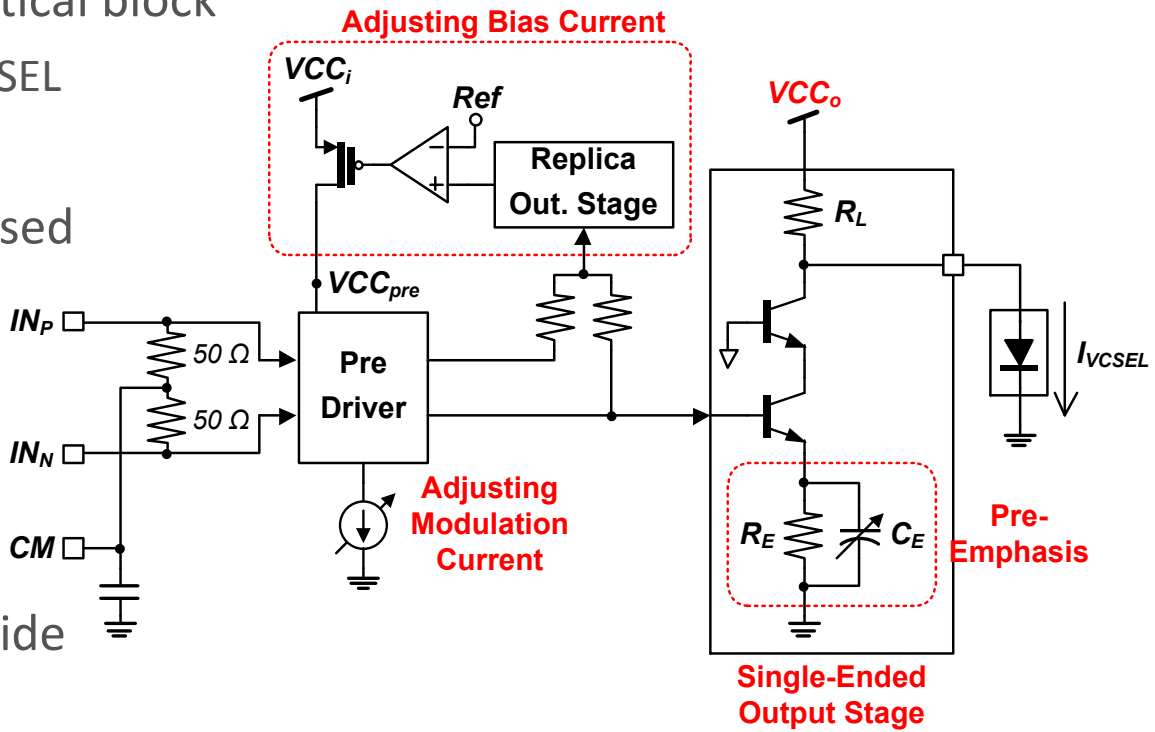


Gen-2



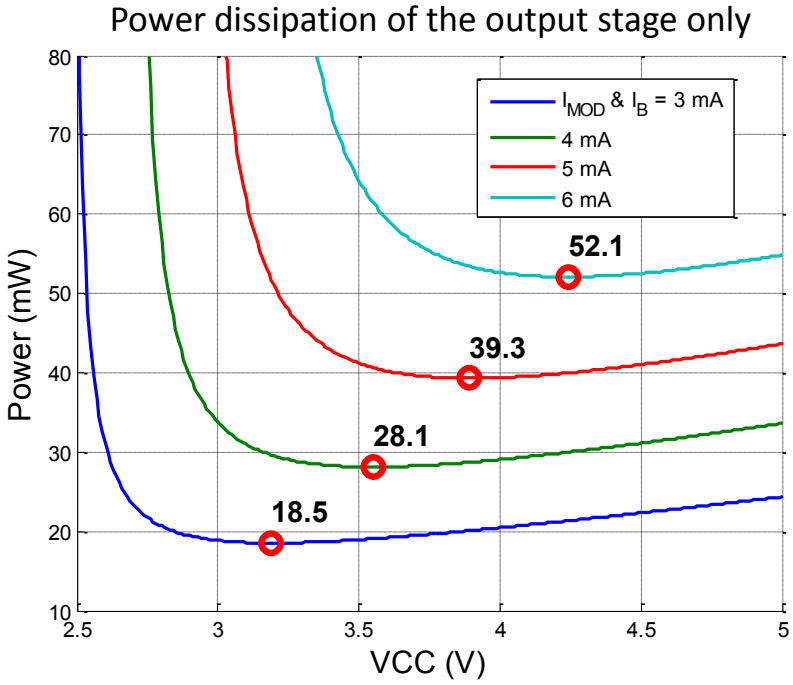
VCSEL Driver Circuit Design for Low Power

- Output stage is the most critical block
  - Driving high current into VCSEL
- Single-ended architecture used
  - Saves up to 50% of power consumption compared to the differential structure
- Feedback loop using the output stage replica to provide stable biasing



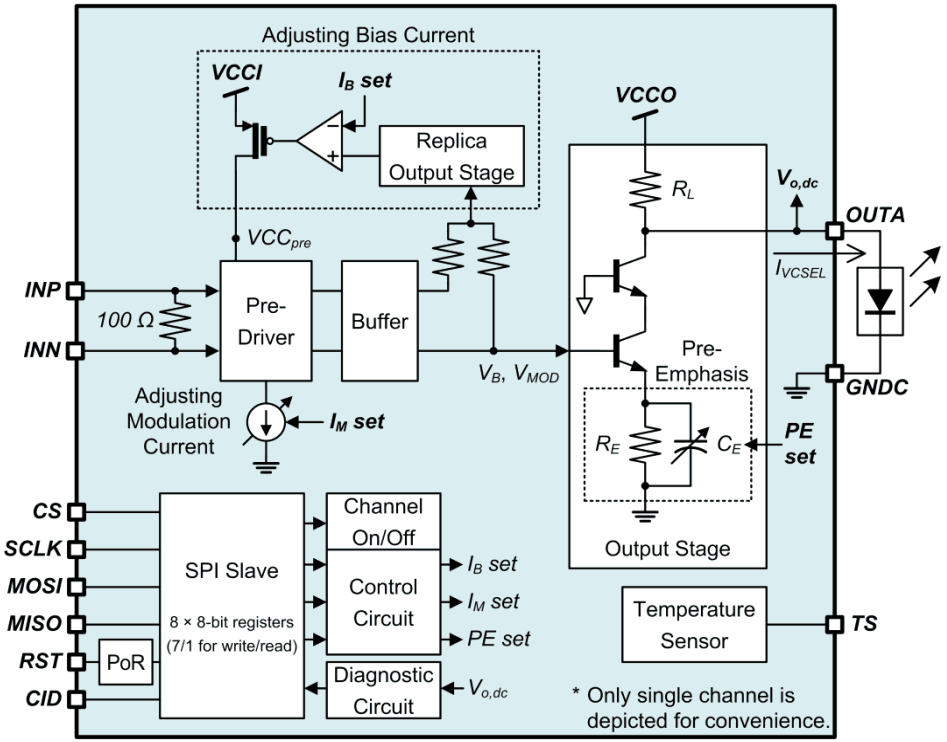
VCSEL Driver Circuit Design for Low Power

- I_{MOD} and I_B should be low to meet the power dissipation requirement (< 55 mW/Ch)
- Driver is optimized for $I_{B/MOD}$ = 3 mA / 3 mA_{pp}
- Driving capability up to $I_{B/MOD}$ = 4 mA / 4 mA_{pp}
  - Needed at high temperature
- VCSEL driver I_{MAX} = 7 mA



VCSEL Driver Circuit Design

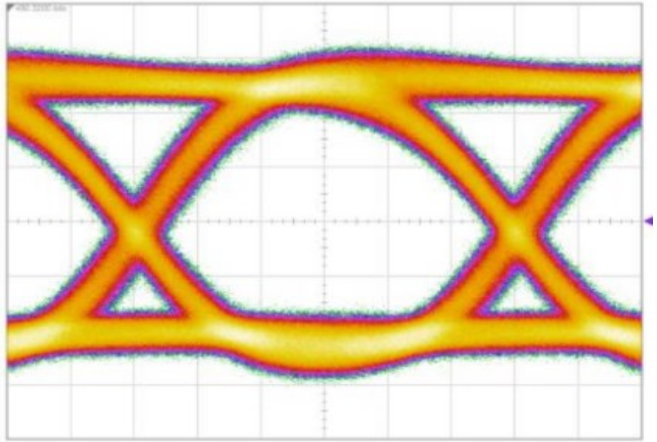
- 3-channel IC
- High speed: 40 Gb/s error free
- Low power: 42.5 mW/channel
- Digital control
  - VCSEL currents $I_{B/MOD}$
  - Bandwidth adjustment
- Wide temperature range till 120°C



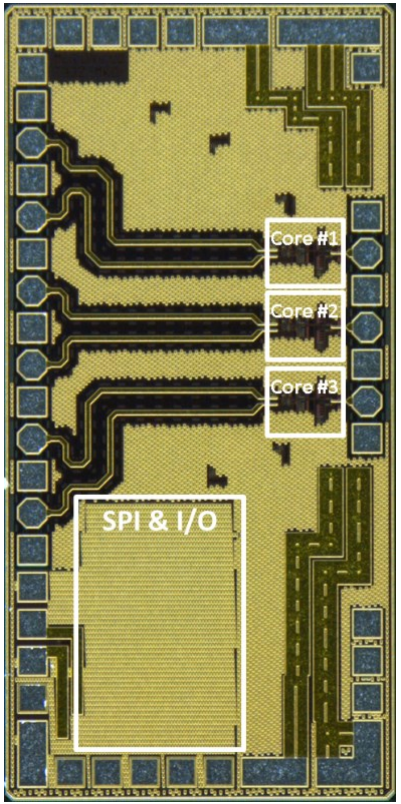
VCSEL Driver Measurement Results

- 3-dB bandwidth 29 GHz
- Maximum data rate 40 Gb/s
- 42.5 mW/channel
- Chip size 1.2 x 2.3 mm²

40 Gb/s

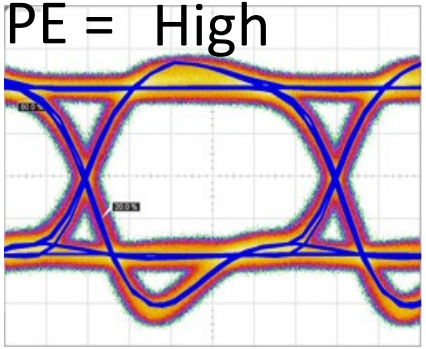


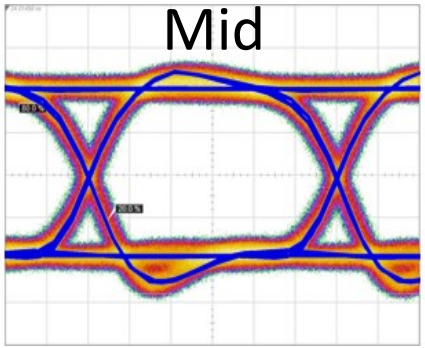
Gen-2

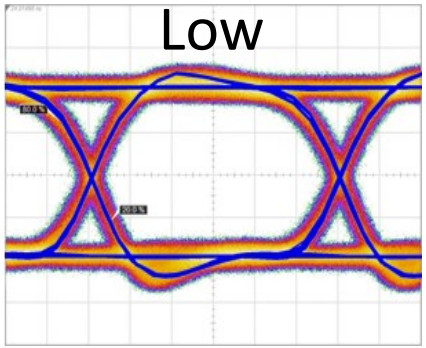


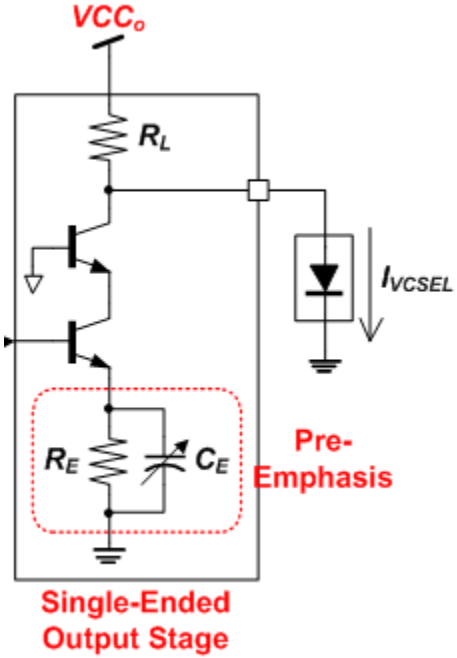
VCSEL Driver Pre-Emphasis

- 3-bit pre-emphasis control
- C_E adjustment in the range from 200 fF to 600 fF
- Bandwidth extension from 21 GHz to 29 GHz



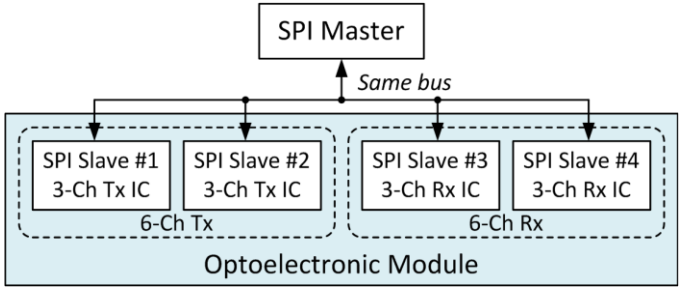






* Blue lines: simulated results

Digital Control Interface

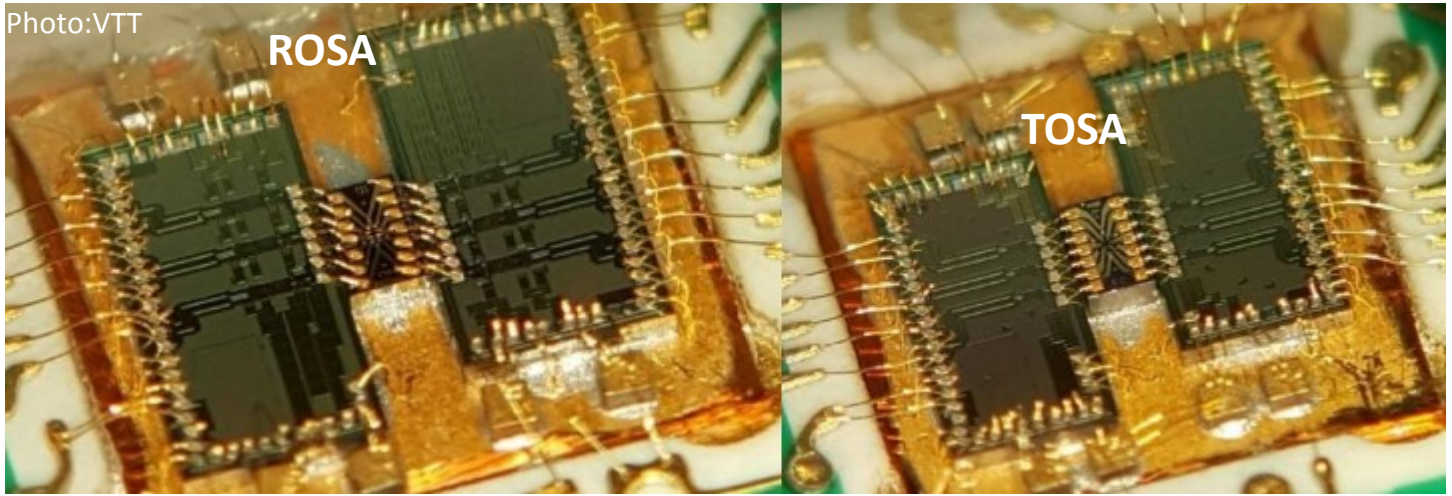


Channel-independent digital control via SPI

- Power-on-reset (PoR) circuit for autonomous start-up
- Non-zero preset value for each control register

Tx/Rx	Control	Bits per Channel	Note
Common	Channel ON/OFF	1	
Tx	VCSEL bias current	4	0 – 5 mA
	VCSEL mod. Current	4	0 – 5 mA_{pp}
	Pre-emphasis	3	
Rx	Jitter	4	
	Gain	4	4kΩ – 13 kΩ
	Output amplitude	4	0 – 750 mV_{ppd}

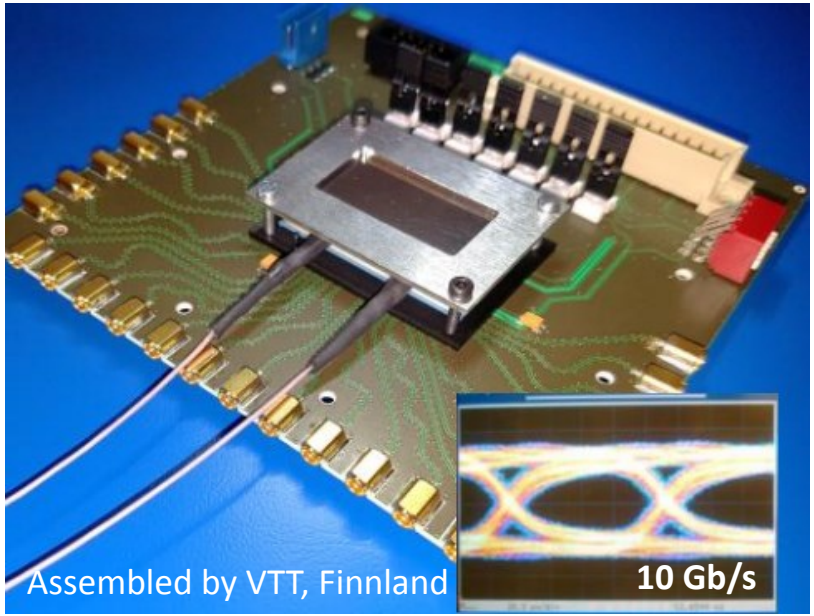
Total Power Consumption

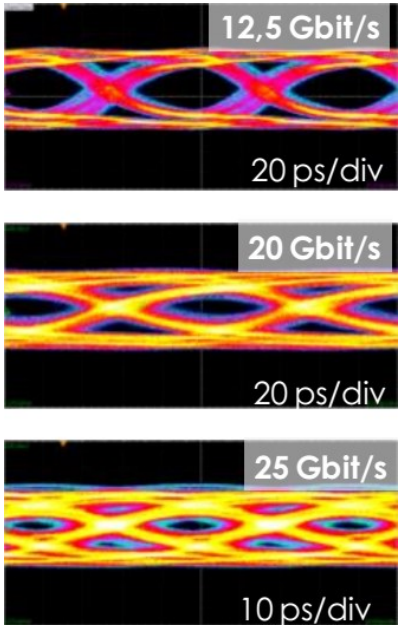


Channel state	Measured TX	Measured RX	Measured Total	Target Total
ON	42.5 mW	67.1 mW	109.6 mW	< 120 mW
OFF	0.9 mW	4.2 mW	5.1 mW	< 10 mW

Multicore Transceiver Module Back-to-back Characterization

- 6-core optic fiber cables
- Data link through 2 MCF fanouts
- 10^{-9} BER at 20 Gb/s
- Error free transmission till 17.5 Gb/s



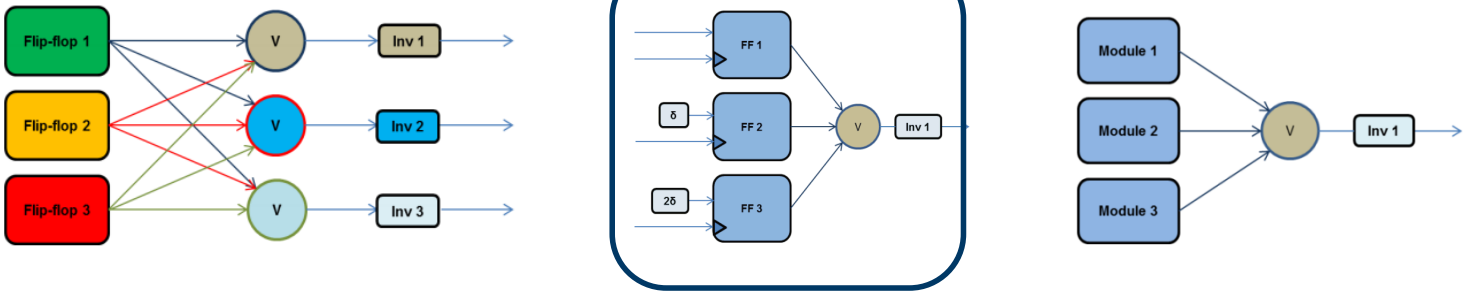


- *L. Stampoulidis, E. Kehayas, M. Karppinen, A. Tanskanen et al., "High-speed, low-power and board-mountable optical transceivers for scalable & energy efficient on-board digital transparent processors," in Proc. International Conference on Space Optics (ICSO), 2018.*

Radiation hardening

- Triple Modular Redundancy flip-flops (TMR-FF) approach to mitigate SEU

- Proven RH design for the SPI interface
  - Based on SGB25RH standard cells and IO library
  - TMR flip-flop are used in SPI core

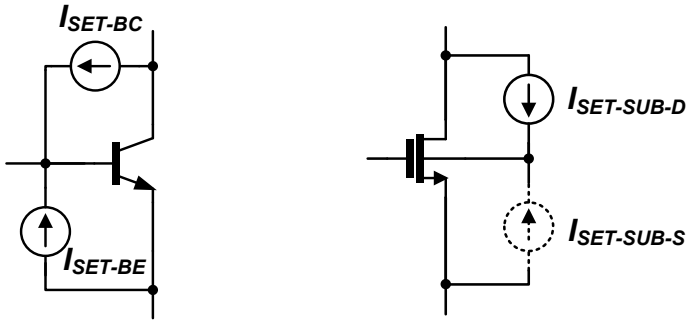


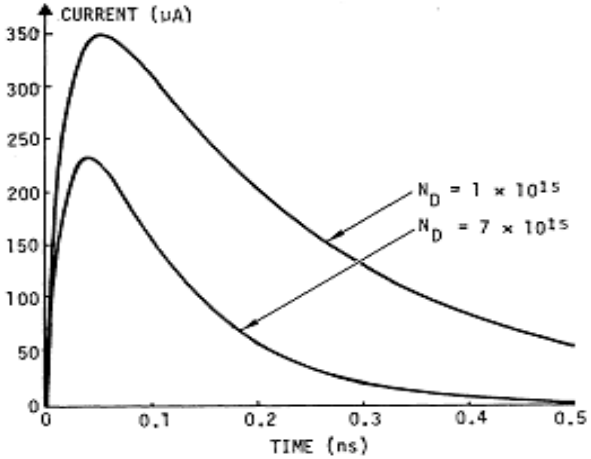
- Sufficient resistance against ionizing radiation
  - 100 kRad for satellites

Ion-strike modeling

- By double exponenntial current source
- τ_1 - determined by technology; $\tau_2 = 4\tau_1$
- τ_1 = 2.5 ps τ_2= 10 ps used in simulation
- Current source is placed between p-n junctions

$$I_{SET} = I_0(e^{-t/\tau_1} - e^{-t/\tau_2}) \qquad I_0 = \frac{Q}{\tau_1 - \tau_2}$$

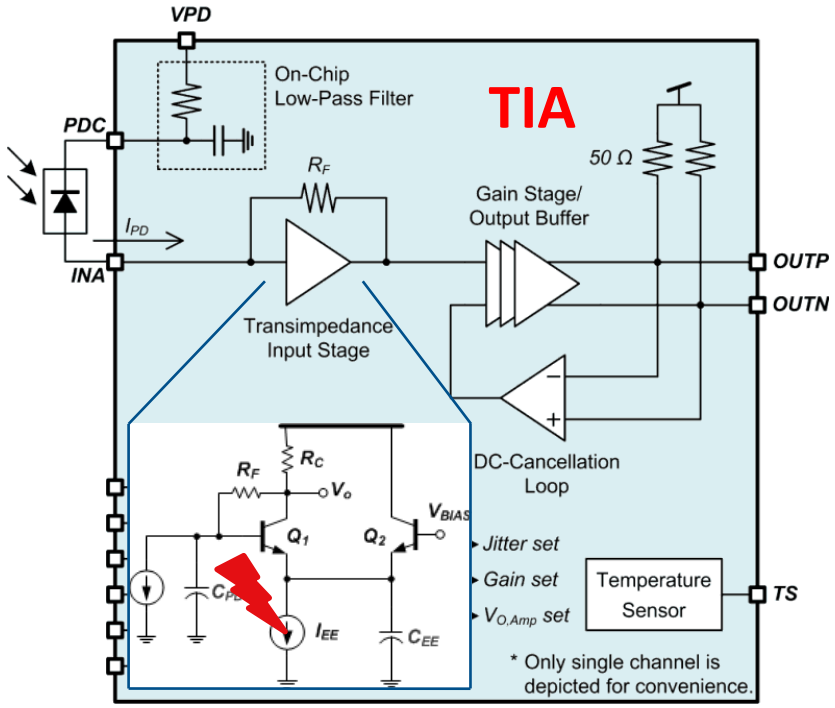




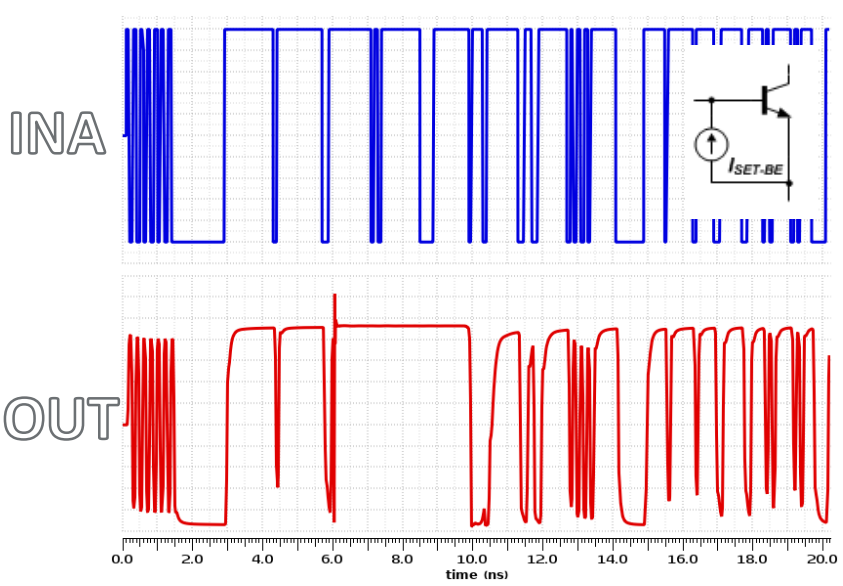
- Disadvantage: in case of high charge unphysical behaviour might be observed
- Solution: use another model
  - *M. Andjelkovic, A. Ilic, Z. Stamenkovic, M. Krstic et al., "An overview of the modeling and simulation of the single event transients at the circuit level," in Proc. IEEE 30th Int. Conf. Microelectronics (MIEL), 2017*

TIA: 2 pC ion strike on current source of the input stage

- Single-ended input stage



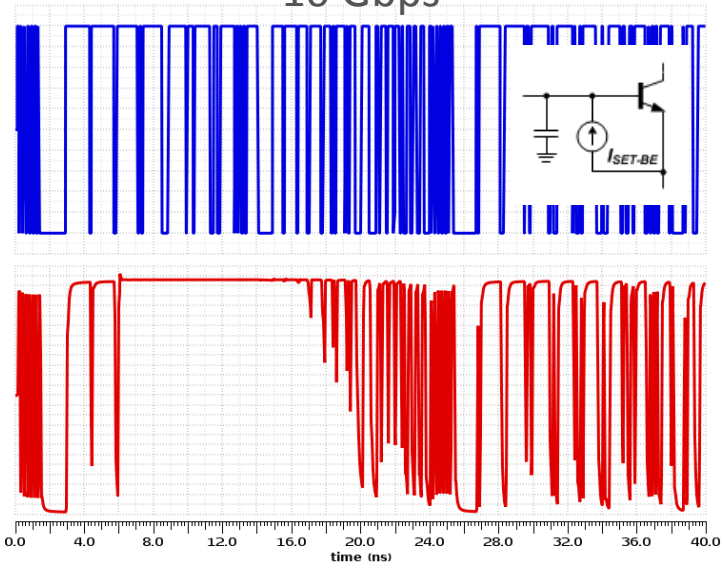
- No capacitance to gnd
- 4 ns corrupted -> 40 bits lost



TIA: 2 pC ion strike on current source of the input stage

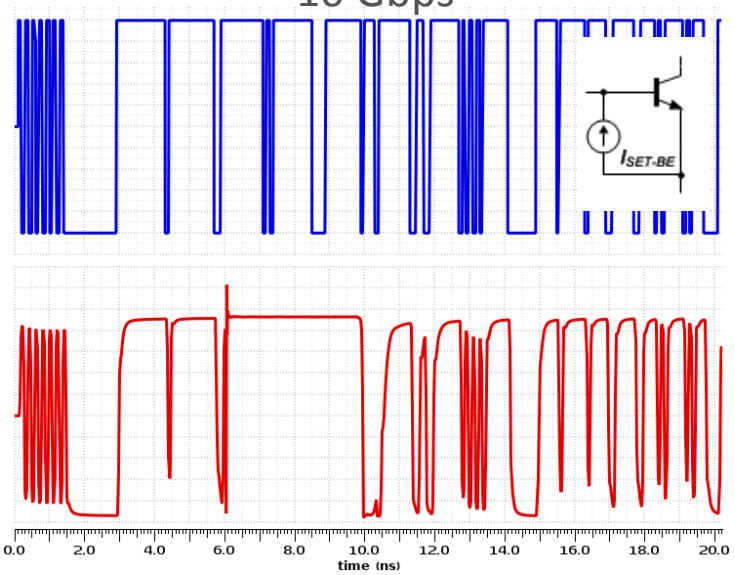
- Single-ended input stage
- 6 pF capacitance at the hit node to gnd
- 14ns corrupted -> 1400 bits lost

10 Gbps



- No capacitance to gnd
- 4 ns corrupted -> 40 bits lost

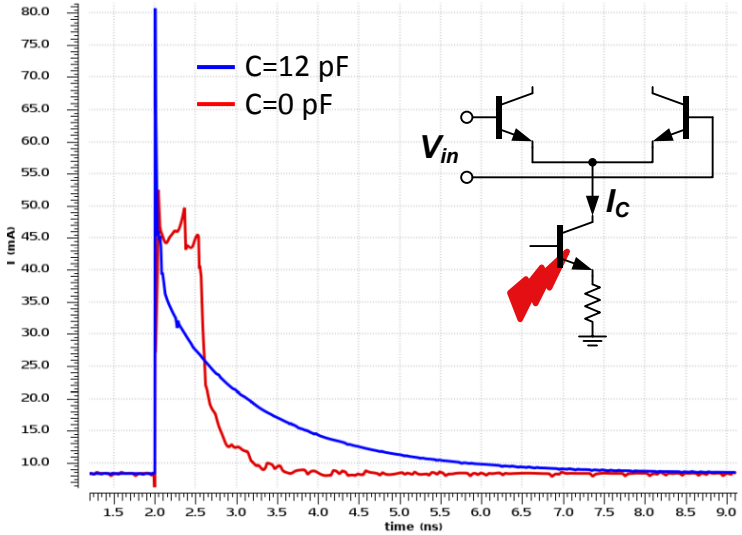
10 Gbps



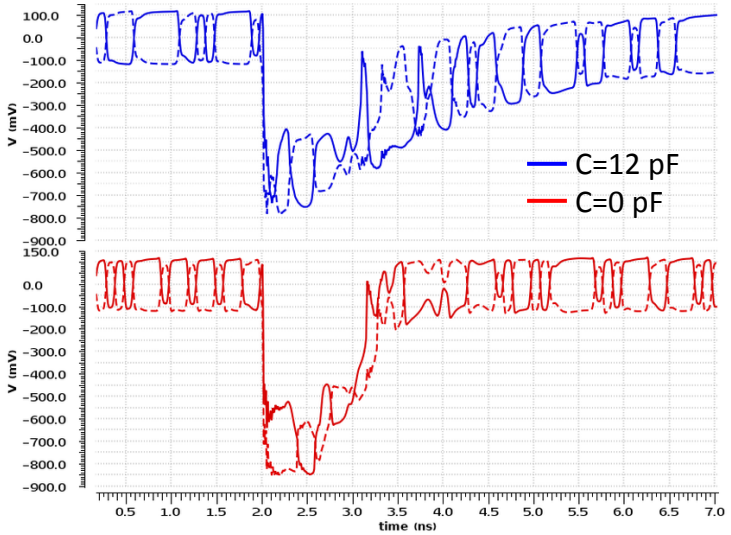
TIA: 2 pC ion strike on current source of the output stage

- Differential output 50-Ohm buffer with and without capacitance at the hit node to gnd
- Recovery time is nearly the same (2ns)

Collector current of the affected transistor

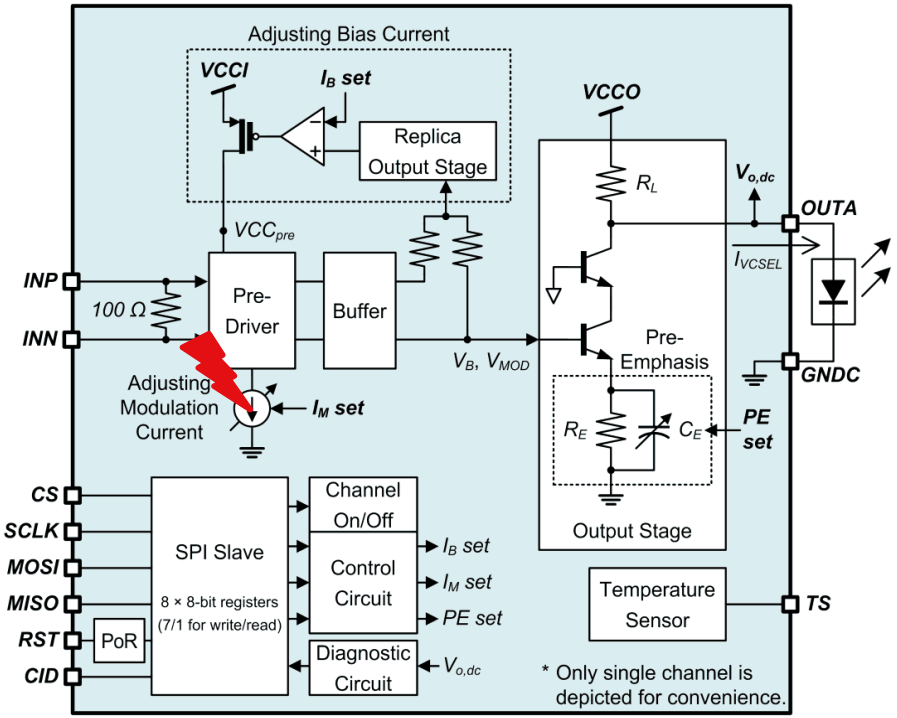


Single-ended TIA outputs

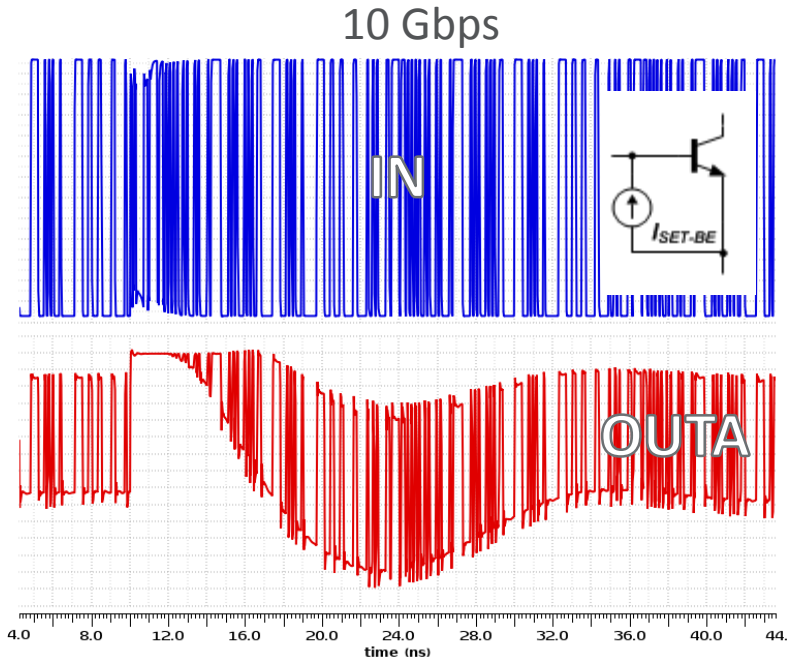


VCSEL-DRV: 2 pC ion strike on current source of the input stage

- Differential input stage / single-ended output stage



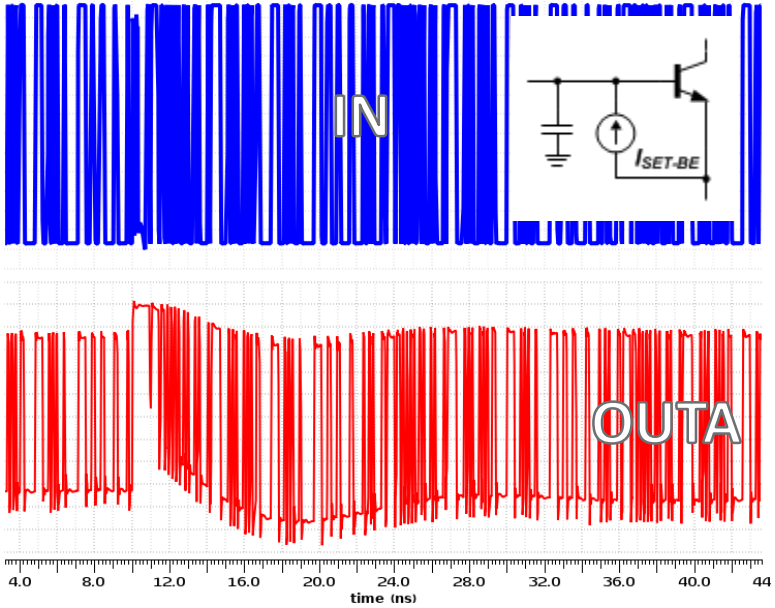
- No capacitance at the hit node to gnd



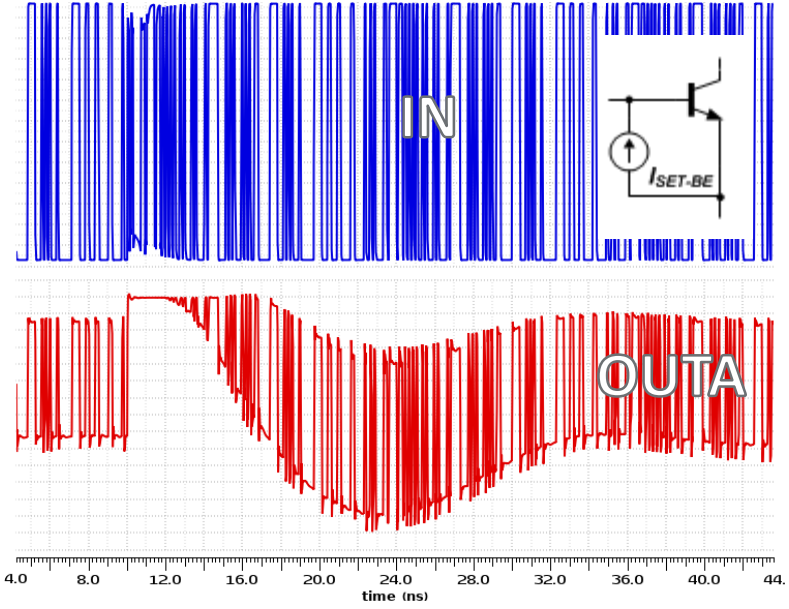
VCSEL-DRV: 2 pC ion strike on current source of the input stage

- Differential input stage / single-ended output stage
- 40 pF capacitance at the hit node to gnd
- No capacitance to gnd

10 Gbps

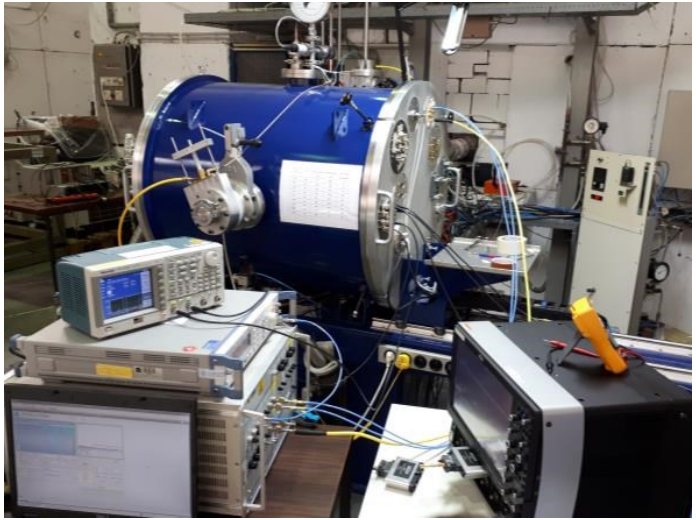


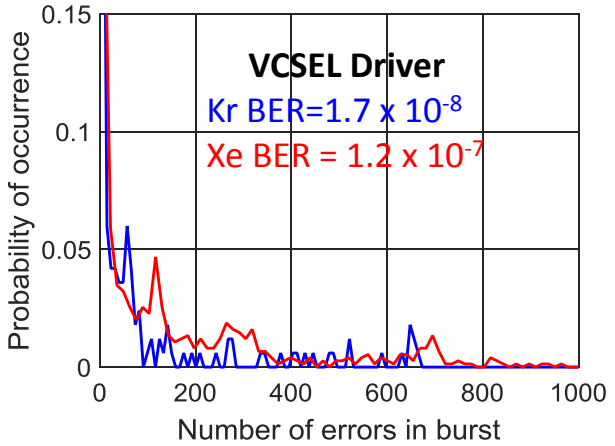
10 Gbps

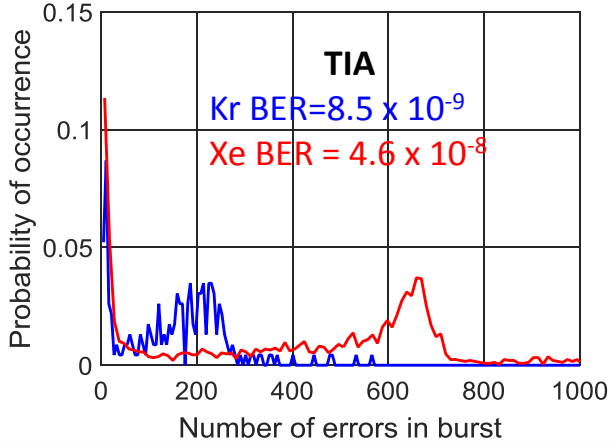


Heavy Ion Test

- BER measurements at 25 Gb/s for both ICs
- Irradiation with ion flux of 5000 particles per second
  - Kr ions LET= 32.4 MeV·cm²/mg
  - Xe ions LET = 62.5 MeV·cm²/mg
- No SEL (latch-up) detected



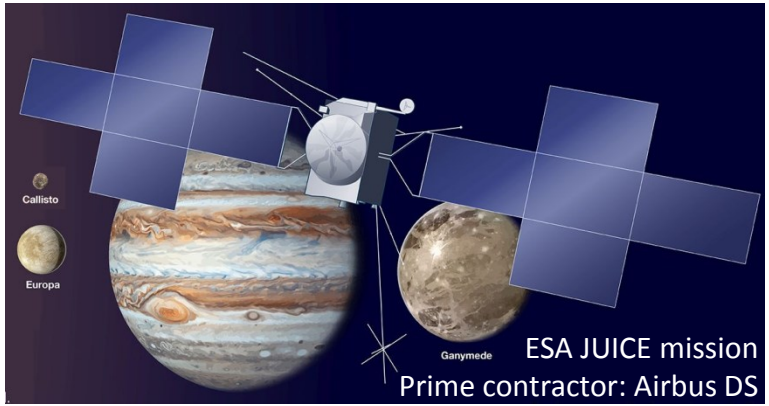




Intermediate Summary

- Higher data throughput requires more channels
- Optimization of power dissipation within a channel is of high importance for space applications
- Optical interconnect system for intra-satellite communication presented
- Low power 3-channel VCSEL driver and TIA ICs shown
- SET influence on analog circuits should be analyzed individually
- Single-ended circuits are more susceptible to ASETs than the balanced ones

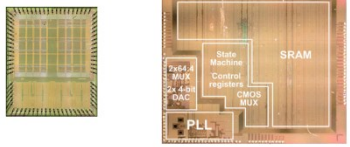
Chirp-Transform Spectrometer ASICs for a mission to Jupiters Moons



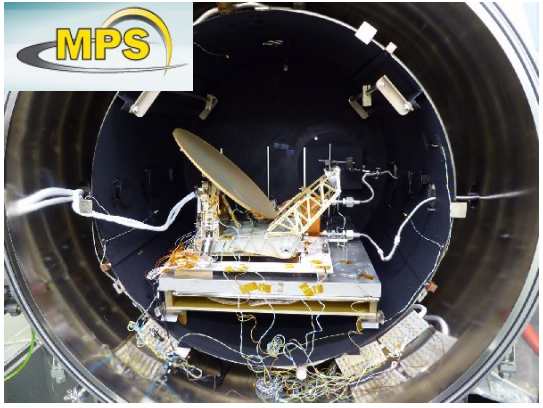
ESA JUICE mission
Prime contractor: Airbus DS

Parameter	Value
Power consumption	4 kW
Weight	5 300 kg
Lifetime	3.5 years
Orbit	Jupiter, Ganymede

ASICs for Chirp-Transform Spectrometer



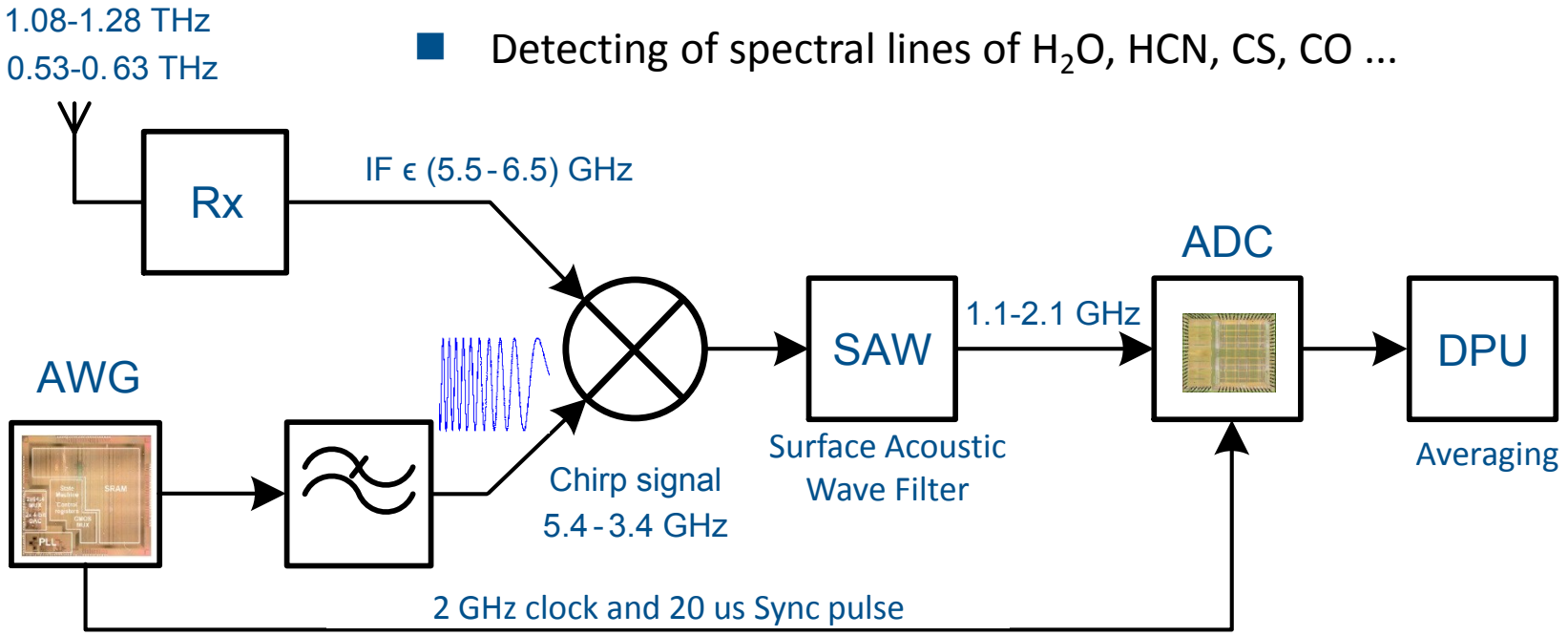
- Design two complex rad-hard ASICs
  - 2-channel Arbitrary Waveform Generator
  - 2- channel Pre-Processor



- Chirp Transform Spectrometer
  - Dual band: 530-625 GHz and 1.08-1.275 THz
  - Max Planck Institute for Solar System Research

- **Ju**piter **Ic**y Moons **E**xplorer mission (JUICE)
  - ESA
  - Launch in 2022 -> Arrival to Jupiter 2030

Chirp-Transform Spectrometer Architecture

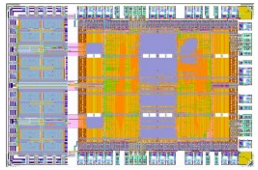


- G. L. Villanueva, P. Hartogh, and L. M. Reindl, "A digital dispersive matching network for SAW devices in chirp transform spectrometers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 4, pp. 1415–1424, Jun. 2006.

ASICs overview

Pre-Processor (65 nm)

- Developed using ST microelectronics C65Space PDK
- 2-channel 8-bit ADC
- 2 x 508 kbit SRAM

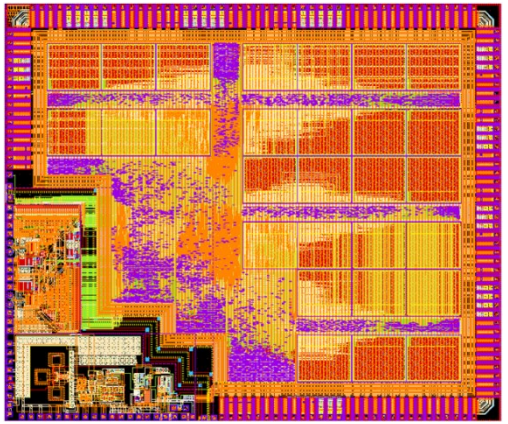


2.1 mm

3.3 mm

Chirp Generator (130 nm)

- IHP 0.13µm SiGe BiCMOS technology
- 2-channel 4-bit AWG including 4-bit 16 GSps DACs
- 2 x 1.6 Mbit SRAM



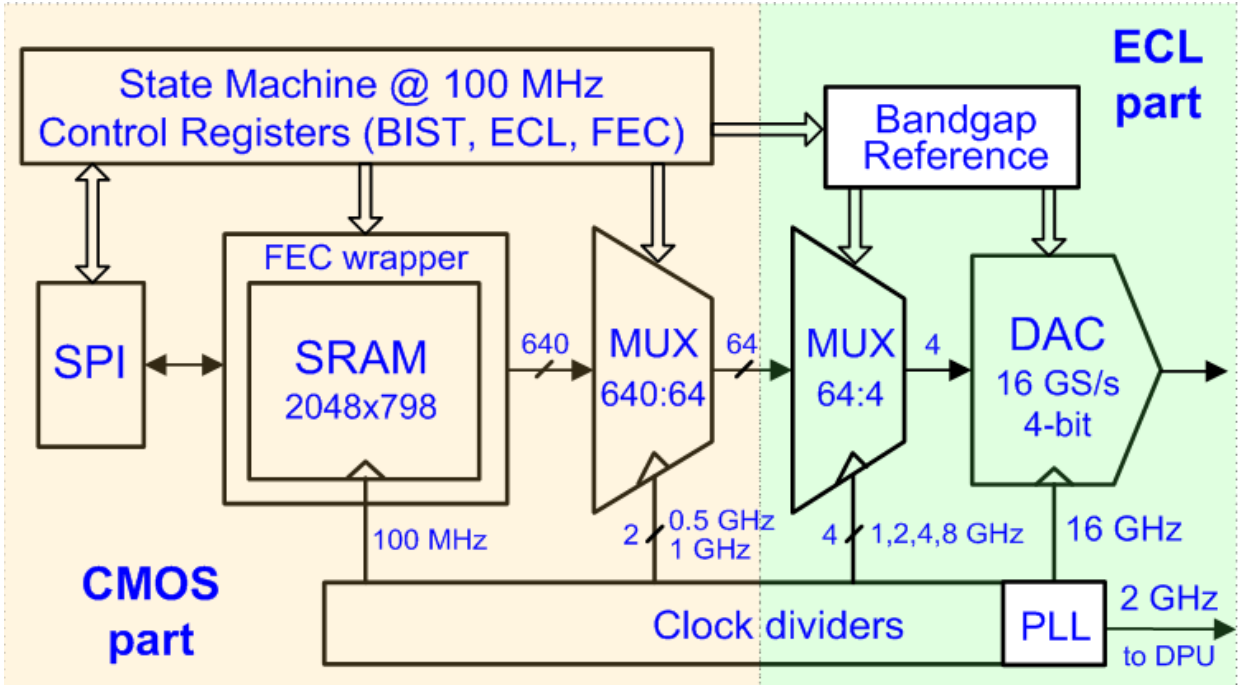
5.7 mm

6.6 mm

Why SiGe BiCMOS?

- SiGe HBTs are inherently radiation-hard w.r.t. gamma-rays, neutrons and protons
  - required total-ionizing dose is 300 kRad
- SiGe frequency synthesizer delivers better phase noise than CMOS counterpart
  - low clock jitter is important for high-speed data converters
- Less power consumption for high speed broadband signals
  - Current-mode logic

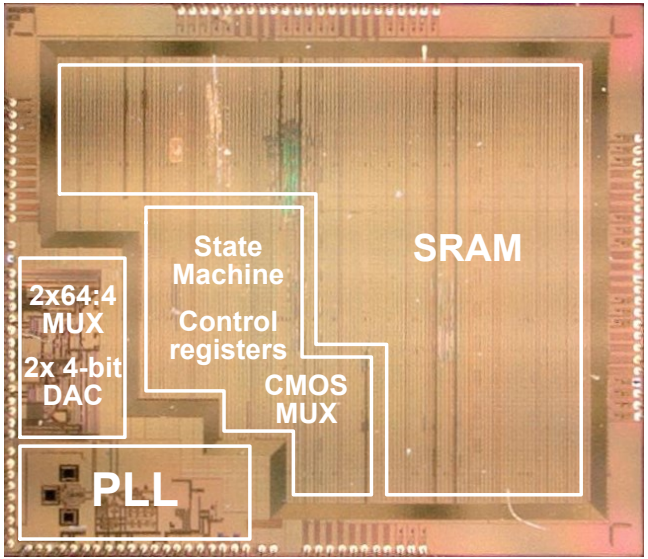
AWG architecture



- *P. Ostrovsky, O. Schrape, K. Tittelbach-Helmrich, F. Herzel et al., "A Radiation Hardened 16 GS/s Arbitrary Waveform Generator IC for a Submillimeter Wave Chirp-Transform Spectrometer," in Proc. IEEE Nordic Circ. and Syst. Conf. (NORCAS), Oct. 2018.*

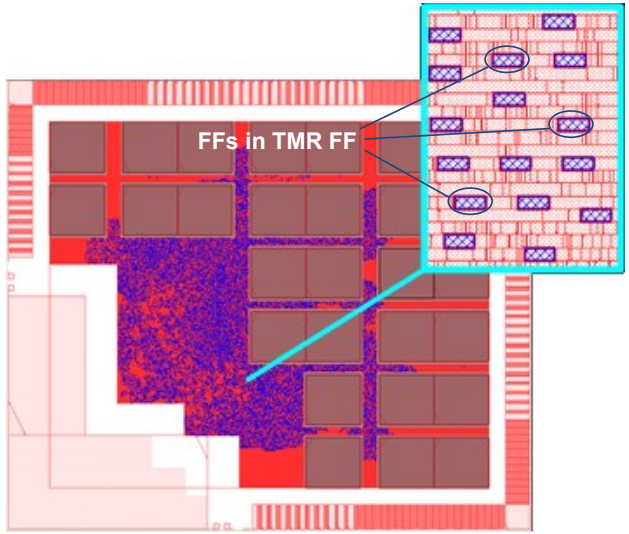
Radiation hardening considerations

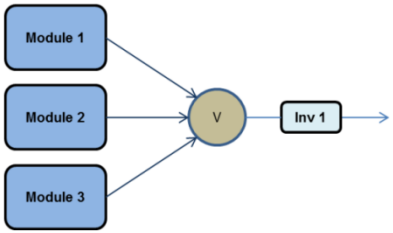
- SRAM
  - No rad-hard SRAM structures available
  - High component density -> SEL and SEU sensitive
- State machine, control register, CMOS MUX
  - SEU sensitive
- IO cells
  - TID sensitive HV NMOS transistors
- PLL, MUX, DAC
  - HBT based circuits -> tolerant to ~1 Mrad of TID
  - Differential ECL logic -> no radiation hardening



Digital logic protection

- RH digital library used
- Forward error correction during SRAM read/write
- Separate placement of the FFs in TMR
- Increasing of driving strength
- Simplest TMR structure used because of power consumption limitations

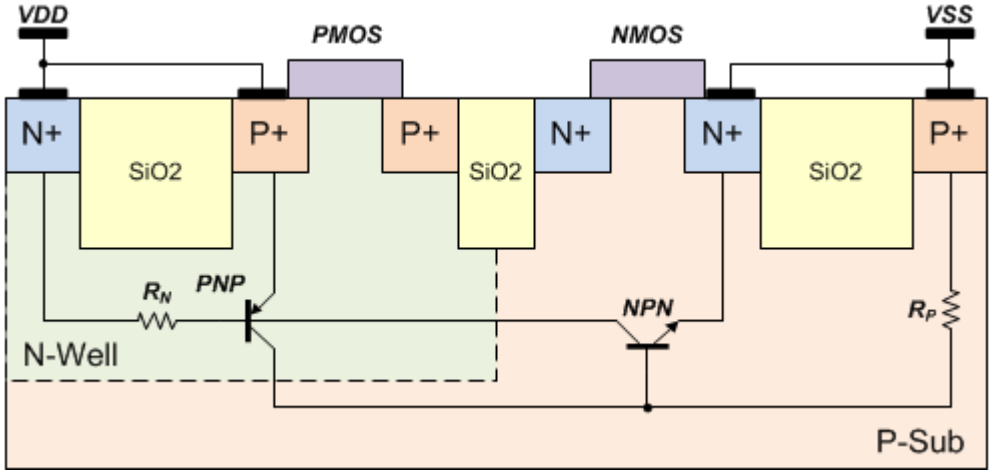




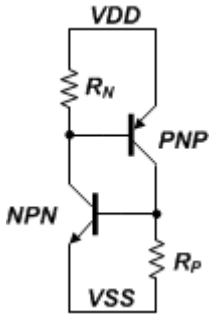
	Non-RH IC	RH IC
Power consumption	1.45 W	3 W
Number of digital cells	~ 57 k	~ 98 k
Number of registers	~ 8 k	~ 22 k

Latch-up effect

- Both parasitic bipolar transistor conducts the current
  - Low resistive path between the power rails
- Gain product of both bipolar transistors more than 1
  - Positive feedback loop

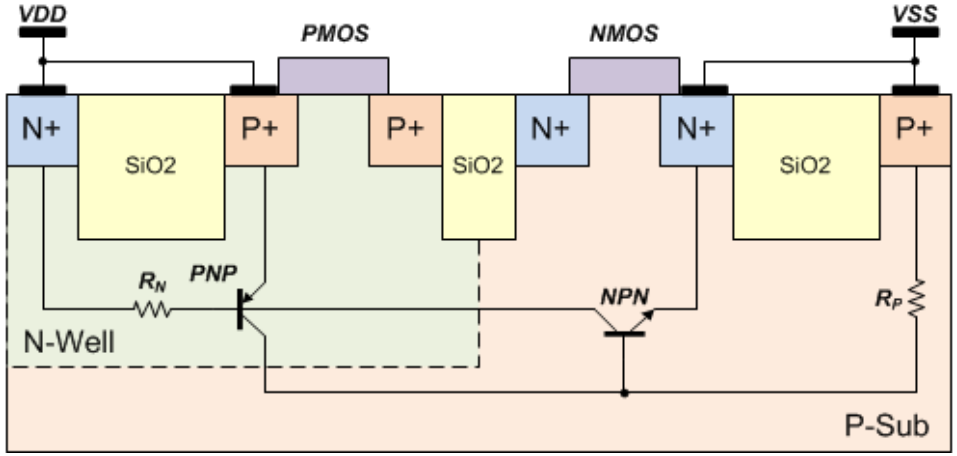


Equivalent circuit



Latch-up effect: possible ways to avoid

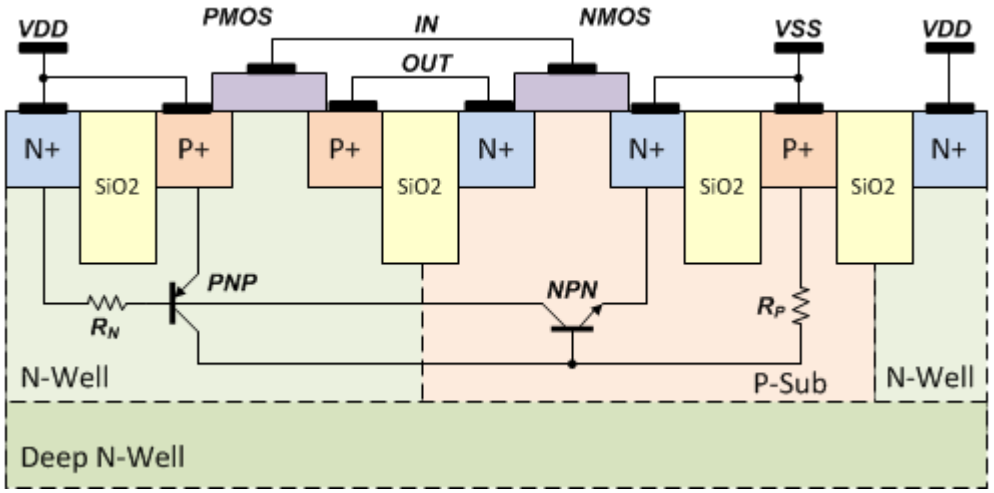
- Decrease gain of parasitic bipolar transistors (↓ β)
  - Increase the base width
  - move NMOS device away from P-Sub-N-Well junction

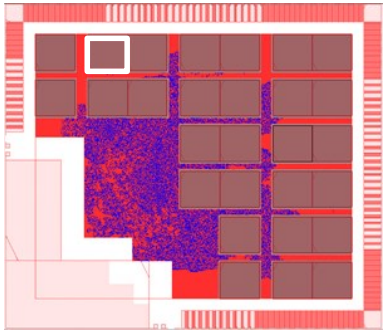


- Bulk/N-Well contacts as close as possible to the source of NMOS/PMOS (↓ R_P and R_N)
- Surround NMOS and PMOS transistors by guard rings (↓ R_P and R_N)
- Surround the structure by Deep N-Well guard rings (↓ R_N ↓β_{PNP})

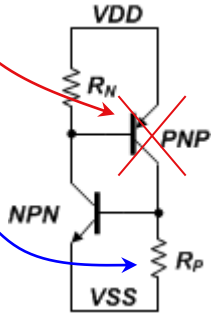
SRAM protection

- Increasing of radiation tolerance in case of an existing SRAM block
  - Deep Nwell areas for each SRAM block
  - Increasing P-Sub contacts density



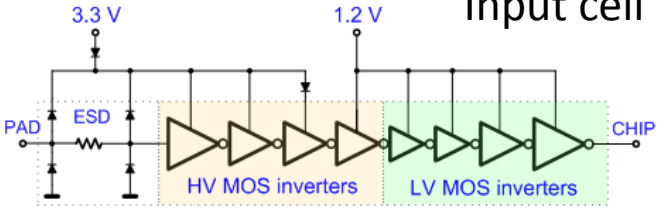


↓R_P



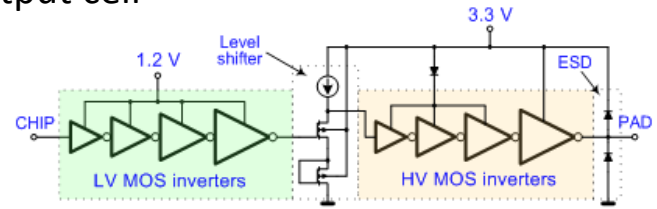
IO Cells

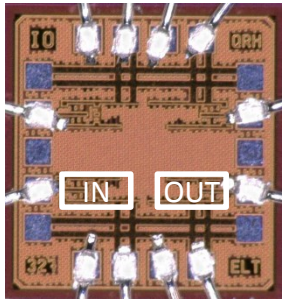
Input cell

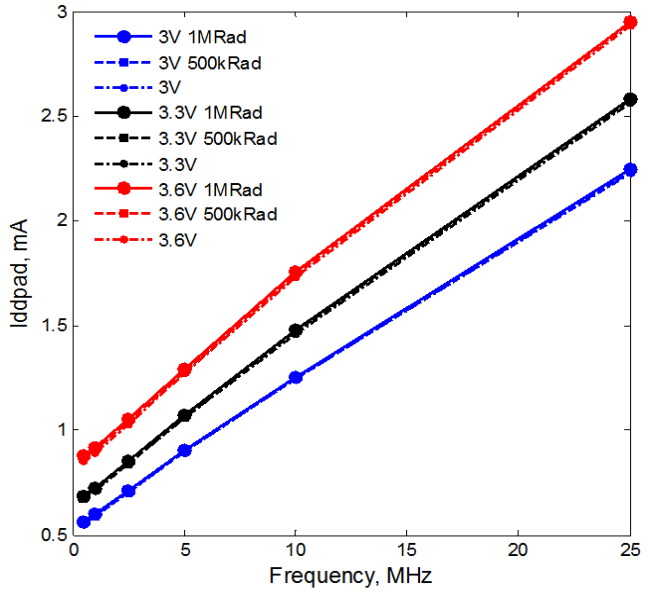


- Back-to-back connection of IO cells
- Irradiated at 500 kRad and 1 MRad

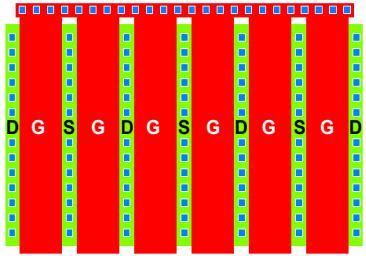
Output cell



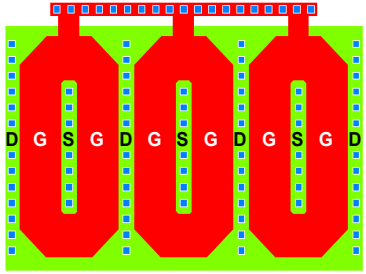




MOS transistor



Enclosed Layout Transistor



Summary

- Chirp-Transform Spectrometer presented
- Selective radiation hardening approach used to optimize power dissipation
- Customized design of the available SRAM block to improve the SEL resistance
- Enclosed Layout Transistors improves TID of the IO cells

Thank you for your attention!

P. Ostrovskyy

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