Design Techniques for Rad-hard ASICs

Virtual Summer School

Radiation Effects in Electronic Devices, Circuits and Systems

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innovations
for high
performance
microelectronics

Projects ELICSIR/ Space Region

Aug 2020

Member of Leibniz Association

Agenda

1. Motivation
2. Radiation Effects
3. Addressing SEEs in Digital Systems
4. Optimizing Overhead in Space Applications
5. Design Examples
6. Conclusions

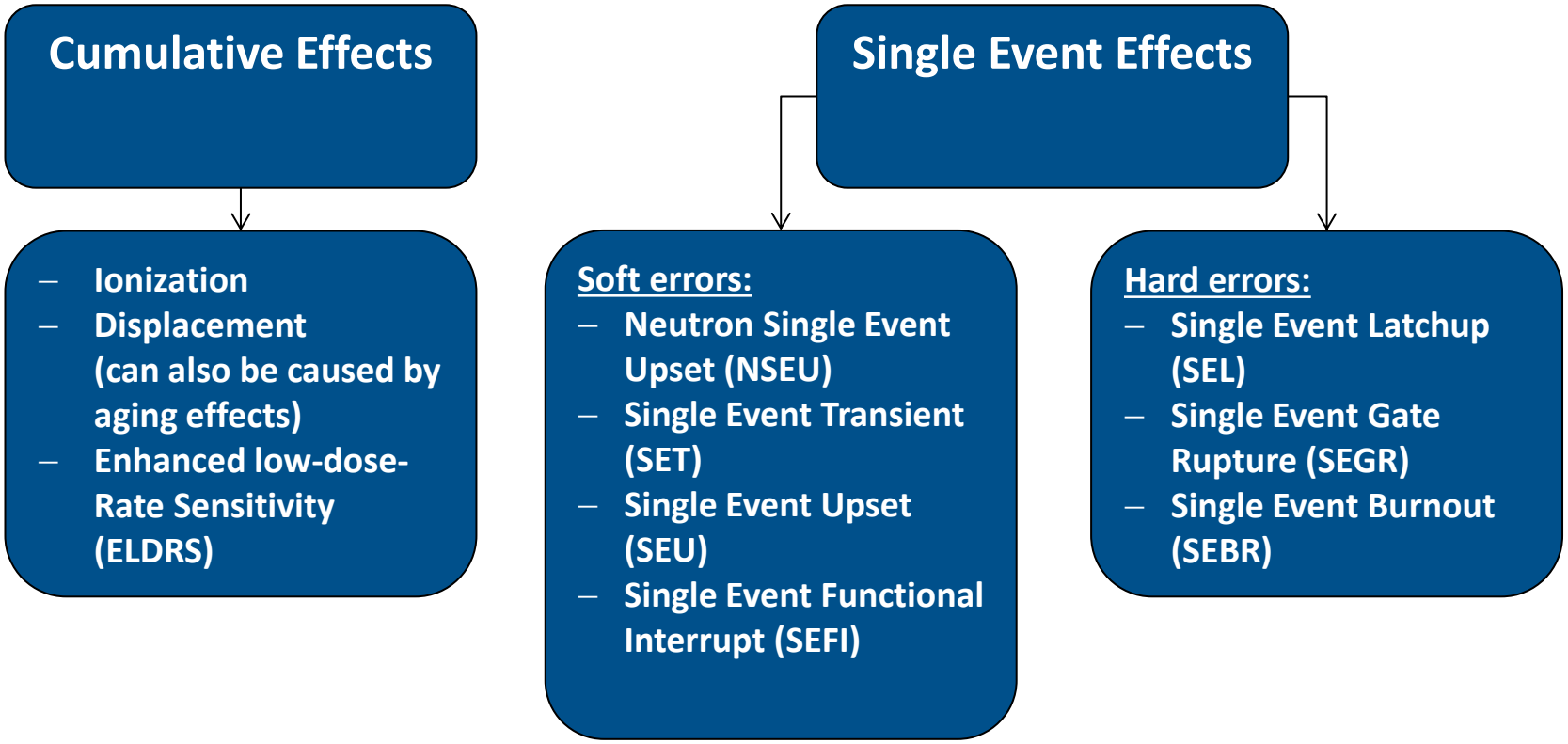
Motivation and goals

- Space applications are imposed with additional requirements, not so critical in traditional application domain
- Temperature: temperature range is extended -55° - +125°
- Reliability: depending on the mission requirements could be even 15 or 20 years
- Radiation hardness and tolerance: immunity against radiation effects
- As a consequence additional design steps are required to fulfil the requirements
- The design methods enhancing radiation hardness are known as radiation hardness by design (RHBD), and are usually based on fault tolerance
  - Fault tolerance is always achieved with some (significant!) cost
- How to limit the overhead imposed by fault tolerance?
  - Advanced static low-overhead techniques which provide certain level of fault tolerance with limited overhead
  - Adaptivity techniques which enable fault tolerance only when required

Effects induced by Radiation

Radiation effects are present not just in space applications

Radiation effects can be split in two general categories:



The effects need to be addressed by corresponding measures

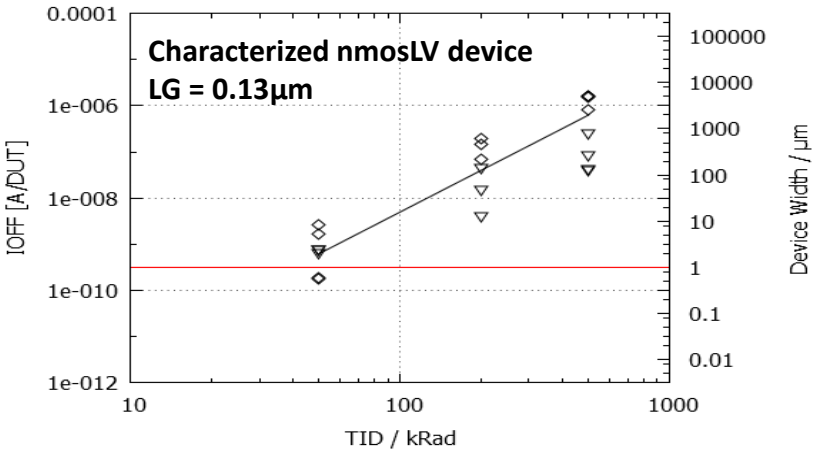
Cumulative Effects and Ways against them

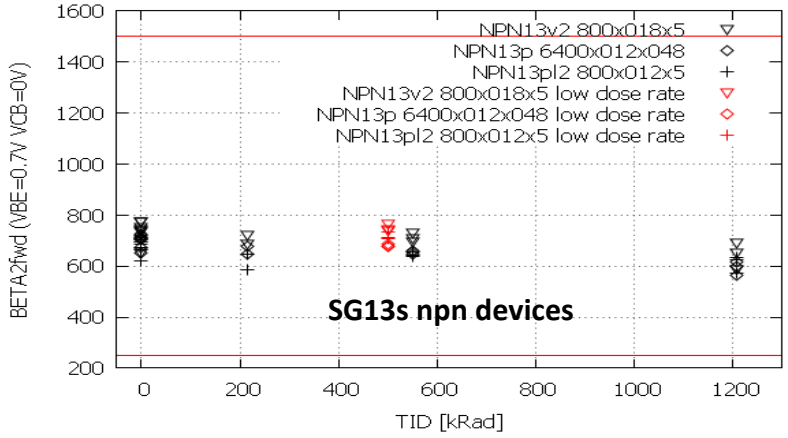
- Cumulative effects affect the parametric changes of the transistors (increase of leakage current, change of threshold voltage, reduction of transistor amplification etc.).
  - After total dose accumulation the system may reach the state outside of the specified functional range.
  - Due to the reduced performance of the transistors the respective faults may appear (timing faults for example)

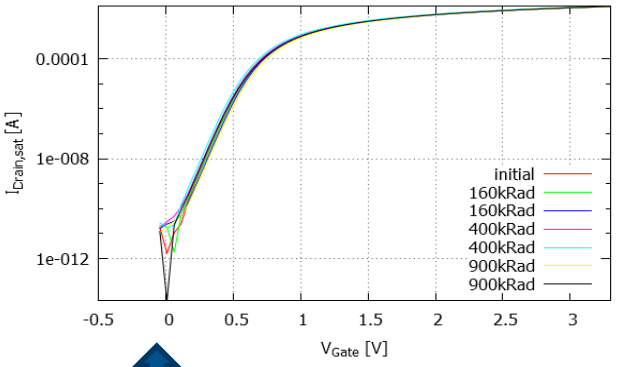
- Cumulative effects are usually addressed:
  - at the level of technology
  - by using specific hardened devices (ELT – enclosed layout transistor, JIC – junction isolated circuit)
  - by using the transistor sizing (bigger transistors are less prone to the parametric changes)

- Online methods could be used for the detection of the changes

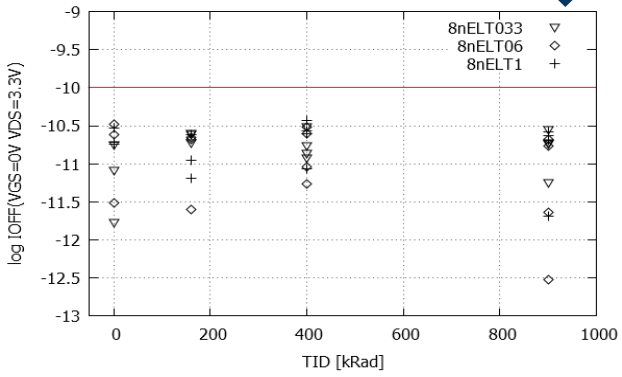
TiD Example: Radiation Assessment of SG13RH



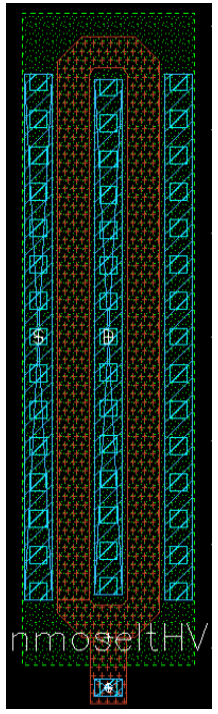




nmoseltHV device



ELT-nmos
Edgeless transistor
RHBD

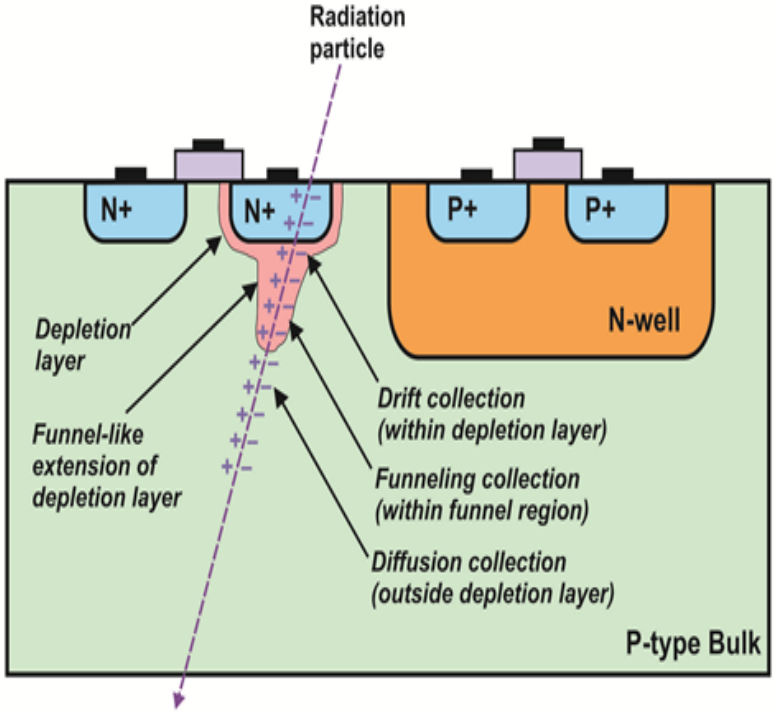


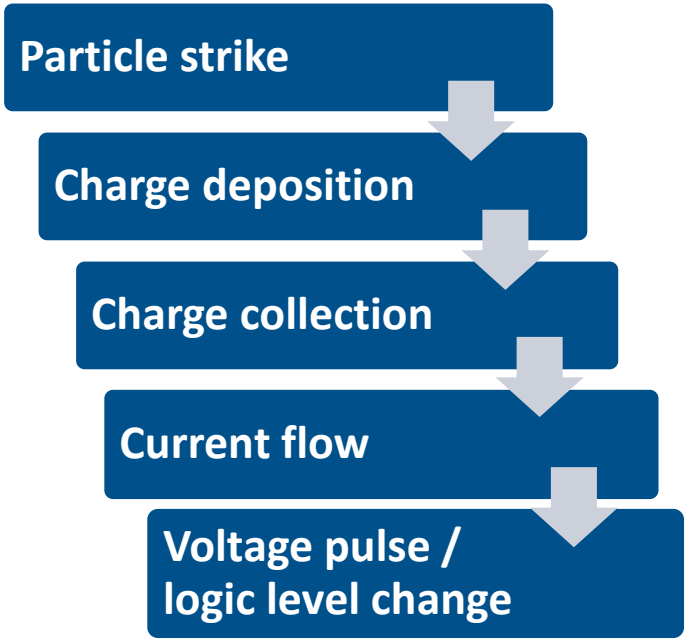
Radiation Source : Helmholtz-Zentrum Berlin für Materialien und Energie GmbH, Berlin. Gamma rays provided by Co^{60} source. Dosimetry performed by Farmer Ionization Chamber, nominal photon energy range from 60kV to 50MV.

Test Hardware : Keithley SCS-4200 Semiconductor Parameter Analyzer with Keithley 707B Switch Matrix Custom IHP Test Fixtures for measurements.

SEE Mechanisms

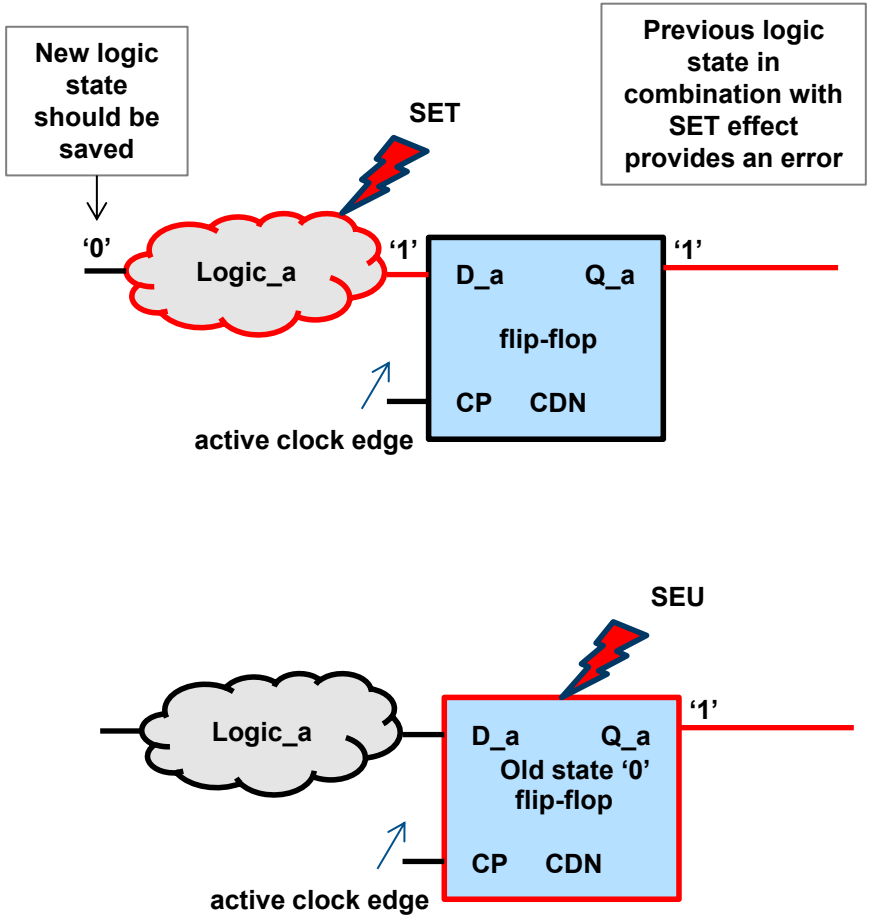
- SEEs are induced by a single energetic particle (e.g. heavy ion)
- Manifested as current flow, leading to subsequent voltage disturbance
- Result in soft errors, i.e. change of logic value stored in memory
- SEE modeling and characterization is a key requirement in rad-hard design



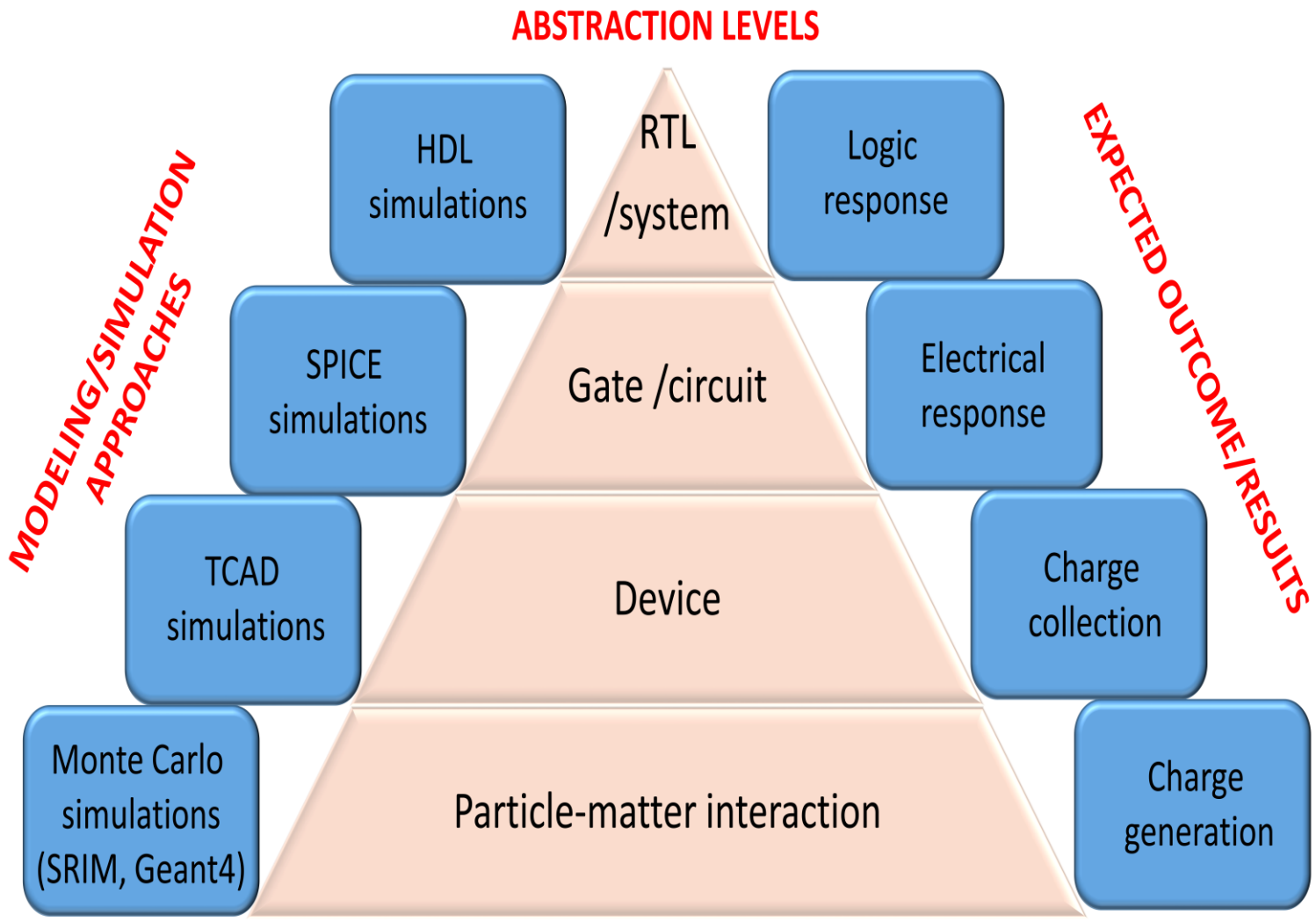


Single Event Transients(SETs)/Single Event Upsets (SEUs)

- High energy particles can cause the bit flipping in logic (SET) or registers (SEU)
- Chip can provide wrong outputs or be brought to non-functional state
- Several ways to addressing these events:
  - transistor sizing
  - special radhard flip-flop architectures (TMR)
  - filtering of transients
  - use of ECC for addressing SEUs in SRAMs

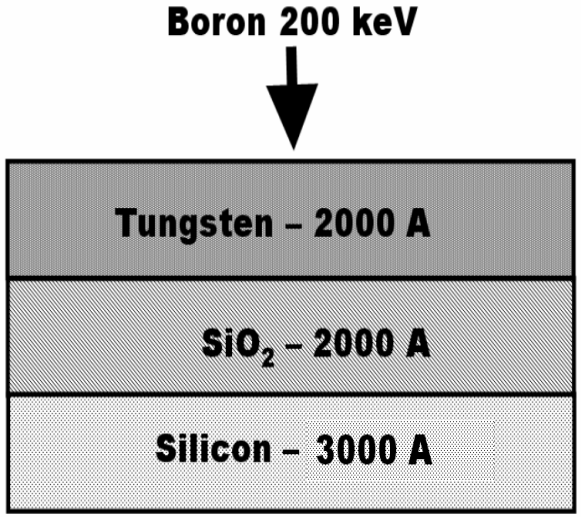


Multi-level SEE Modeling and Simulation

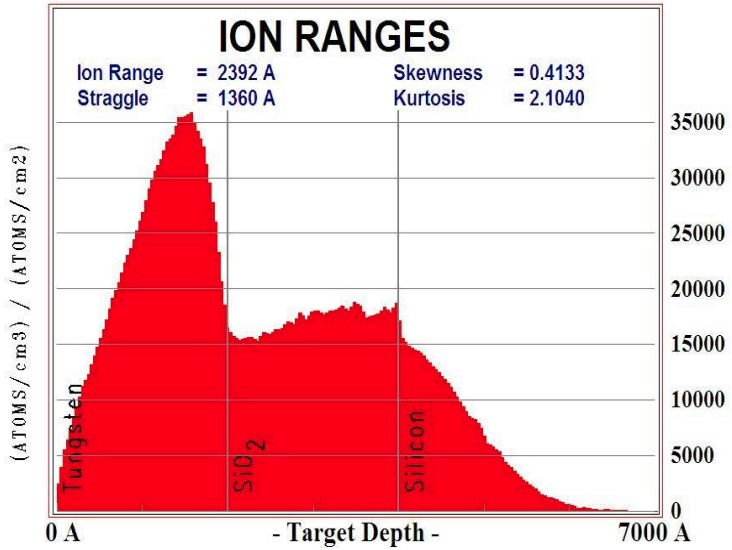


Particle-Matter Interaction Simulations

- Analysis of particle-induced charge deposition
- Allows to identify the charge deposition in each layer
- Performed with Monte-Carlo based tools:
  - **SRIM/TRIM open source simulator**



SRIM/TRIM inputs	SRIM/TRIM outputs
Layer structure of device	Charge deposition profile
Particle energy / type	Range of particle in matter
Angle of incidence	LET (linear energy transfer) as a function of range

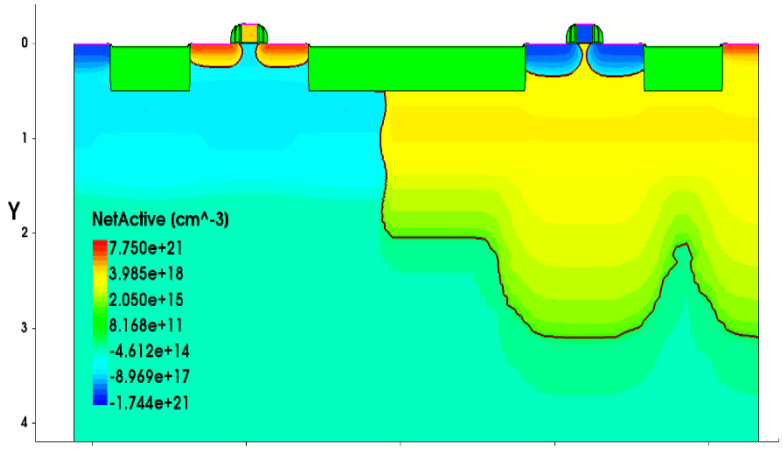


www.srim.org

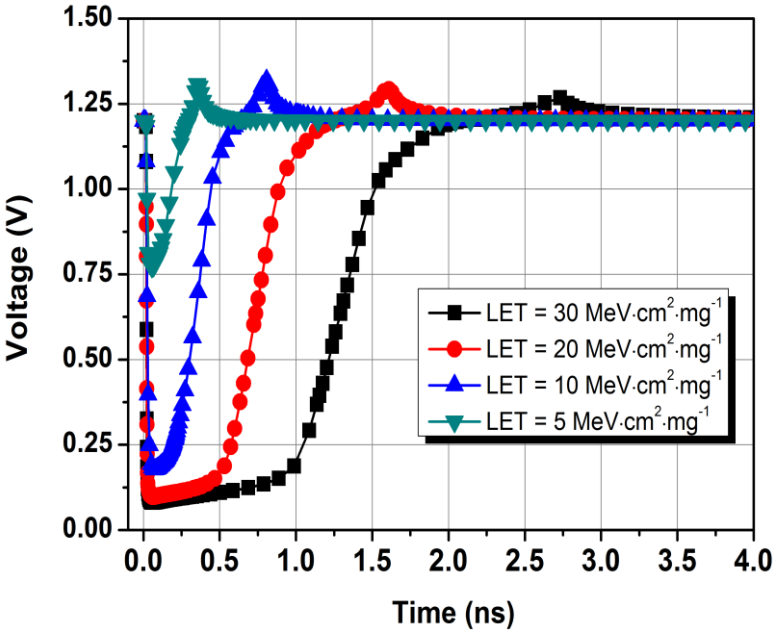
Device Simulations

- Analysis of charge collection process in a single device (transistor)
- Performed with commercial TCAD tools:
  - **Synopsys Sentaurus**
- Built-in heavy ion model
- Two operating modes: 2D or 3D
- Can be coupled with SPICE (mixed-mode)

2D TCAD simulation of SETs in 130 nm inverter

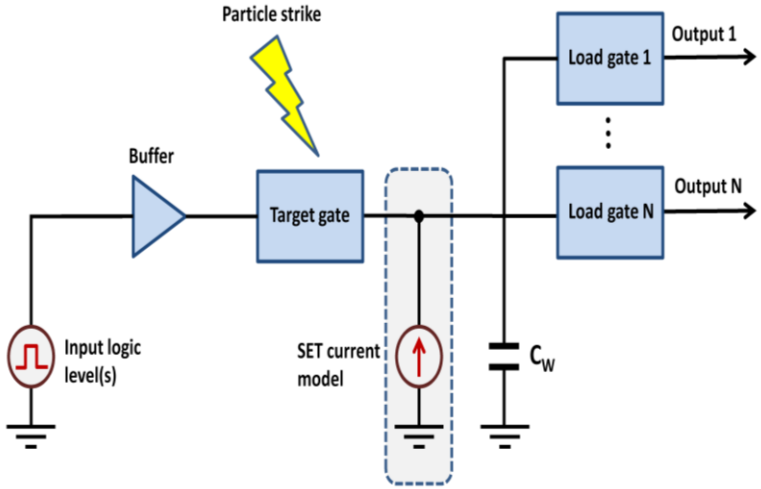


TCAD inputs	TCAD outputs
Device structure and technology parameters	Induced current pulse shape
Particle specifications (LET, strike direction and location)	Induced voltage pulse shape

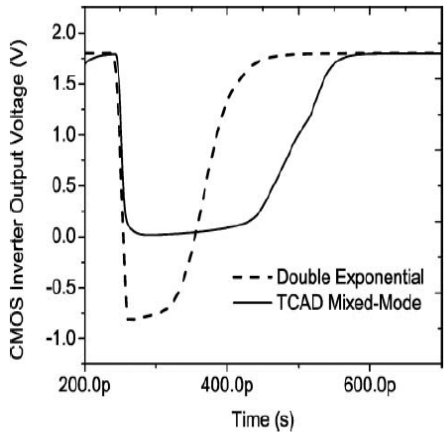


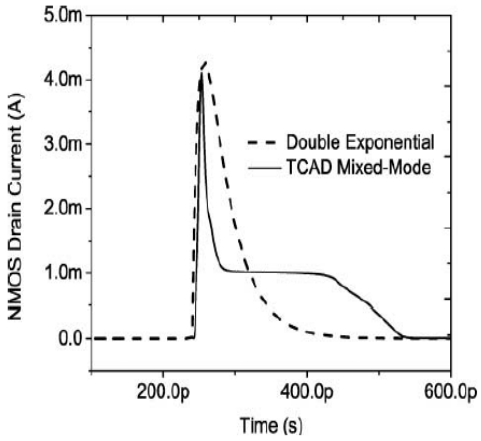
Gate/circuit simulations

- Current injection in SPICE simulations



- Limitations of double-exponential model

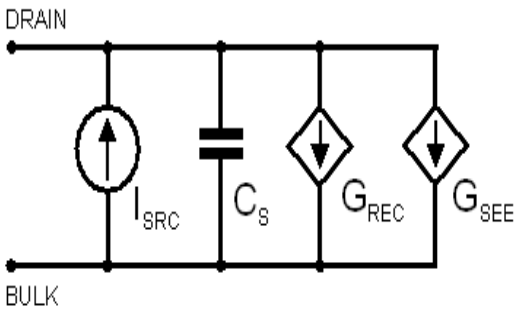




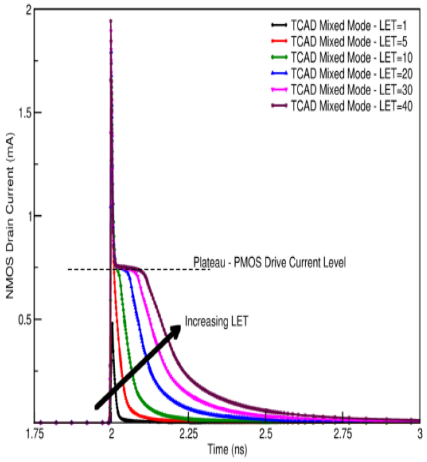
- Bias-dependent current model: realistic

- Common SEE current model:
  - **Double-exponential current source**

$$I_{SET}(t) = \frac{Q_{COLL}}{\tau_f - \tau_r}\left(e^{-t/\tau_f} - e^{-t/\tau_r}\right)$$

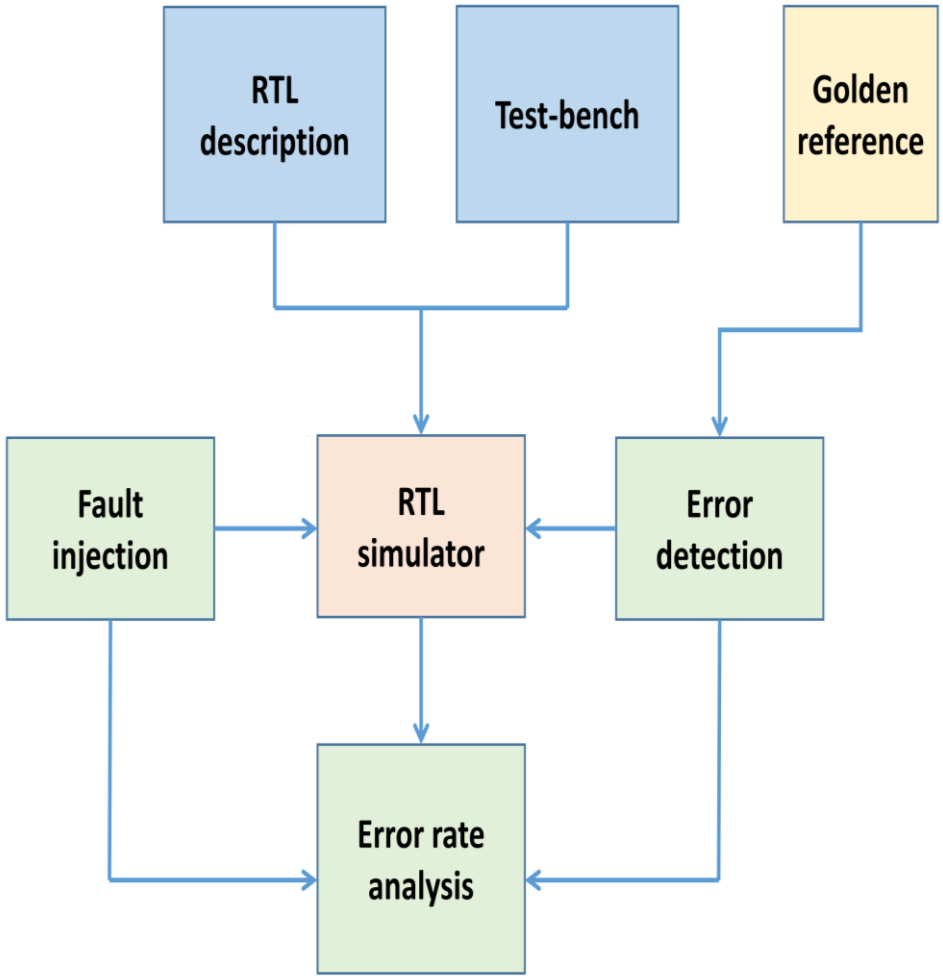


J. S. Kaupilla, IEEE TNS, 2009



RTL/system Simulations

- Fault injection in complex digital circuits (e.g. processors)
- Faults (SEEs) are modeled as:
  - bit flips (SEUs in memory elements)
  - temporary level changes (SETs in combinational gates)
- Suitable for analysis of SEE propagation effects in large designs
- Performed with RTL (VHDL- or Verilog-based) simulators:
  - **Modelsim**
  - **NCSim**



Comparison of SEE Simulation Approaches

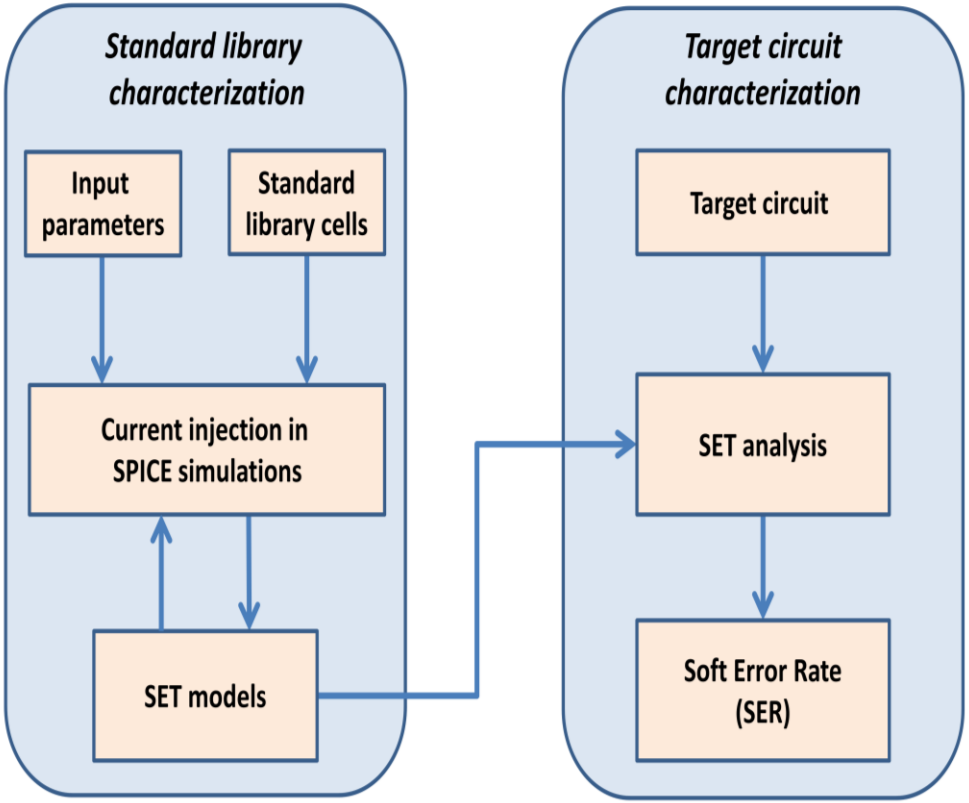
Approach	Advantages	Disadvantages
Particle-matter	Very fast simulations (in the order of seconds)	Neglects technology parameters
Device	Accurate analysis of charge collection	Too slow even for simplest structure (can last several hours)
Gate/circuit	Provides insight into electrical effects Fast for small circuits	Neglects some important physical aspects Too slow for complex circuits
RTL/system	Fast analysis of SEE propagation in complex circuits	Neglects electrical and physical aspects

Optimization of SEE Characterization

- Multi-level SEE simulation is time consuming for complex circuits
  - Simulations have to be done for every circuit node

- Optimization approach:
  - Characterization of SEEs in standard cells -> done only once
  - Use characterization data to establish analytical models for SER estimation

- Challenges:
  - Minimize the simulations
  - Establish accurate models
  - Apply the models effectively on a large design



Soft Error Rate (SER) Modeling

Total SER of a digital circuit:

$$SER = SER_{COM} + SER_{SEQ}$$

$$SER_{COM} = k \cdot Flux \sum_{i}^{Nodes} Area(i) \cdot e^{\frac{-Q_{CRIT}(i)}{Q_S}} \cdot P_{EM} \cdot P_{LM} \cdot P_{TM}$$

$$SER_{SEQ} = k \cdot Flux \sum_{i}^{Nodes} Area(i) \cdot e^{\frac{-Q_{CRIT}(i)}{Q_S}} \cdot P_{LM} \cdot P_{TM}$$

P_{EM} = Probability of electrical masking

P_{LM} = Probability of logical masking

P_{TM} = Probability of temporal masking

SEE Generation Modeling – Critical Charge

- **Critical charge model based on superposition principle**

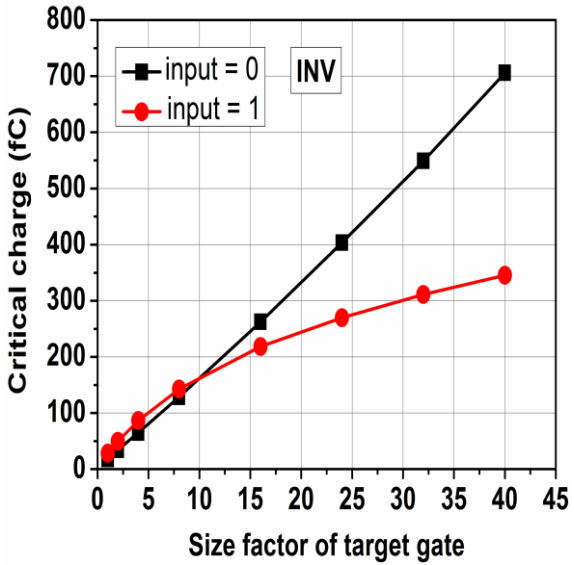
$$Q_{CRIT} = Q_{NOM} + \sum_{i=1}^{N} Q_i \cdot (K_i - K_{iNOM}) + f_{ERROR}$$

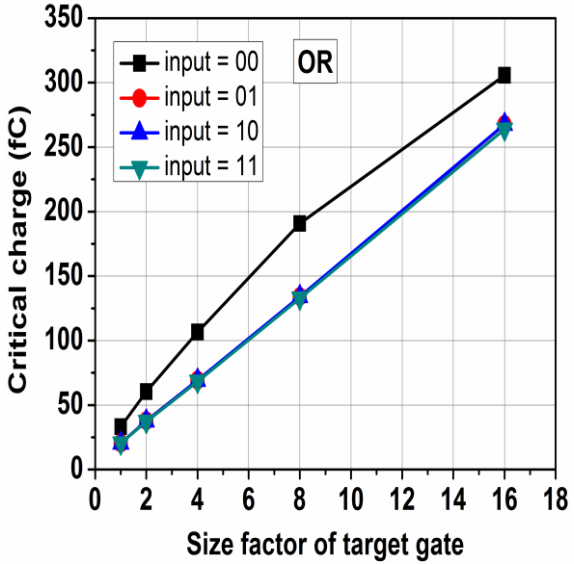
- **Critical charge in terms of target gates's size factor**

$$Q_{CRIT} = Q_{NOM} + Q_1 \cdot (S - 1) + f_{ERROR}$$

- **Q_{CRIT} values are the same for some input levels**
  - Allows to reduce the number of simulations during standard cells characterization

For 130 nm CMOS





SEE Generation Modeling – SET Pulse Width

- **Sufficient to perform simulations only for the lowest driving strength**

for $S = 1$ and nominal V_{DD}

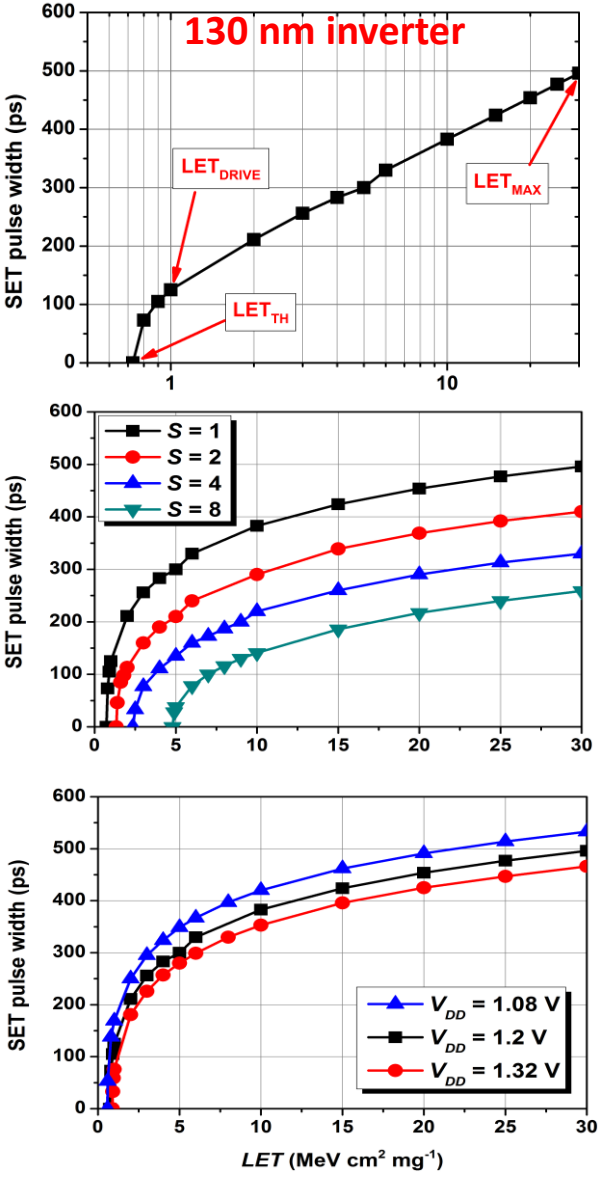
$$T_{SET}(LET) = \begin{cases} a_1 + a_2 \cdot \ln(LET), LET < LET_{DRIVE} \\ b_1 + b_2 \cdot \ln(LET), LET \geq LET_{DRIVE} \end{cases}$$

for $S > 1$ and nominal V_{DD}

$$T_{SET}(LET, S = n) = T_{SET}\left(\frac{LET}{n}, S = 1\right)$$

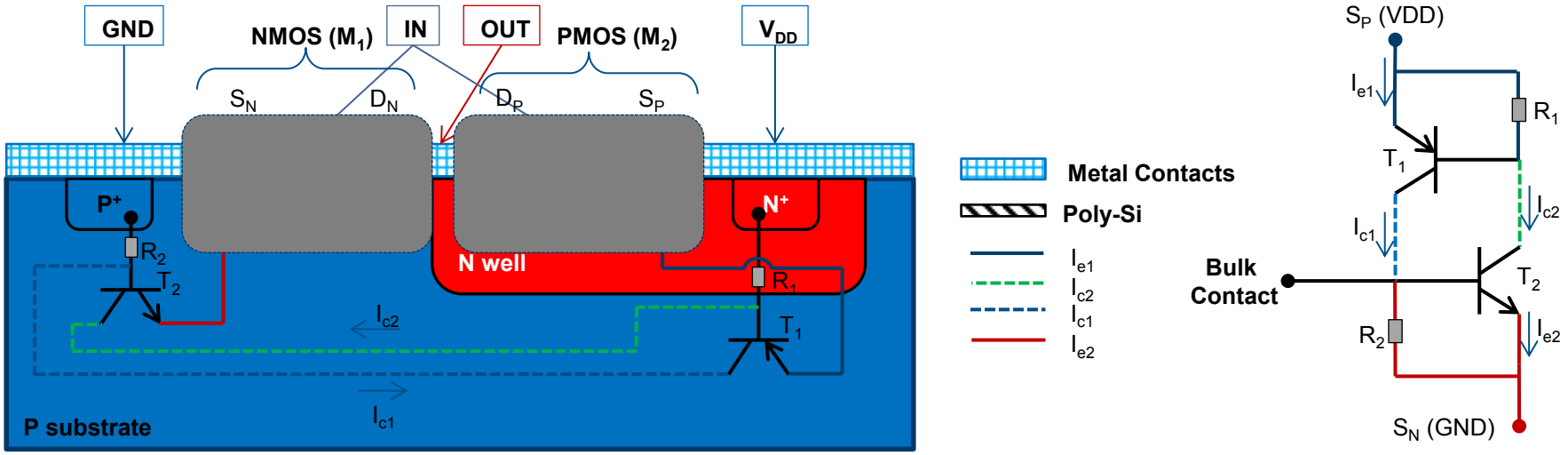
for V_{DD} variation

$$\Delta T_{SET}(\Delta V_{DD}) = \Delta V_{DD} \frac{\Delta T_{SET\_MAX}}{\Delta V_{DD\_MAX}}$$



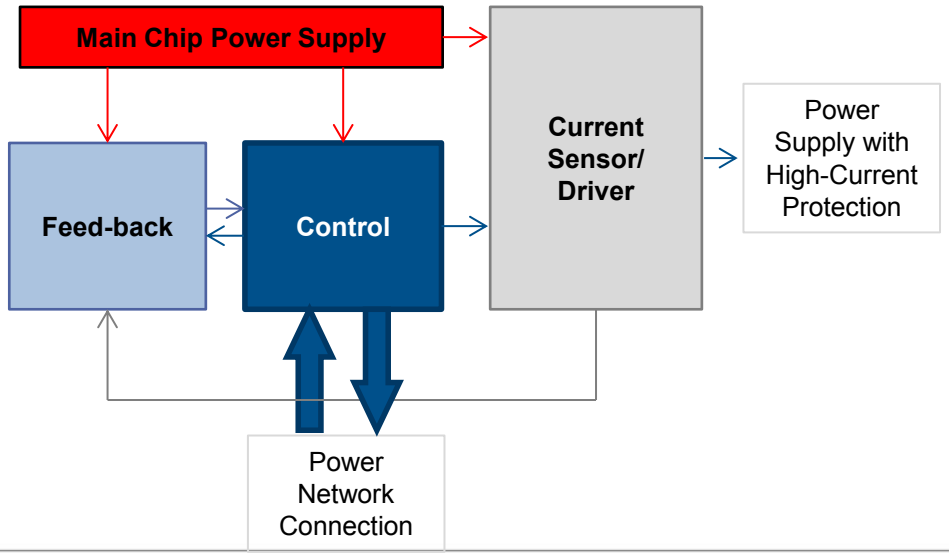
Single Event Latchups (SELs)

- **Single Event Latchups**
- Abnormal high current caused for example by single energetic particle causing in CMOS creation of parasitic bipolar transistors



Addressing SELs

- Some technologies are SEL hard (Silicon on Insulator, FDSOI)
- Strict design rules, substrate contacts, isolating MOS
- Protection circuits on the board (detecting SELs and switching off the power supply
- On-chip protection circuitry

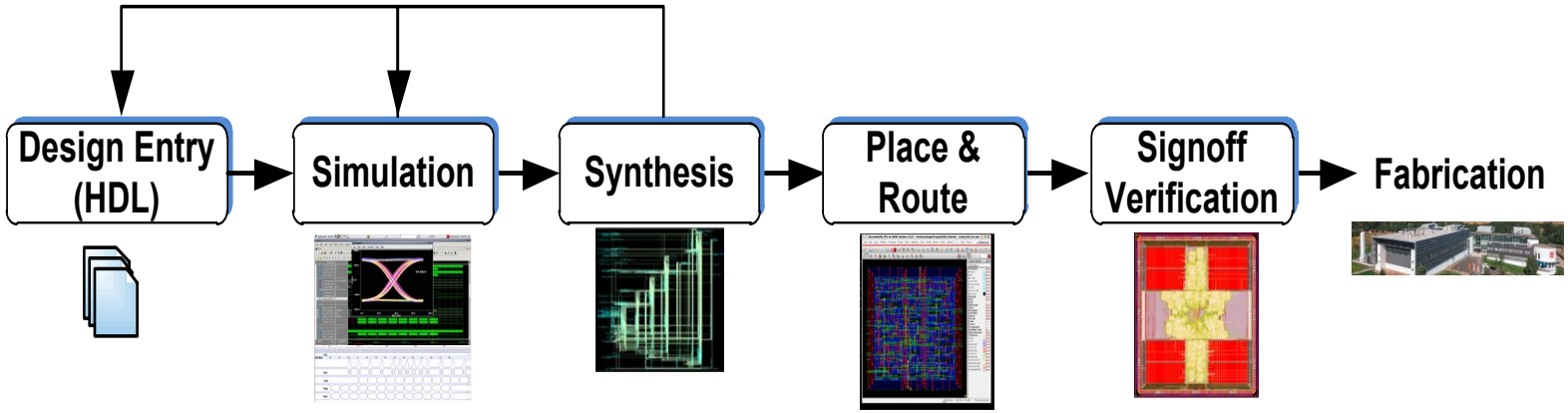


Addressing SEUs in Digital Systems

- In order to address SEUs the RHBD methods need to be applied
- The methodology could be applied at the different abstraction level of the design process
  - Cell level
  - RTL level
  - System level
- The methods could be static or dynamic
- Usual approach to deal with radiation induced errors are based on fault tolerance
  - The methods lead to overhead, and the goal is to reduce this overhead as much as possible without comprimising the application requirements

Digital Design Flow – Stages + Fabrication

- Design Entry → RTL Design Description
- Simulation →RTL simulation, Timing Simulation, PL Timing Simulation
- Synthesis → Translate RTL description to technology dependent gate level design
- Place & Route (PnR) → Physical Implementation of synthesized design
- Signoff → Geometrical, Electrical & Connectivity Verification
  - **D**esign **R**ule **C**heck/**E**lectrical **R**ule **C**heck & **L**ayout **V**ersus **S**chematic → DRC/ERC & LVS
- Fabrication → Mask layout send to fab in binary format (e.g. GDSII)
- Some additional/modified steps needed for radhard designs



Fault-tolerant Techniques

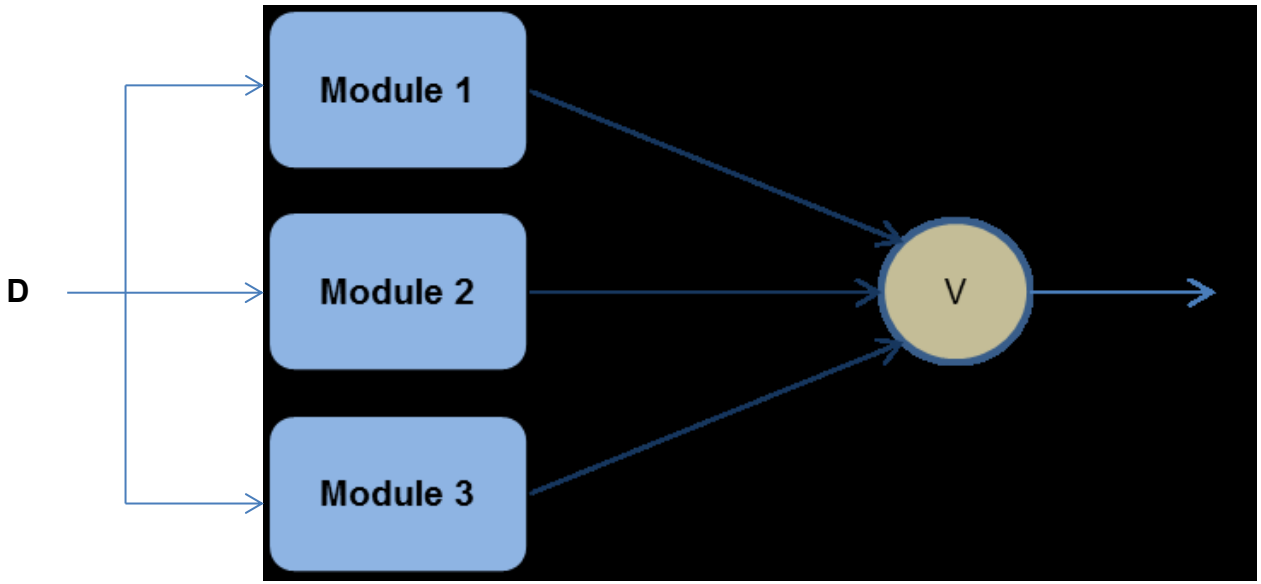
Almost all fault-tolerant techniques are based on the redundancy

- Hardware redundancy (N-modular, triple and double modular redundancy)
  - Could be preferable choice for safety critical systems
- Information redundancy (error detection and correction)
- Time redundancy
- Software redundancy

Hardware Redundancy with TMR

- The general approach is N-modular redundancy
  - Such systems are also known as M-of-N Systems
  - N=3, Triple Modular Redundancy (TMR)
  - N=2, Dual Modular Redundancy (DMR)

How TMR works?



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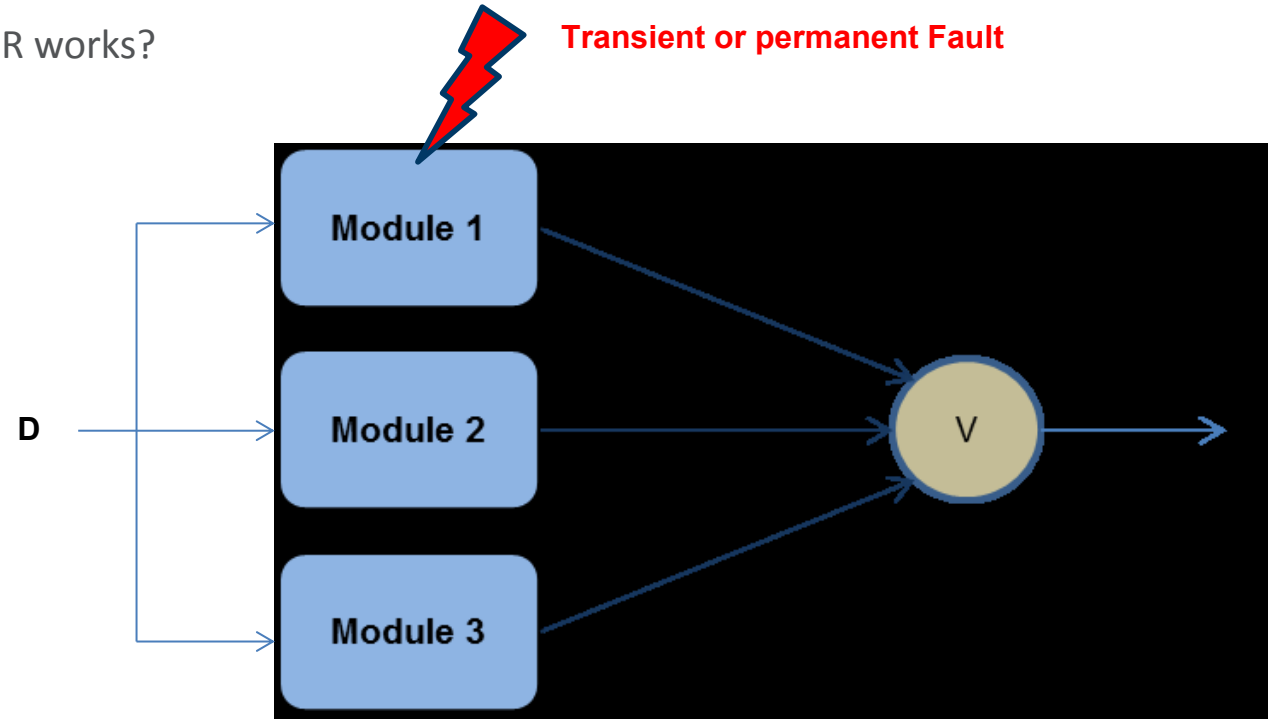

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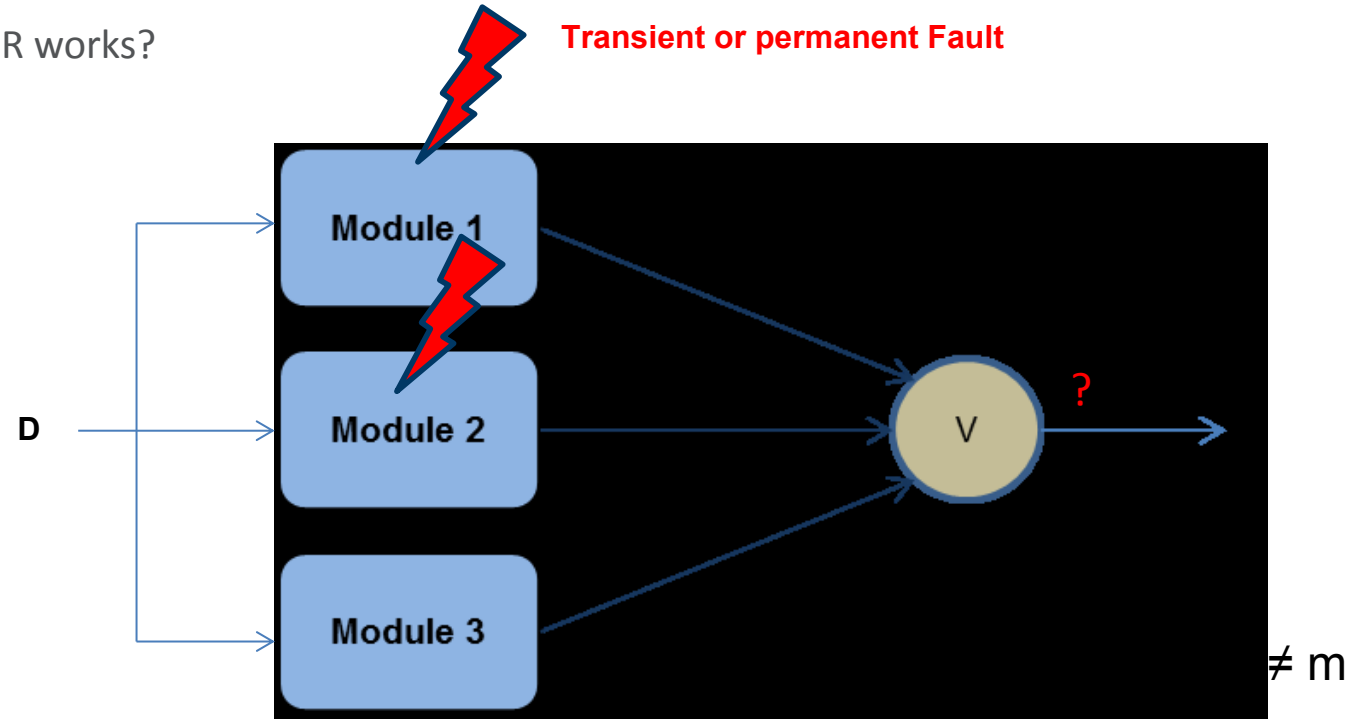
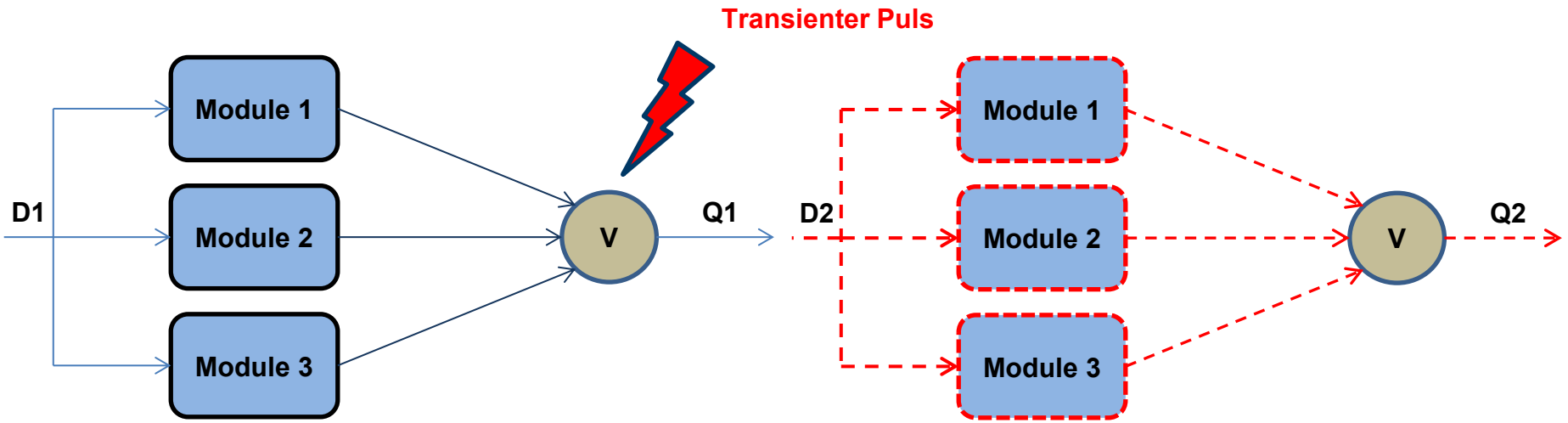


TMR is 2-of-3-System!

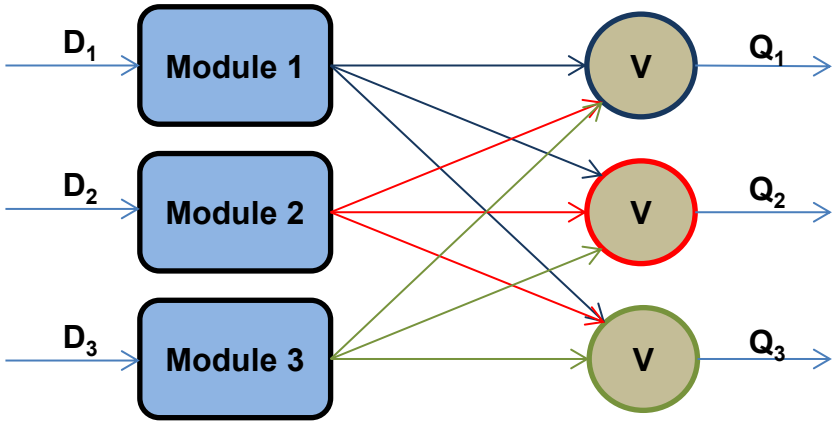
Limits of the simple TMR-Circuit

- Voter (V) is the single point of failure!



Alternative TMR-Architecture

- Full TMR-architecture, including TMR-Voter

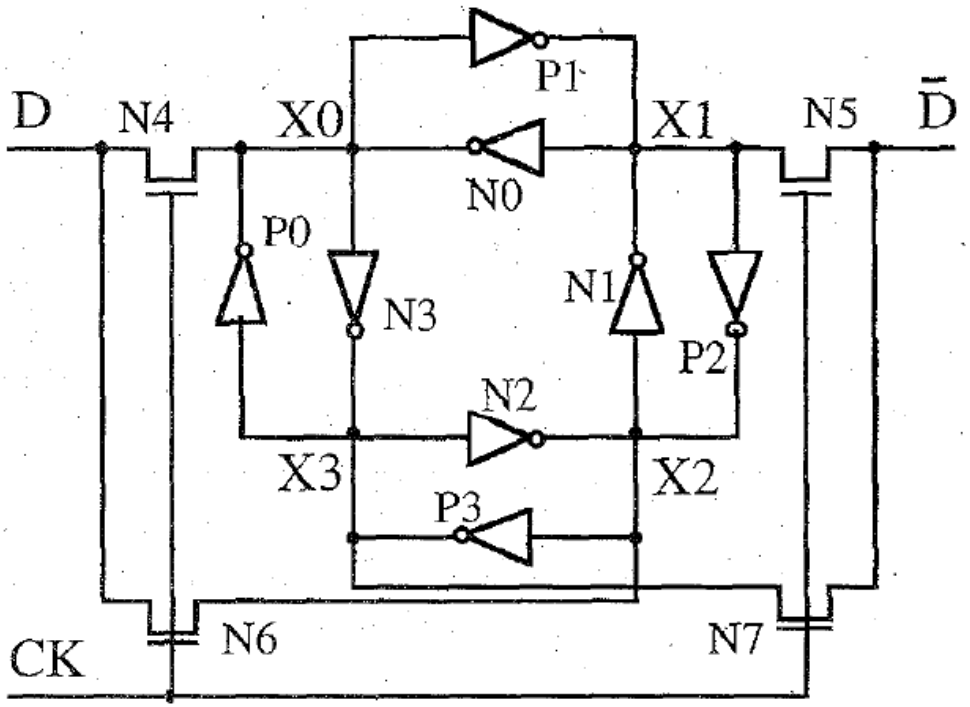


Radiation Hardness on the Cell Level

- The usual approach of space design companies is to address the radiation hardness at the cell level
- As a result the special cell library is designed (usually known as **radhard libary**)
- Important elements of the radhard cell library:
  - Radiation tolerant flip-flops: in order to avoid SEUs and filter SETs
    - TMR, DICE, HIT flip-flops
  - Special buffers tolerant against SETs: for clock and reset tree
    - Sizing of transistors could influence radiation sensitivity
  - Guard Gates: for SET filtering
    - Special architecture
  - IO pads, including SET filtering
  - Radhard SRAM:
    - radiation tolerance of the control interfaces
    - increased critical charge of the cell
    - special cell placement to avoid multi-bit upsets (MBU)
    - ECC for SEU correction

DICE Architecture

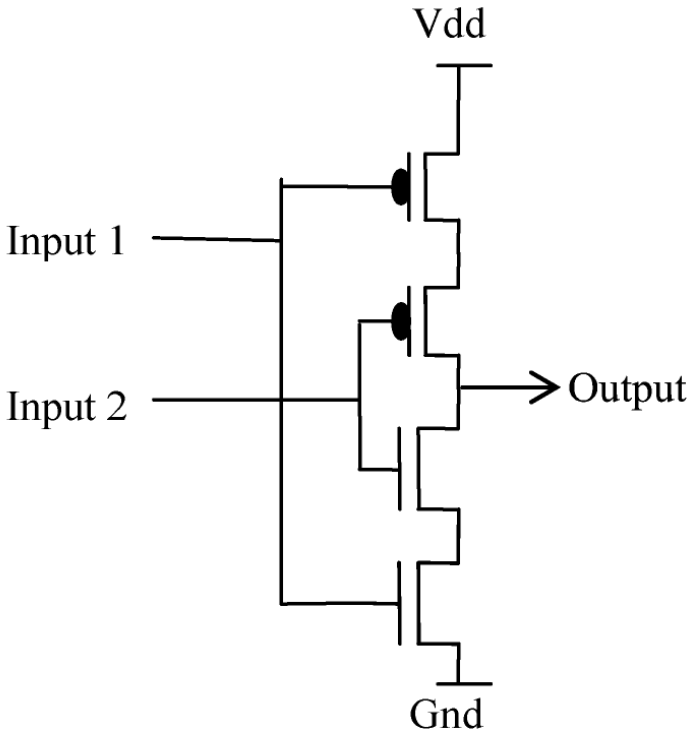
- Architecture based on the dupplication of the crosscoupled gates in order to avoid that single node upset can lead to latch state change.
- The other nodes are the „keepers“ of correct state
- This architecture is widely used in the industry relevant radhard standard cell designs

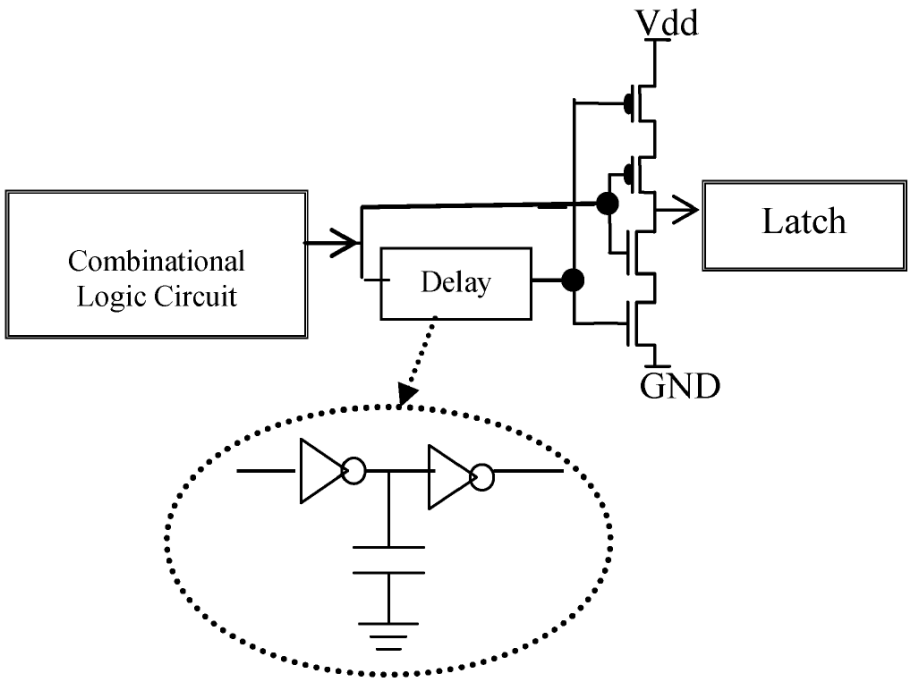


T. Calin, M. Nicolaidis, and R. Velazco, “Upset hardened memory design for submicron CMOS technology,” *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, pp. 2874–2878, Dec. 1996.

Guard Gate

- Guard gate is used as a filter against SETs
- The structure is based on the C-element input stage without keeper

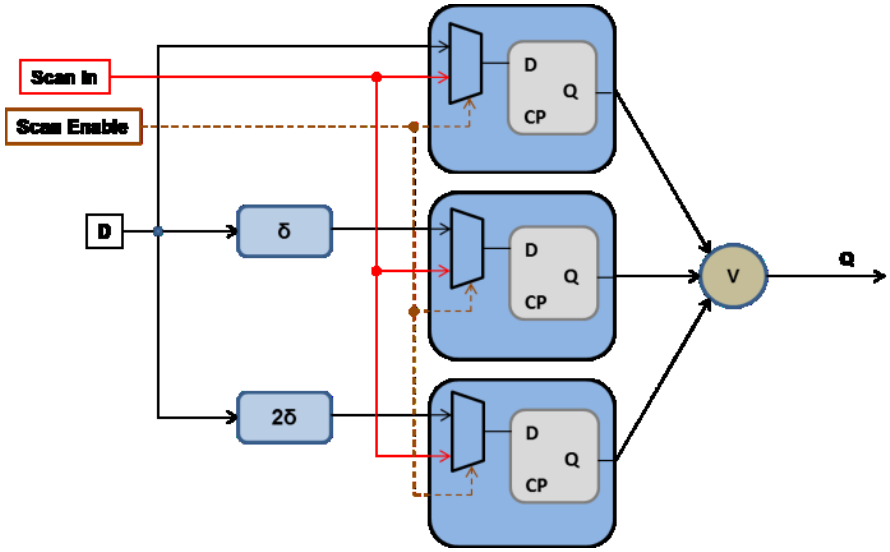


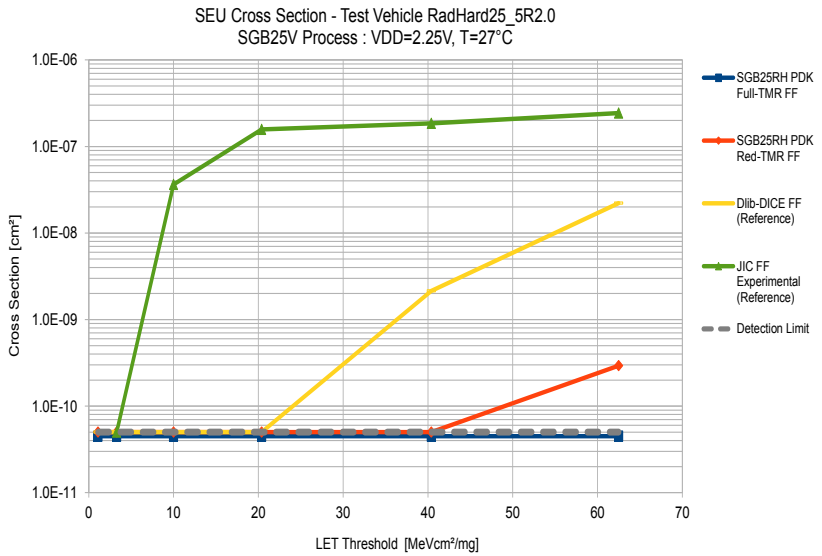


A. Balasubramanian, B. L. Bhuva, J. D. Black, L. W. Massengill, RHBD Techniques for Mitigating Effects of Single-Event Hits Using Guard-Gates

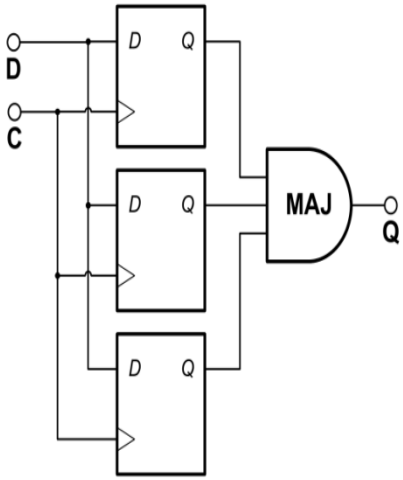
TMR Flip-Flops

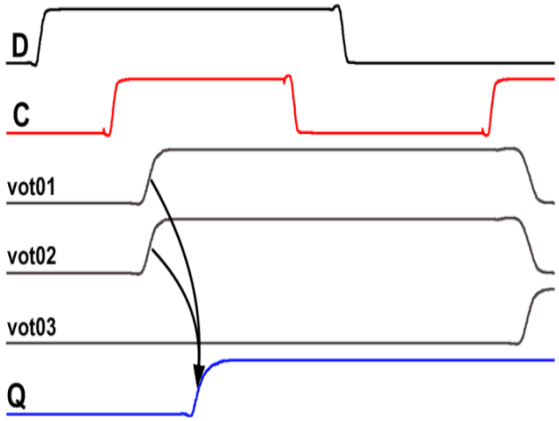
- TMR architecture could be effectively used against SEUs
- Single SEU in TMR scheme can be outvoted
- Cell placement is very critical to avoid MBUs (multiple bit upsets)
- Incoming SETs can be avoided with adding delay on input line
- The solution is very expensive in terms of additional hardware and power overhead





TMR in Application





The third flip-flop is hit by a particle, voter (MAJ gate) corrects the output

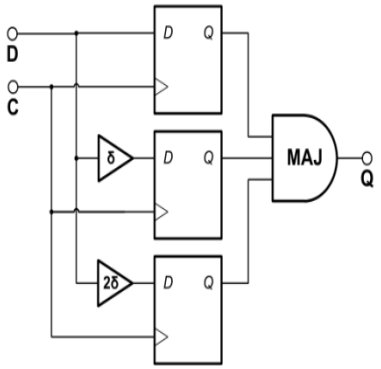
- TMR requires a triplication of sensitive logic
- A voter circuit (majority voter)

When and how to add TMR?

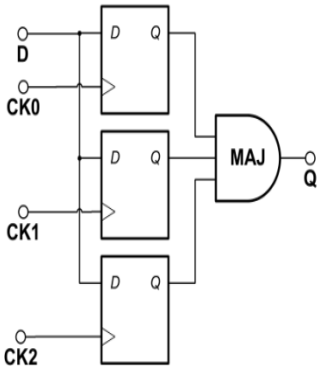
TMR with D-SET mitigation

D-SET – Mitigation

- Filter elements on datapath
- Filter elements on clock path

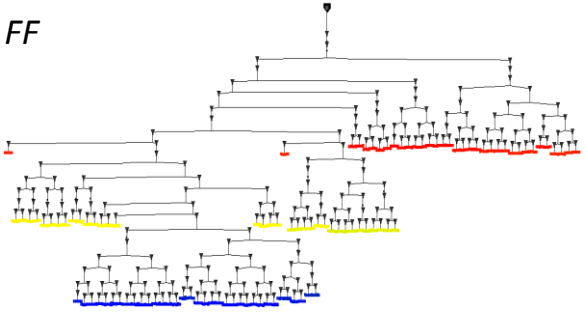


ΔTMR – FF



ϕTMR – FF

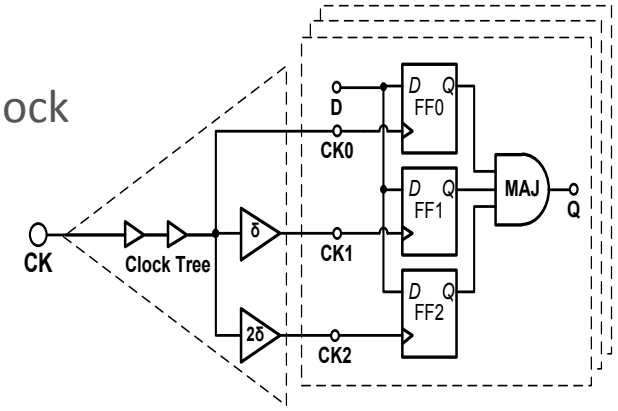
Clock Tree



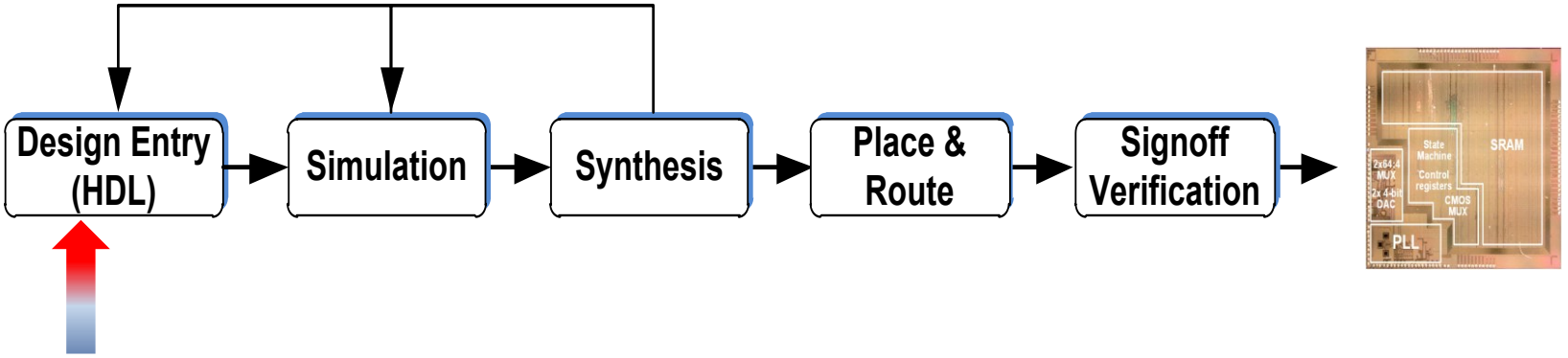
TMR Approaches in RH-Standard Cells

- ΔTMR: filtering is realized with local delay filters on datapath in each TMR cell

- ϕTMR: filtering is realized by hard delay insertion during clock tree synthesis (redundancy in time)



TMR Design Flow(s) – Soft-TMR – Approach I



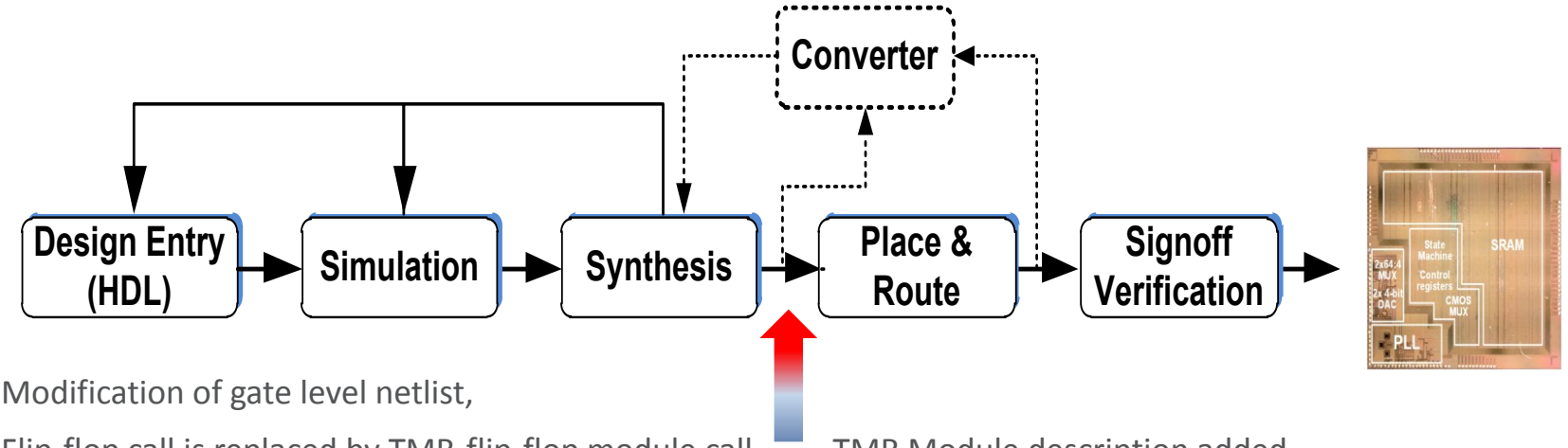
- TMR can be directly introduced at Design Entry Stage
  - Triplication of flip-flops and other logic is described at RTL Level
  - Voter functionality added in each flip-flop that should be protected:

```
Y <= (A and B) or (B and C) or (A and C)
```

Pro: Straigtforward, no additional effort except modification of HDL code

Cons : More complicated further steps of design process, it is difficult to pre-evaluate the library, use of standard RTL-IPs not possible.

TMR Design Flow(s)– Soft-TMR – Approach II



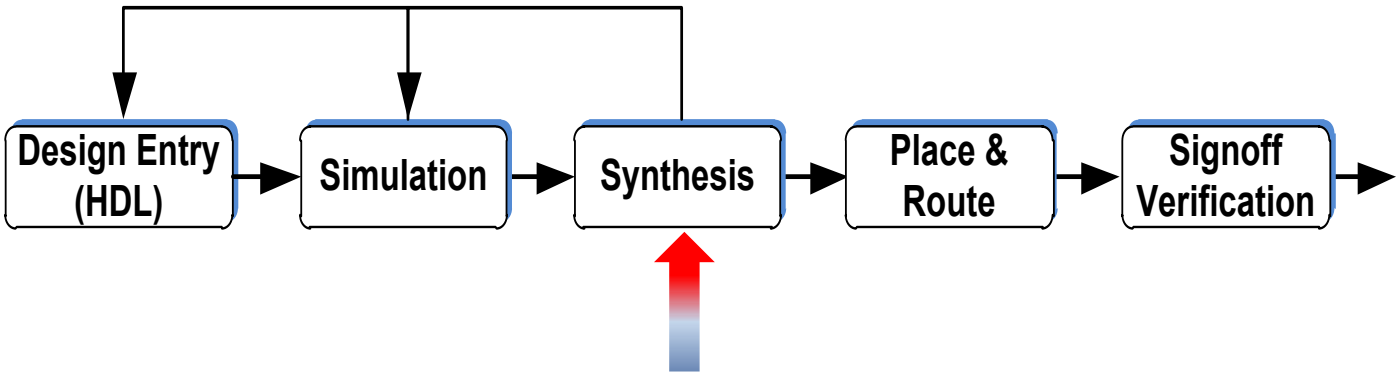
- Modification of gate level netlist,
- Flip-flop call is replaced by TMR-flip-flop module call, TMR Module description added

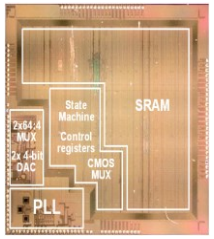
```
dfx1 u1 (.D(netA), .C(clk), .RN(nRST), .Q(Qlock) ); -> dtmrfx1 u1 (.D(netA), .C(clk),
.RN(nRST), .Q(Qlock) );

module dtmrfx1 (input D,C,RN, output Q);
       dfx1 ff0 (.D(netA), .C(clk), .RN(nRST), .Q(vot0) );
       dfx1 ff1 (.D(netA), .C(clk), .RN(nRST), .Q(vot0) ); ... ...
Endmodule
```

Pro: easy to constrain, no modification of source code

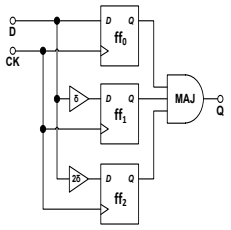
Cons : Same as previous approach, additional design steps

TMR Design Flow(s) – TMR – Library Approach III





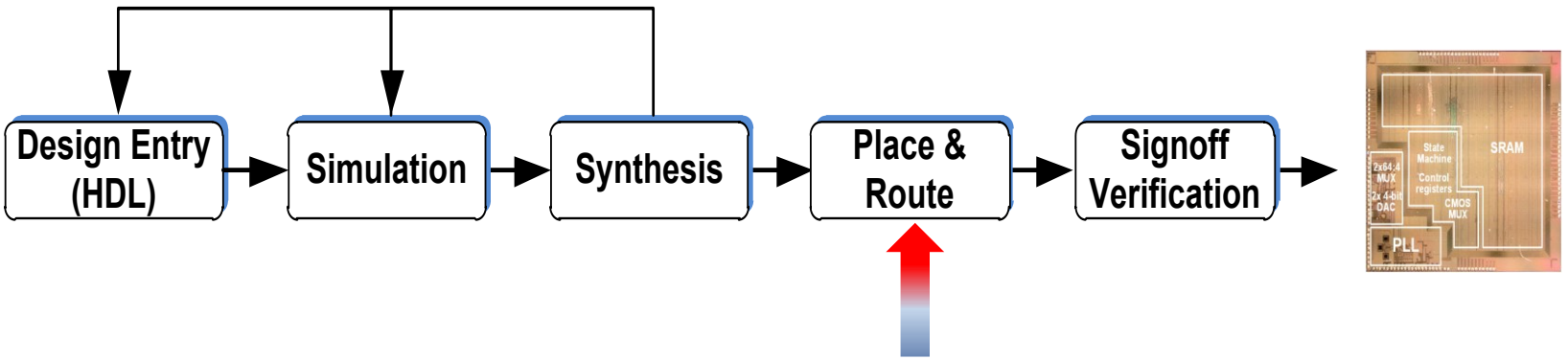
- Link pre-characterized RH-cells/TMR flip-flops at synthesis stage
  - ΔTMR flip-flops are part of a special radhard standard cell library
  - TMR cells are seen as common, but larger and slower flip-flops
  - Simply mapped during standard compilation



Pro: Radiation-Hardness By Design (RHBD) integrated on library level

Cons : Standard cell design of TMR cells and characterization is an additional high-effort task, higher overhead compared to previous approaches

How to introduce TMR – Libarary approach IV (not often used)



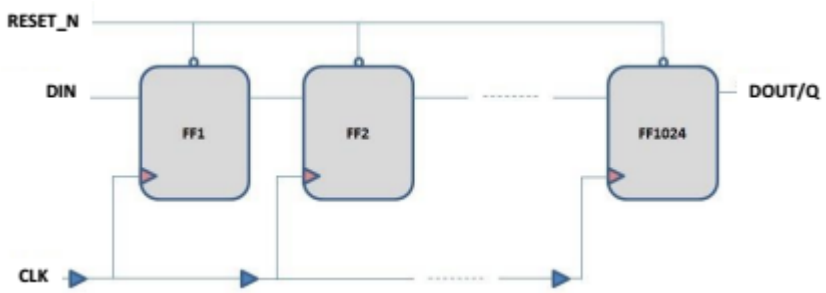
- Full triplication of sensitive logics and modules at layout level
  - Triplicated blocks must be conneced at upper hierarchy level
  - Design constraints must be modified (complex at system level)

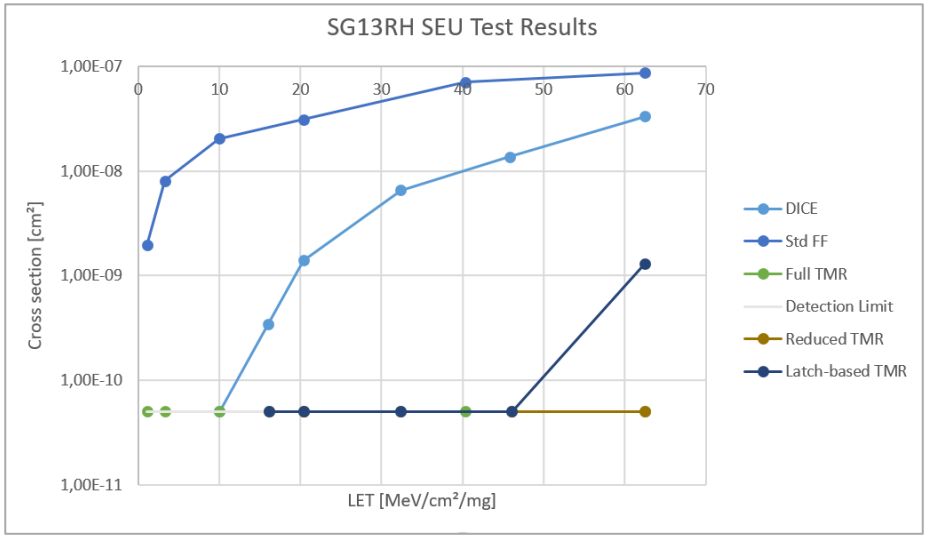
Pro: Effective Radiation-Hardness By Design (RHBD)

Cons : Complex design flow, additional design converter might be required, overhead

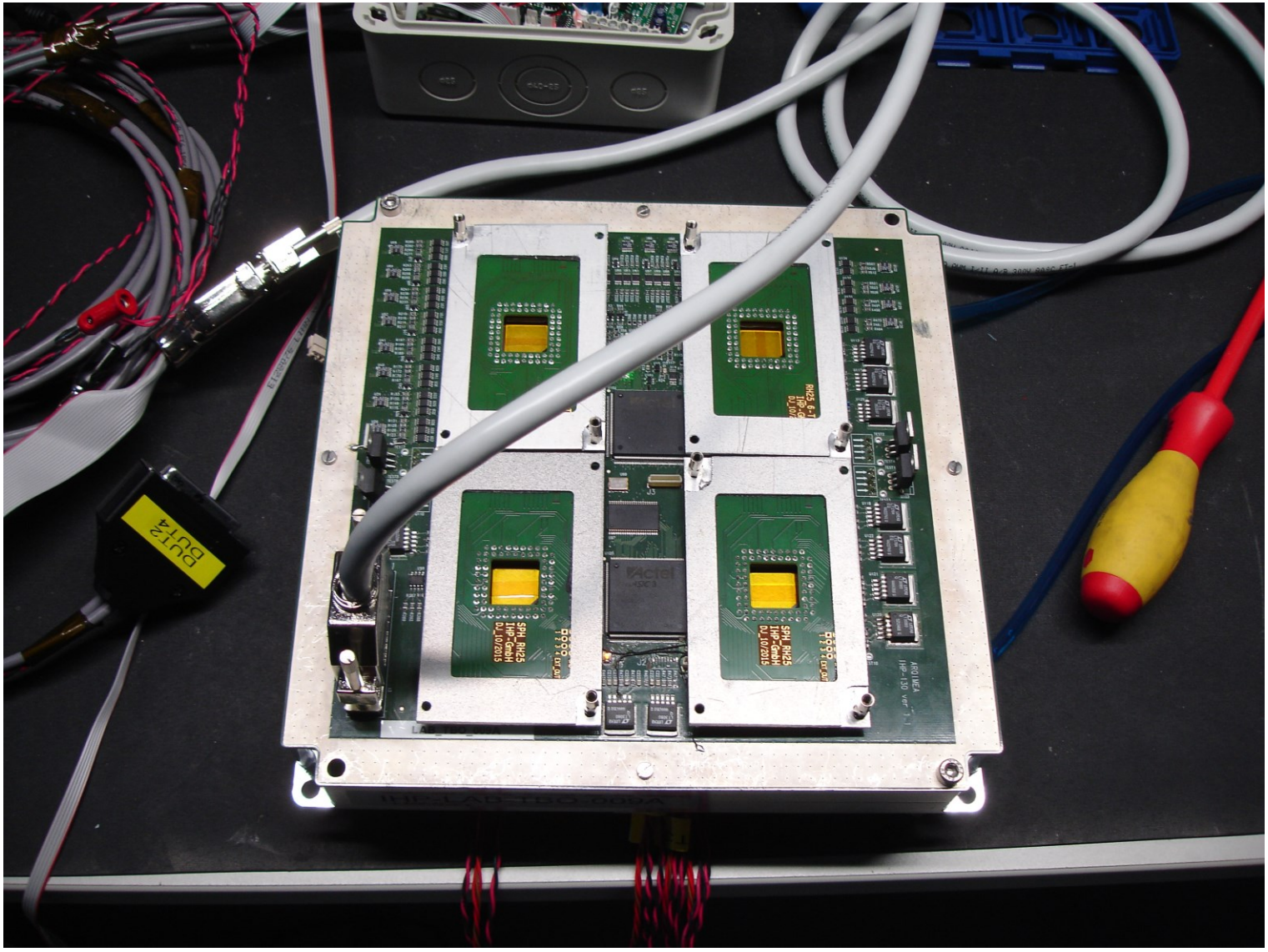
Radiation Testing

- Radiation testing is performed in the special labs equipped for TiD or SEE tests
- For TiD there are plenty of labs supporting Co-60 gamma radiation experiments
- SEE tests are possibile only in few labs (UCL, RADEFF etc.)
- For SEE tests special test setup is needed and the corresponding test vehicle
- Typical test vehicle – shift register
- TiD tests have also specific procedure

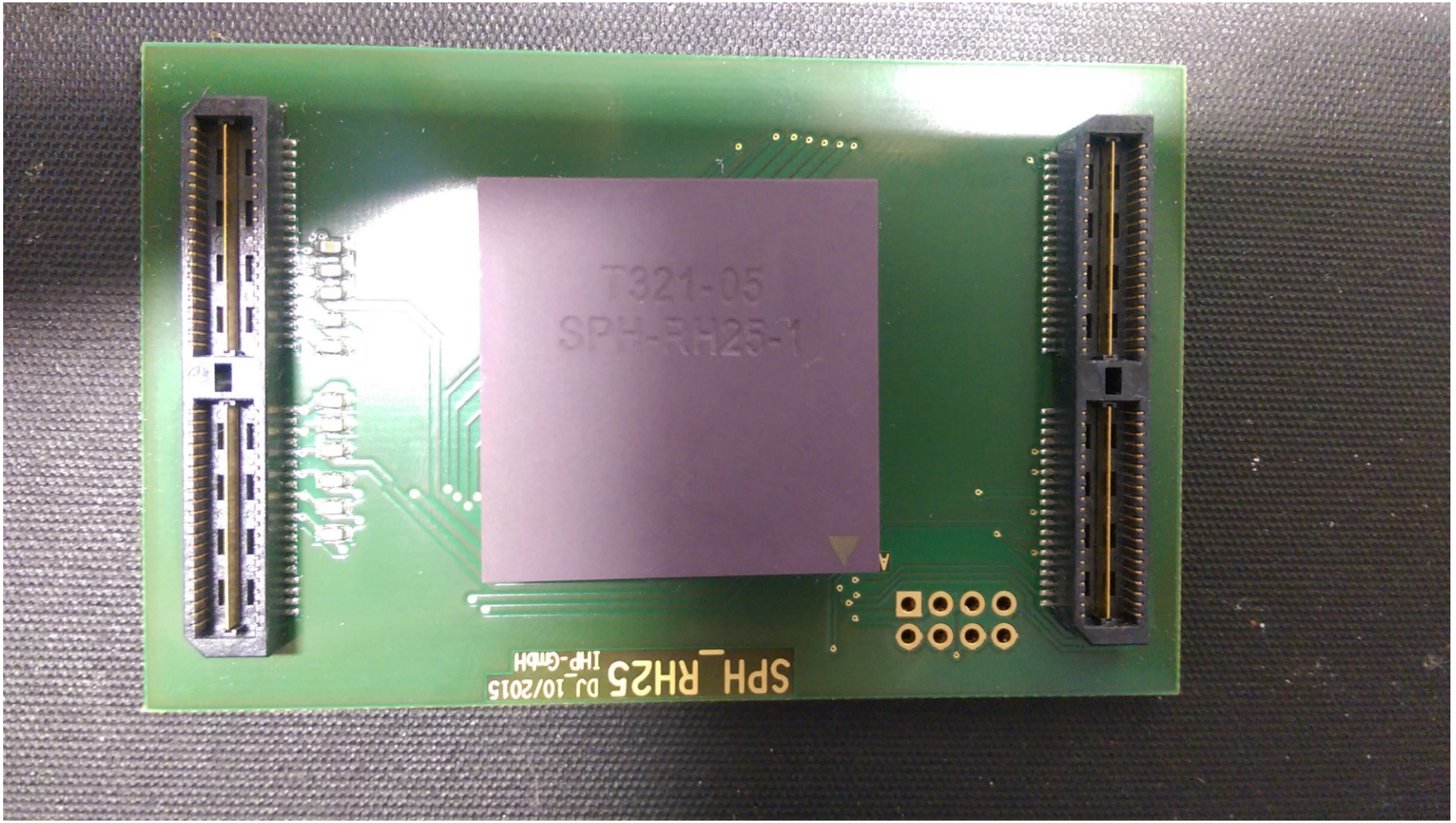




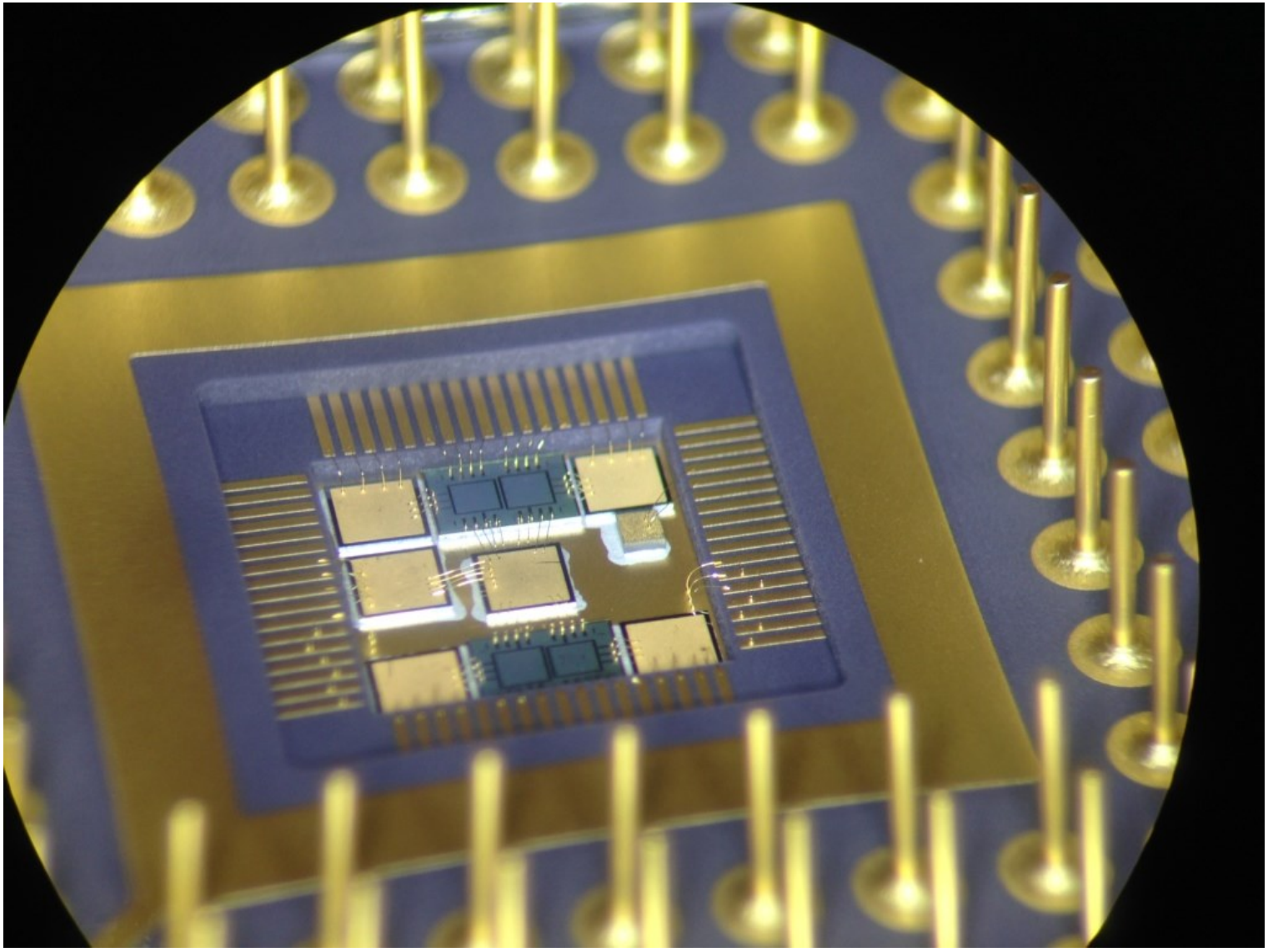
Radiation Testing



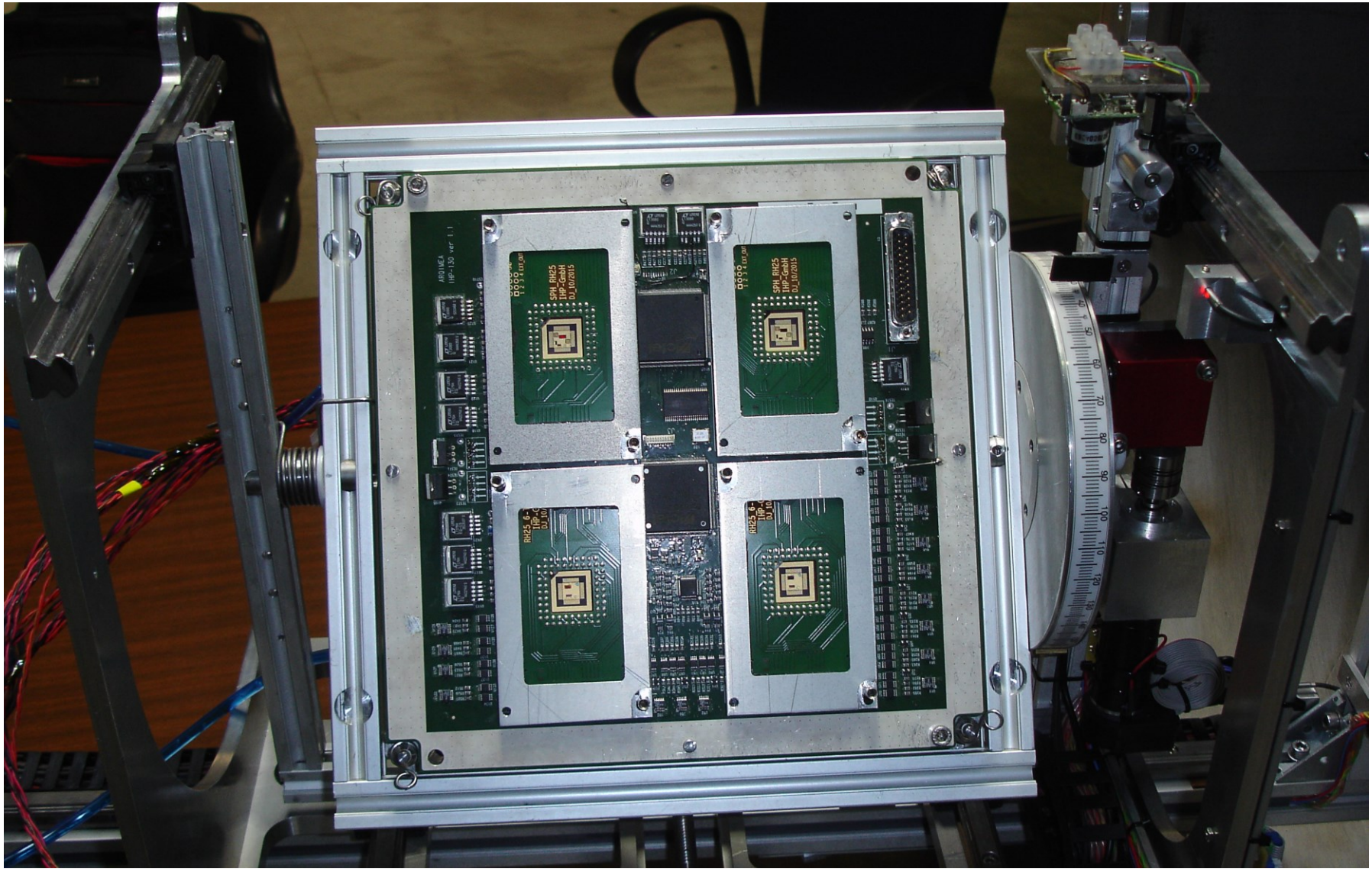
Radiation Testing



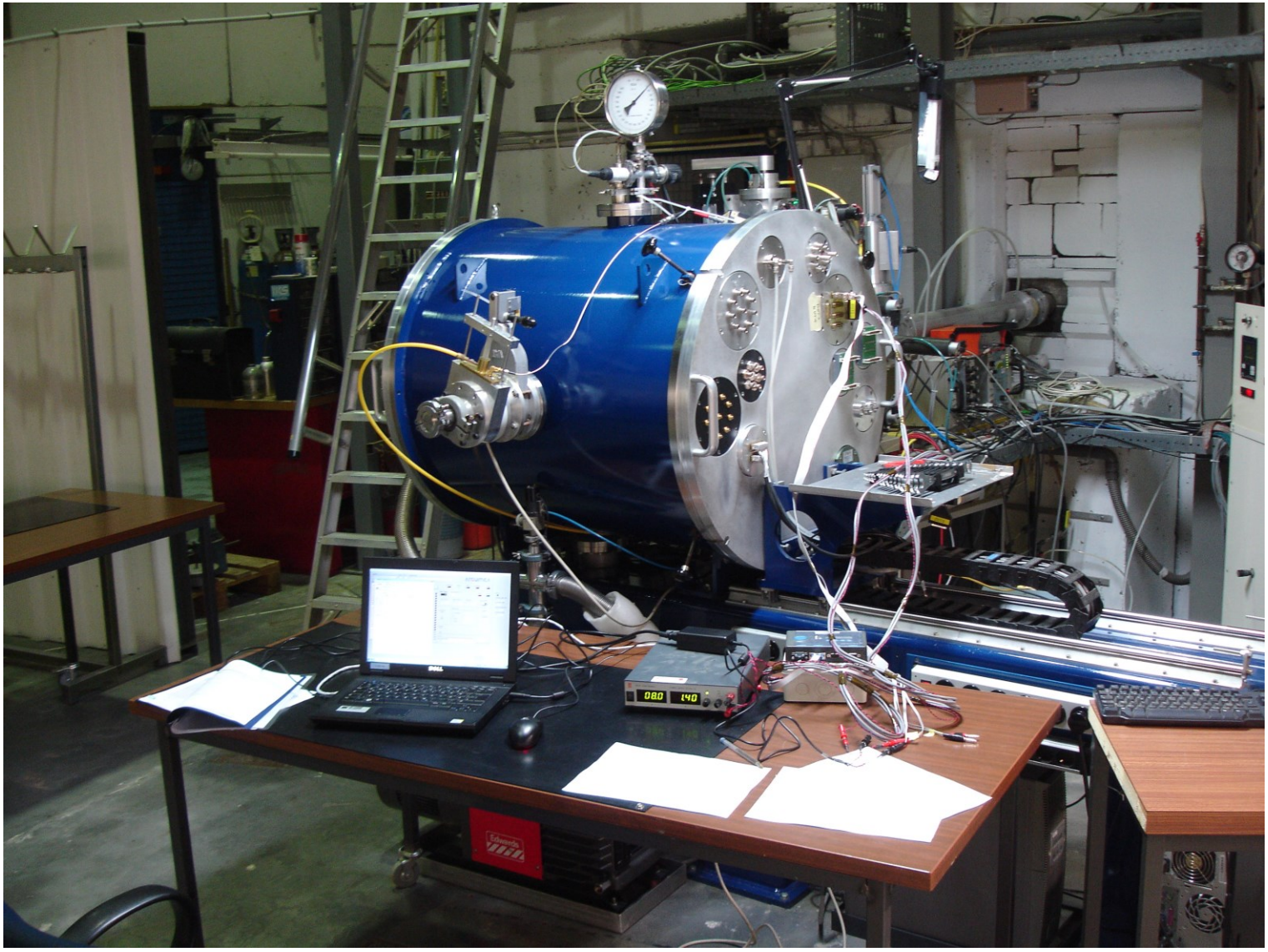
Radiation Testing



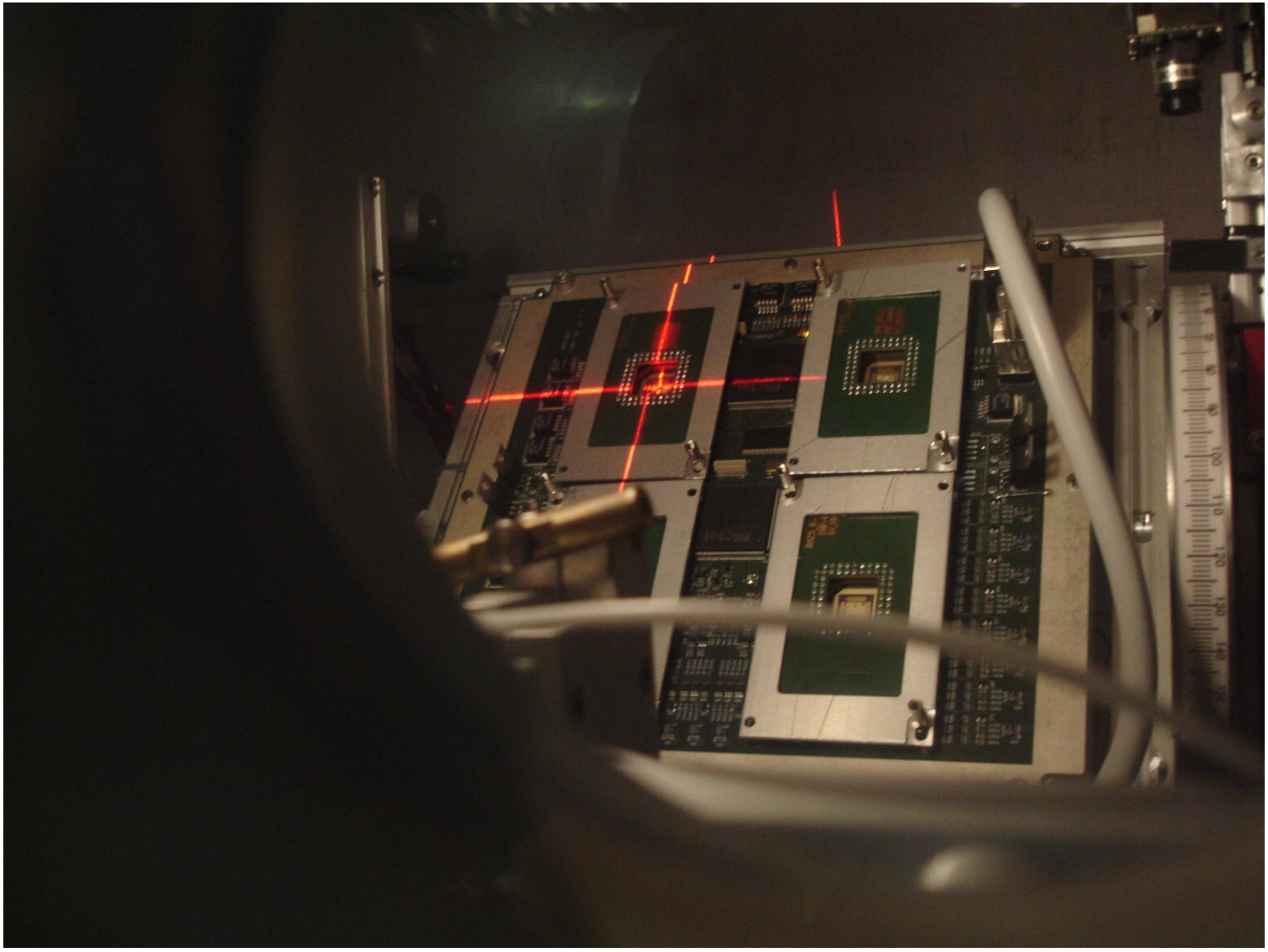
Radiation Testing



Radiation Testing



Radiation Testing



Consequences and Solutions

Redundancy = Power/Area Increase and performance drop!

The overhead could be more than N times baseline

The classical FT techniques could be performed in the more optimal way:

Static solutions:

- Limiting the level of fault tolerance but significantly reducing overhead (partial FT, ECC codes etc.)

Dynamic (adaptive) solutions:

- Enabling system adaptivity: using overhead only when it is needed
- Adaptivity is the key requirement for complex system implementation in advanced technologies

Example solutions:

- Static - partial and selective fault tolerance, FEDC
- Adaptive - adaptive MPSoCs

Resilience: Addressing with the same mechanisms different challenges

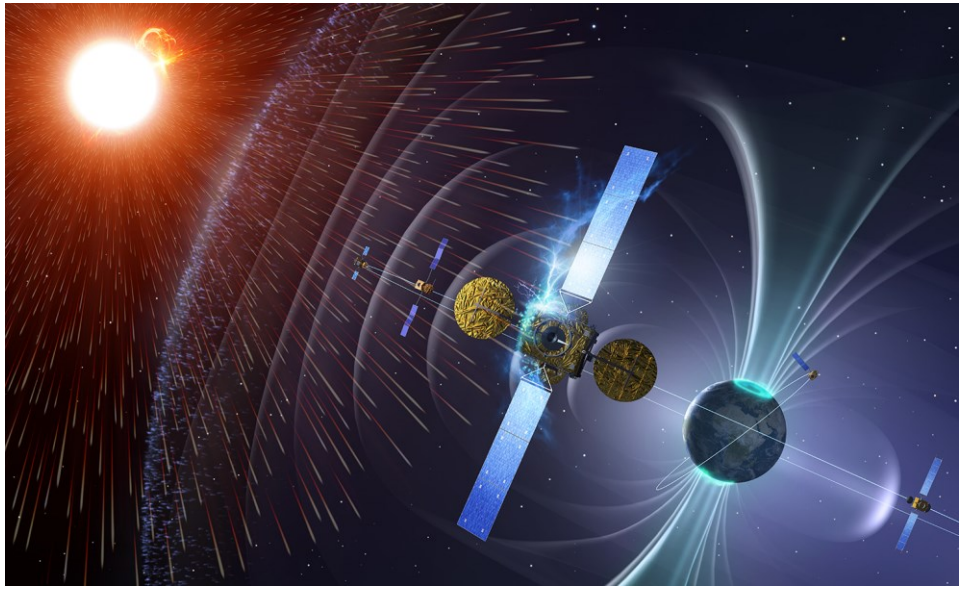
- Faults, PVT variations, security

Static Solutions

Selective Fault Tolerance – Motivation

- Continuous reduction of transistor size increases sensitivity for upsets in sequential elements
  - Mainly radiation induced
- Especially important for space applications because of higher particle radiation

- Protection of flip-flops against soft errors in digital circuits incurs significant overheads
- Reduce protection costs by protecting only flip-flops in which faults have an intolerable impact
- Identify critical flip-flops in which faults can produce
  - an effect on system output
  - persistent error in system state



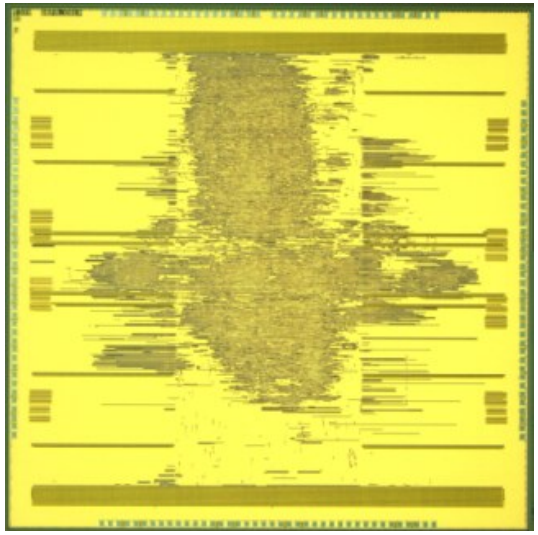
[https://www.esa.int]

A. Breitenreiter, et al, "Selective Fault Tolerance by Counting Gates with Controlling Value" 2019 IEEE 25th International Symposium on On-Line Testing And Robust System Design (IOLTS), Rhodes Island, Greece, July 2019, accepted paper.

Partial Fault Tolerance

- We can reduce the overhead if we protect with redundancy only the parts of the systems which are most critical (control logic, command/status registers)
- This method is called partial fault tolerance
  - However, some part of the system remains fully unprotected

- Example: Design of Digital Beamforming Network processor for synthetic aperture radar (EU Project DIFFERENT)
- Digital baseband IC and in IHP technology
  - DFBN Chip tape-out Aug 2015 – 46 mm2 in SGB25V
  - Tested on wafer and operational up to 250 MHz!
  - Optimized overhead
    - saving 20% in area and 33% in power
    - radiation hardened TMR flip-flops in control logic
    - Standard flip-flops in datapath



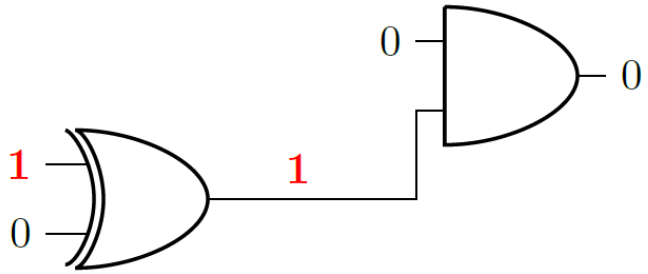
DBFN Baseband Processor - 46mm^2 in SGB25V, Sep 2015

Identification of Critical Flip-Flops – Overview of Methods

- Fault injection
  - Very high effort
- Error propagation probability calculation
  - High effort
  - Doesn‘t scale well for large circuits
  - Limited consideration of reconvergent paths
- Search for methods with lower complexity by higher level of abstraction
- Structural netlist analysis
  - Identification of critical flip-flops by structural properties directly derived from netlist
  - Reduced complexity
  - Sufficient accuracy?

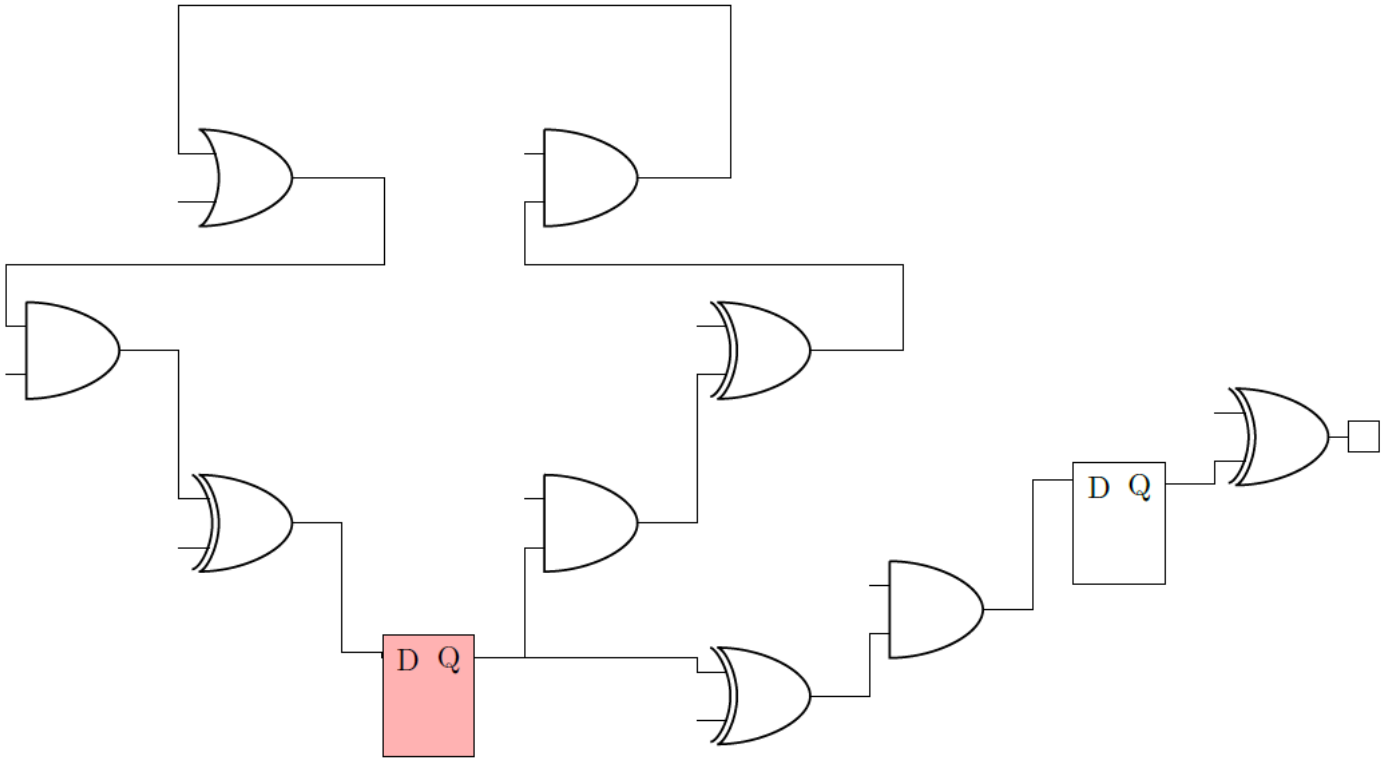
Proposed Method

- Two effects of faults regarded as critical
  - Propagation to primary outputs
    - Output paths with low probability of masking
  - Permanent error in system state
    - Feedback paths with low probability of masking
- Logical masking by gates with controlling value
  - AND
    - Controlling value ‘0’
    - One input ‘0’ → output ‘0’ independent of the other input
  - XOR
    - No controlling value
    - Every transition at the inputs causes a transition at the output
- Idea:
  - Paths with low number of gates with controlling value have low probability of masking
  - Select Flip-Flop for protection if
    - on cycle with a low number of gates with controlling value
    - Path to output with a low number of gates with controlling value



A. Breitenreiter, et al, "Selective Fault Tolerance by Counting Gates with Controlling Value" 2019 IEEE 25th International Symposium on On-Line Testing And Robust System Design (IOLTS), Rhodes Island, Greece, July 2019, accepted paper.

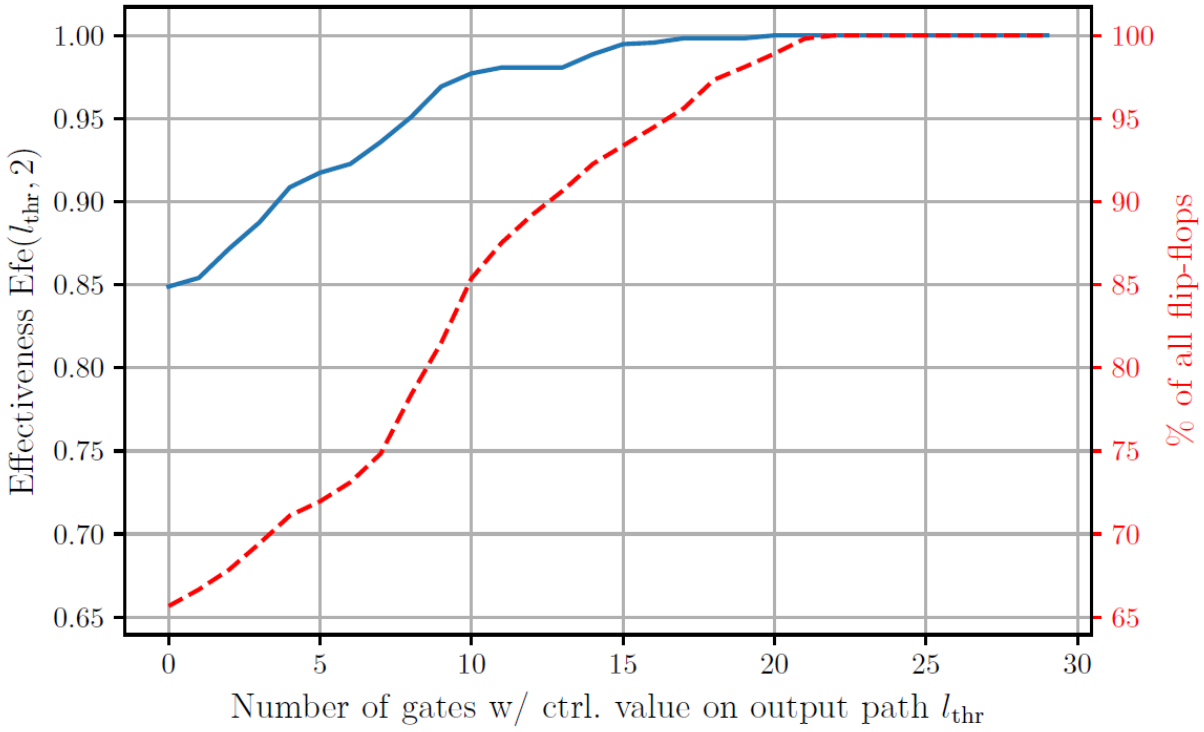
Proposed Method – Illustration of the criteria



- The red flip-flop
  - is on a cycle with c = 4 gates with controlling value
  - has an output path with l = 1 gates with controlling value

Evaluation Results – Merged Results

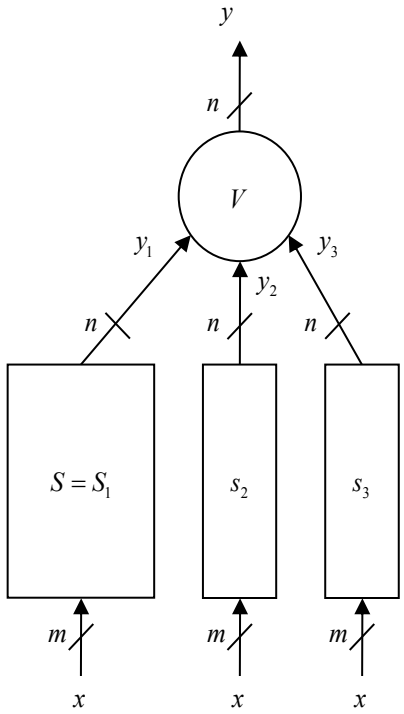
- Effectiveness of flip-flop selection based on the number of gates with controlling value on the output paths and number of gates with controlling value on cycles
- Threshold for the number of gates with controlling value on cycles c_{thr}



- Protecting about 75% of all flip-flops can avoid 95% of the errors

Another Method for Selective Fault Tolerance

- Fault tolerance is guaranteed only for input assignments of critical tasks, since it is not required for other signals
- We can make the trade-off between the FT level and area increase



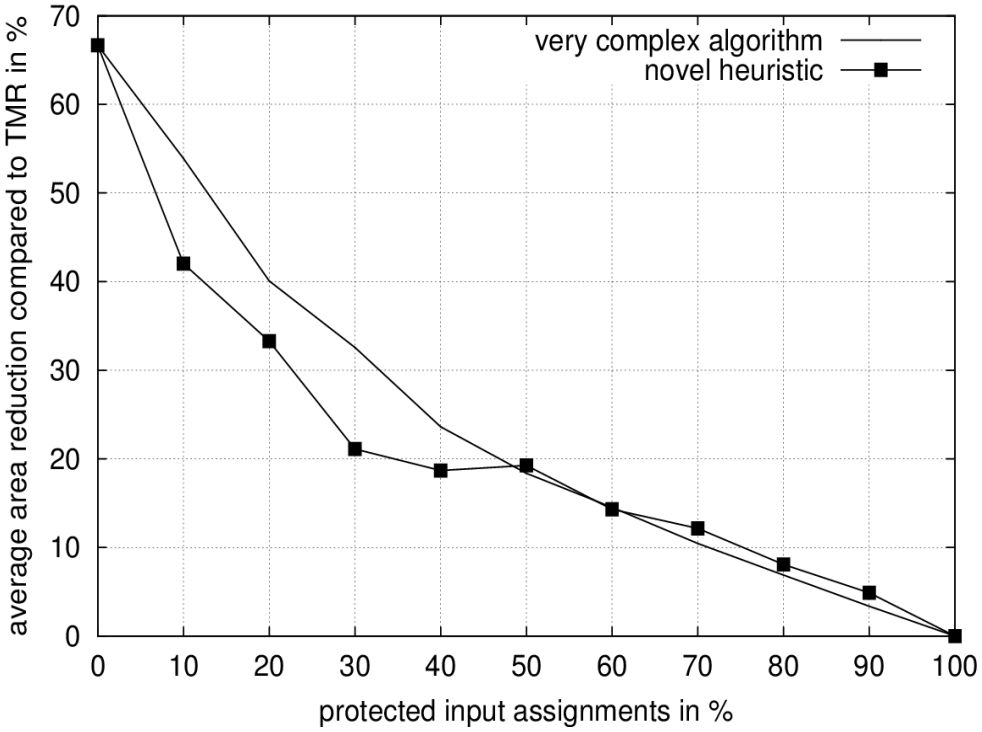
$$s_2(x) = \begin{cases} S_1(x) & \text{if input is critical} \\ 0 & \text{otherwise} \end{cases} \longrightarrow \text{optimize } s_2$$

$$s_3(x) = \begin{cases} S_1(x) & \text{if input is critical} \\ 1 & \text{otherwise} \end{cases} \longrightarrow \text{optimize } s_3$$

*Reducing the Area Overhead of TMR-Systems by Protecting Specific Signals, M. Augustin, M. Gössel, R. Kraemer, Proc. IEEE IOLTS 2010
*Eine neue Fehlertoleranzmethode zur Verringerung des Flächenaufwandes von TMR-Systemen, M. Augustin, M. Gössel, R. Kraemer, Proc. ZuE 2010

Improvements of Selective Fault Tolerance

- Methodology could be easily integrated in standard design flow
  - Selective Fault Tolerance applicable to real industrial designs
- The reduction of area overhead compared to TMR is significant
  - Near to the computationally very intensive solution
- The protection of 20% of all possible input/output assignments leads to an area reduction of one complete system compared to TMR



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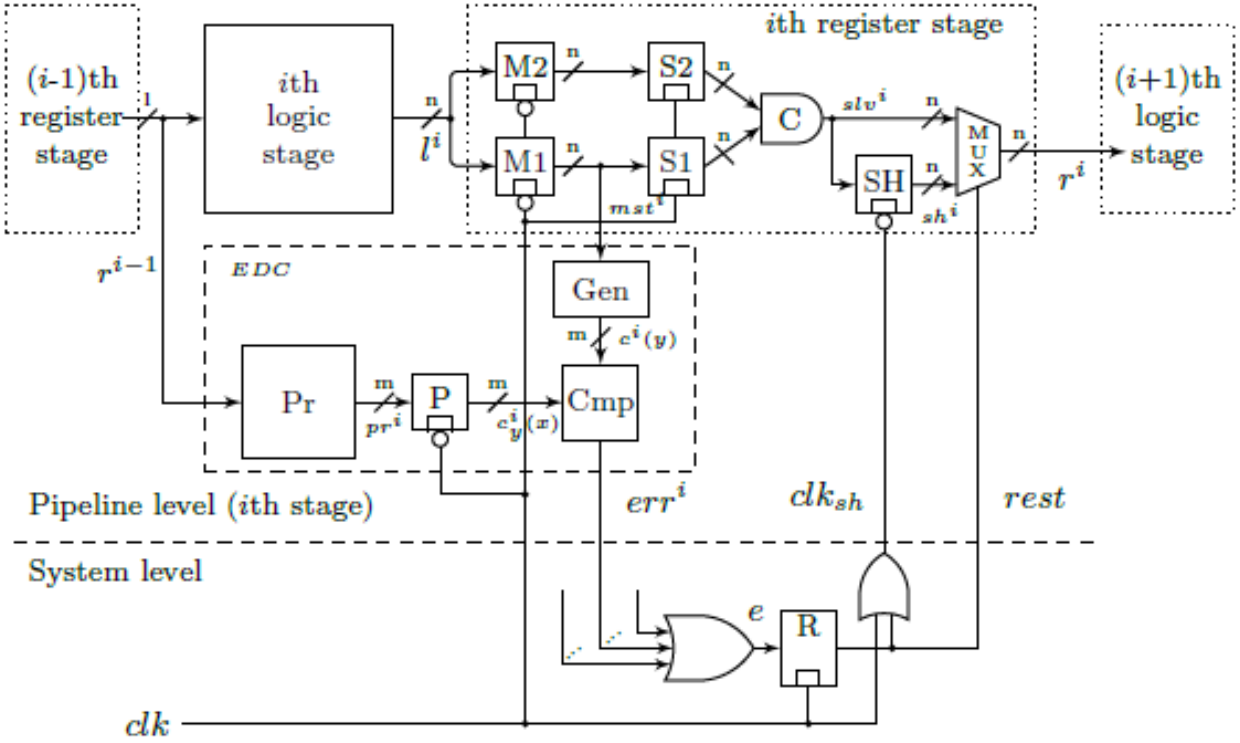
Full Error Detection and Correction (FEDC)



Focused on full error correction

- All injected SETs could be corrected
- Suitable for long transients as well
- Effective against timing errors

Hardware/power overhead reduced compared with TMR

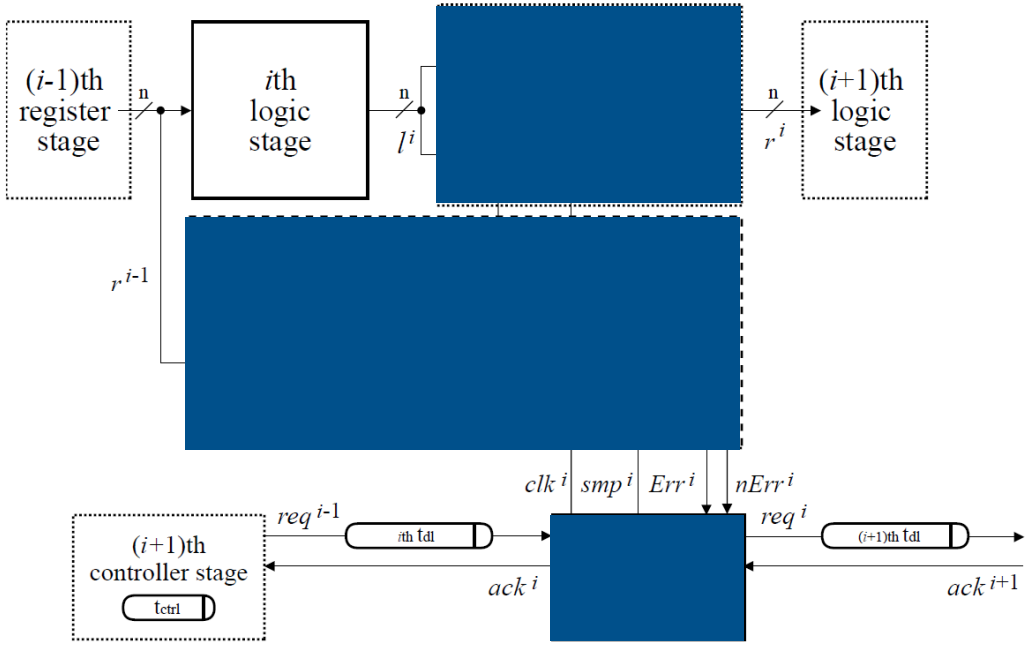
- Saves around 28% power

Circuit	Dynamic Power [mW]	Area Comb [mm2]	Area Sequential [mm2]	Area Total [mm2]
TMR	0,600	0,0421	0,0125	0,0470
FEDC	0,432	0,035	0,0126	0,0418

Milos Krstic, et al., Enhanced Architectures for Soft Error Detection and Correction in Combinational and Sequential Circuits, Microelectronics Reliability, 2016

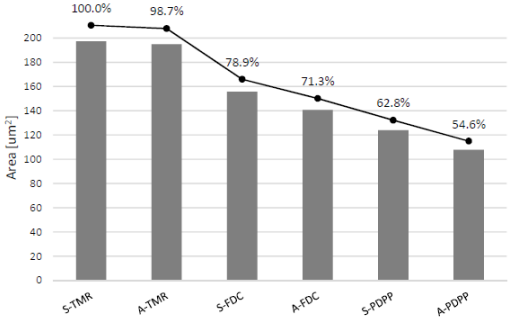
Asynchronous Full Error Detection and Correction - AFEDC

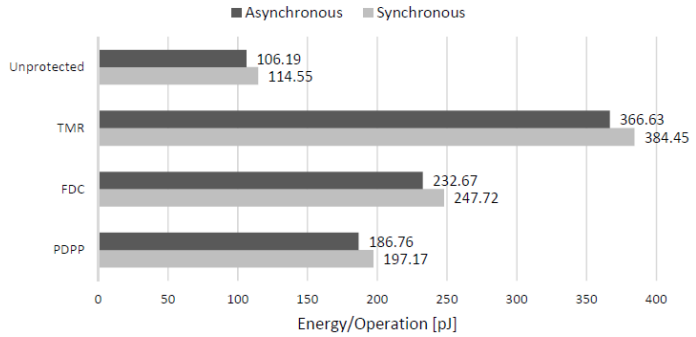
- Soft error resilient stage
  - Latch-based register
    - Dual Modular Redundant - DMR
    - C-element as voter
  - Bundled-data controller
    - 2-phase protocol
    - Click design
  - Error Detection Circuit - EDC
    - Partial Duplication with Parity Prediction
    - Full Duplication and Correction - FDC
    - Q-Flop - QF



PNA-DIVIDER FAULT COMPARISON.

Circuit	Injected faults	Flagged faults	Not corrected SETs	
			No. of not corrected SETs	%
S-Unprotected	14885	350	350	100%
A-Unprotected	15190	389	389	100%
S-TMR	45128	24996	0	0%
A-TMR	46088	25424	0	0%
FEDC-FDC	29917	1047	0	0%
AFEDC-FDC	30821	1140	0	0%
FEDC-PDPP	22609	766	135	17.62%
AFEDC-PDPP	23333	692	363	52.46%





F. Kuentzer, M. Krstic, Soft Error Detection and Correction Architecture for Asynchronous Bundled Data Designs, IEEE Transactions on Circuits and Systems I: Regular Papers – TCAS-I, 2020

Dynamic Methods

Dynamic Methods on the MPSoCs Level

Multiprocessors have varying application requirements

- performance
- dependability (fault-tolerance, lifetime, …)
- power consumption

E.g. Earth observation satellite

- image processing
- orbit change
- waiting new task

- Target: NMR mechanisms, lifetime aspect
  - Self-repairable system based on configurable micro-operation units, selected by the programmer
  - Timing-critical applications are also considered
  - Dynamically adapting to the application requirements
  - Trade-offs between higher endurance, fault-tolerance, performance and power efficiency

A. Simevski, R. Kraemer, M. Krstic, Investigating Core-Level N-Modular Redundancy in Multiprocessors, IEEE MCSoC-14

Architectural Framework for Adaptable Multiprocessors

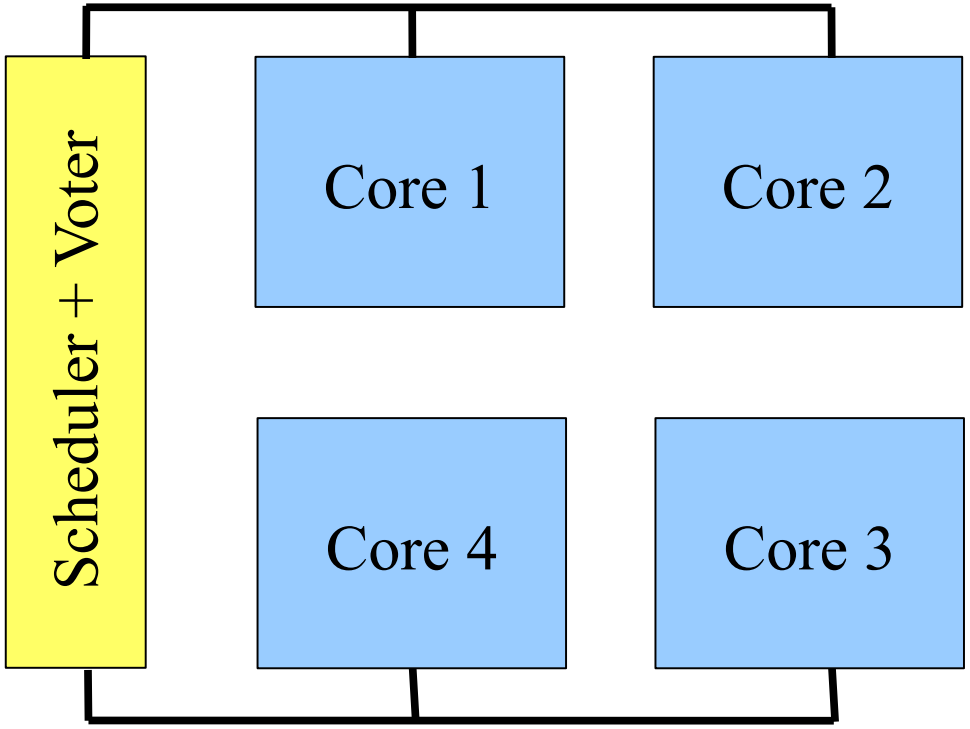
Framework addressing fault-tolerance and aging effects for space and automotive applications

- Aging monitors
- Automated HW/SW verification, design & test
- Programmable NMR voters

Modes of operation

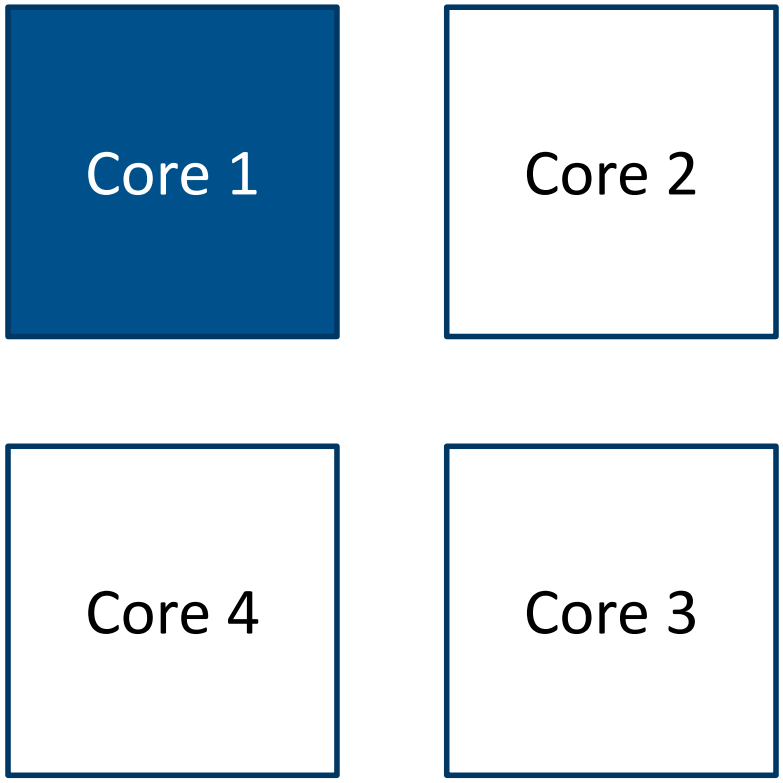
- De-stress
- Fault-tolerant
- High-performance

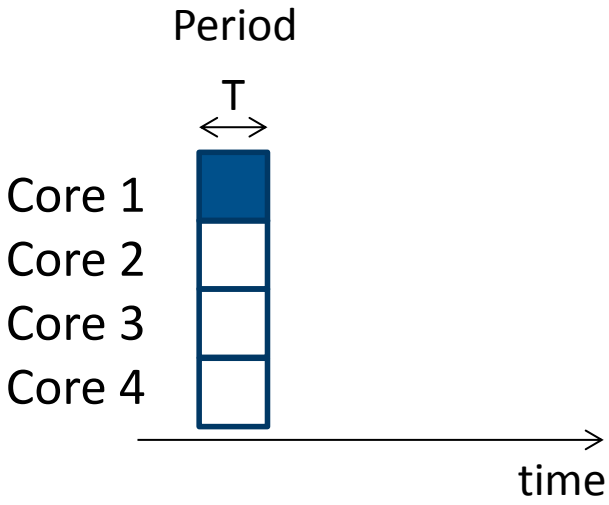
Dynamic mode change depending on the application requirements



A. Simevski, R. Kraemer, M. Krstic, Investigating Core-Level N-Modular Redundancy in Multiprocessors, IEEE MCSoC-14

De-stress mode



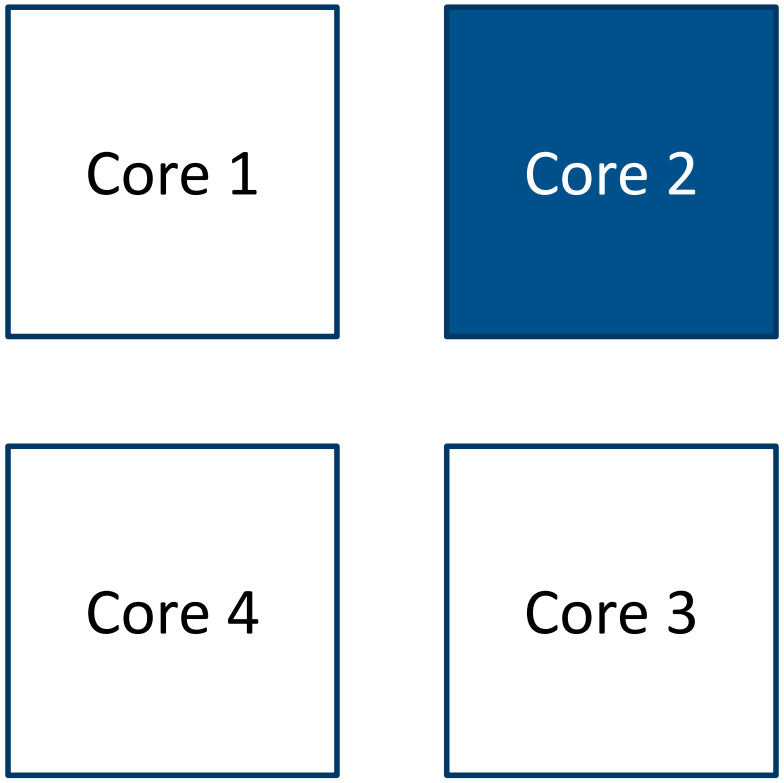


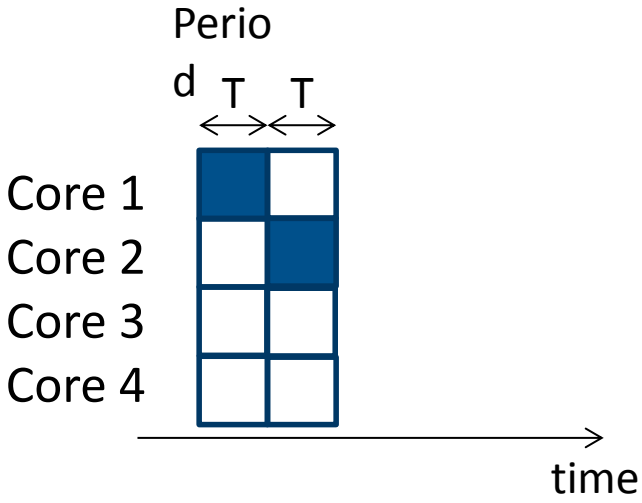
Legend:

= active core

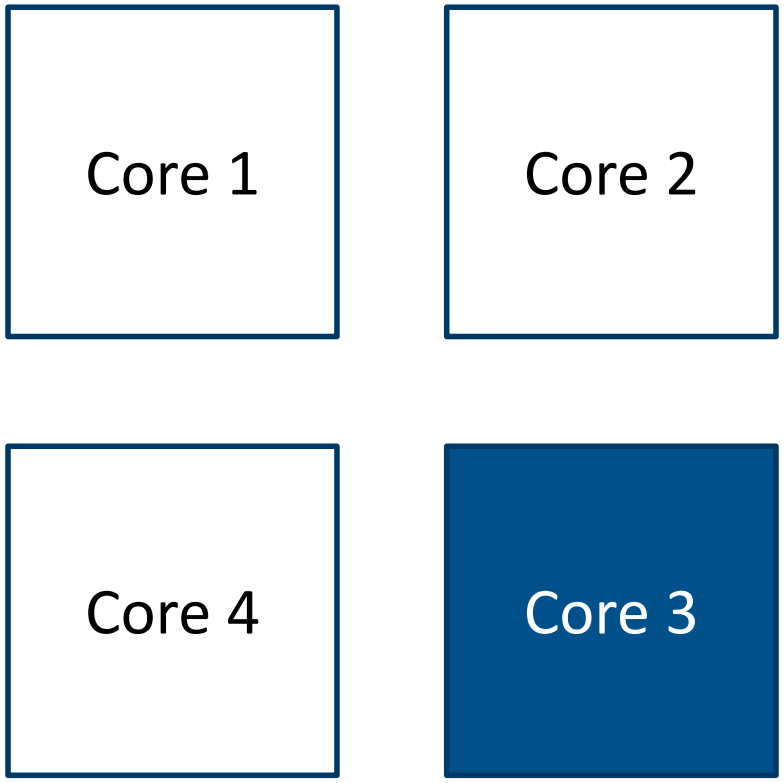
= inactive core

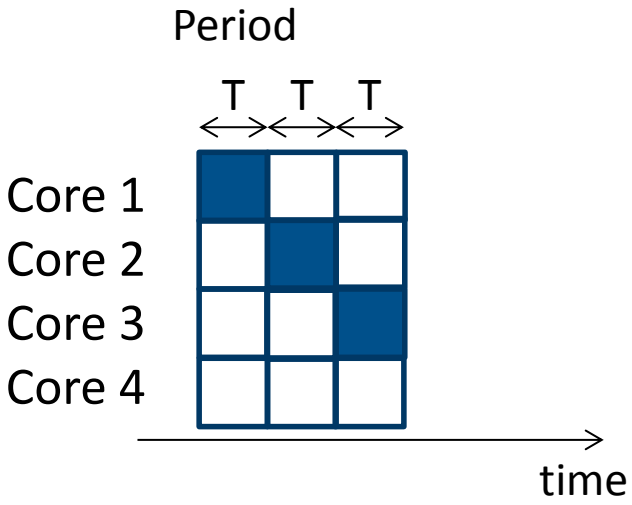
De-stress mode



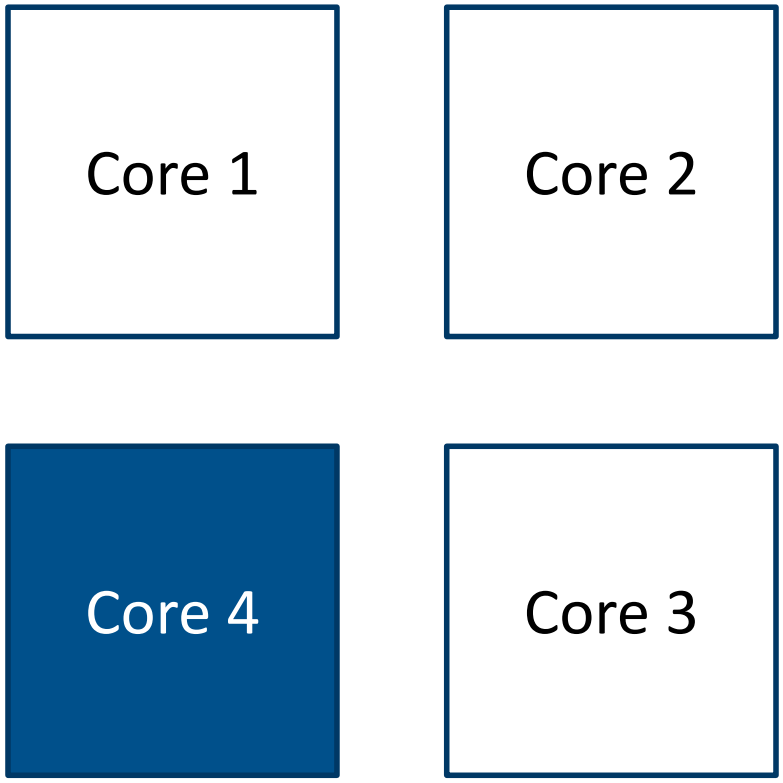


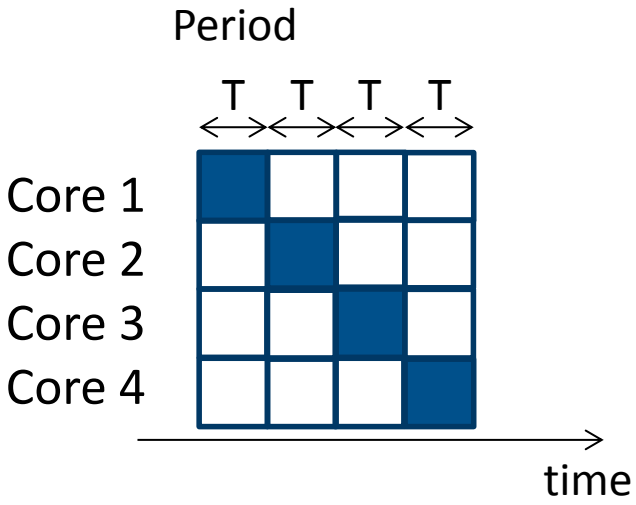
De-stress mode



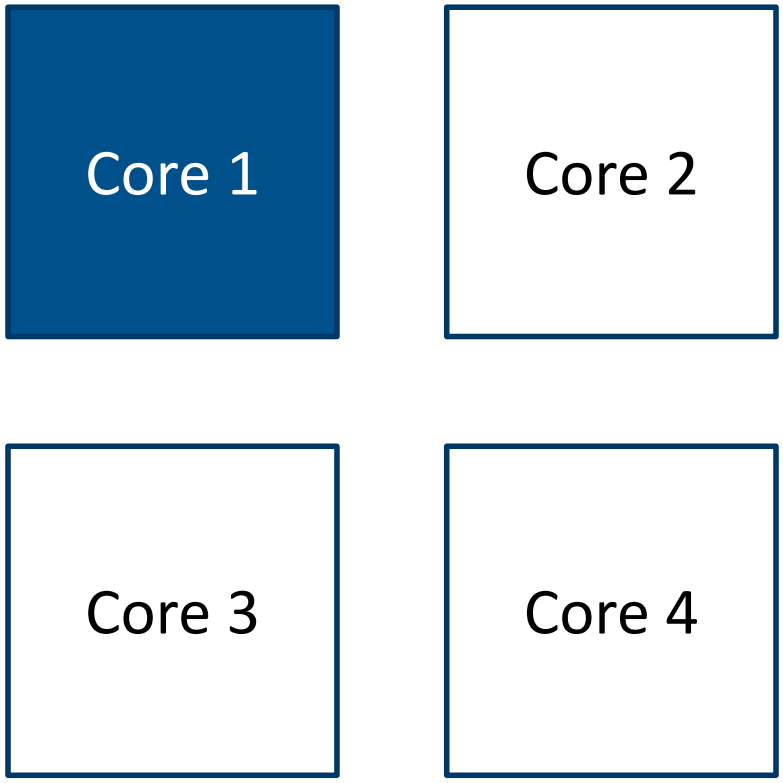


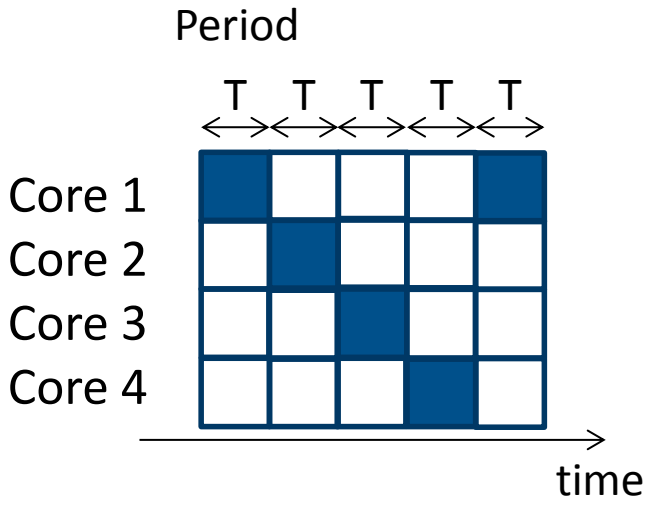
De-stress mode



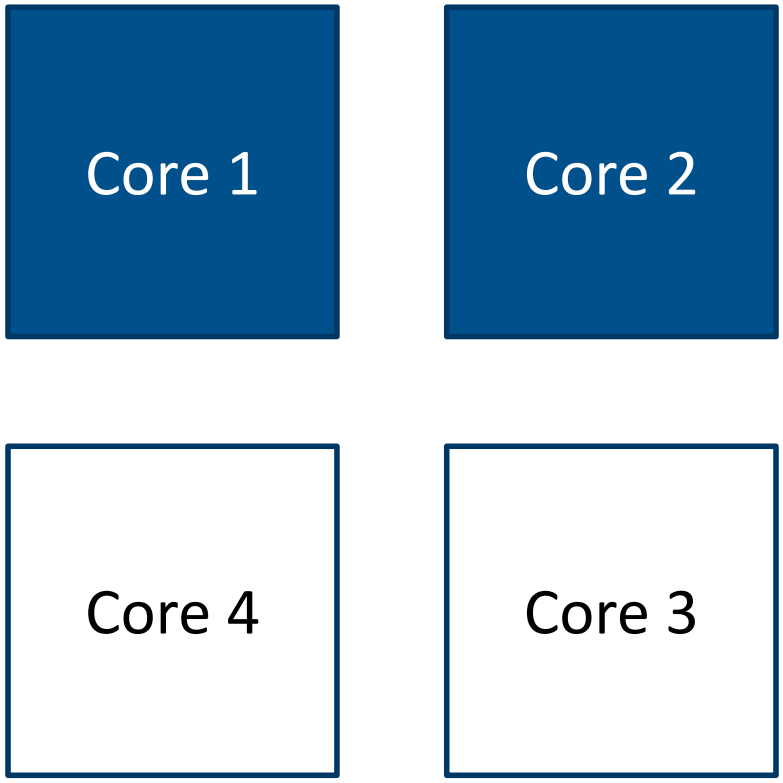


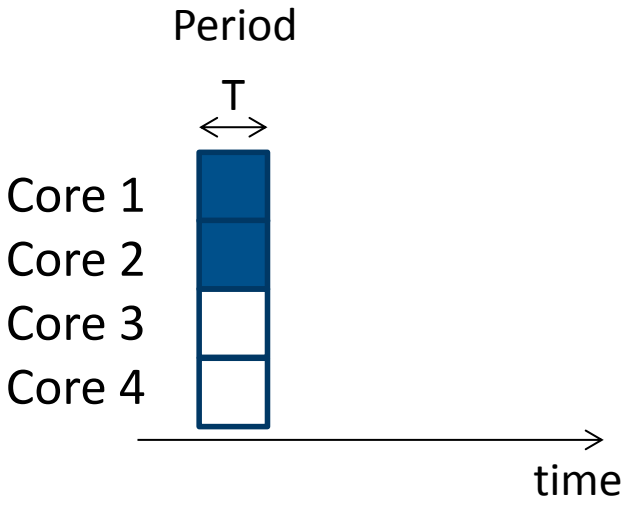
De-stress mode





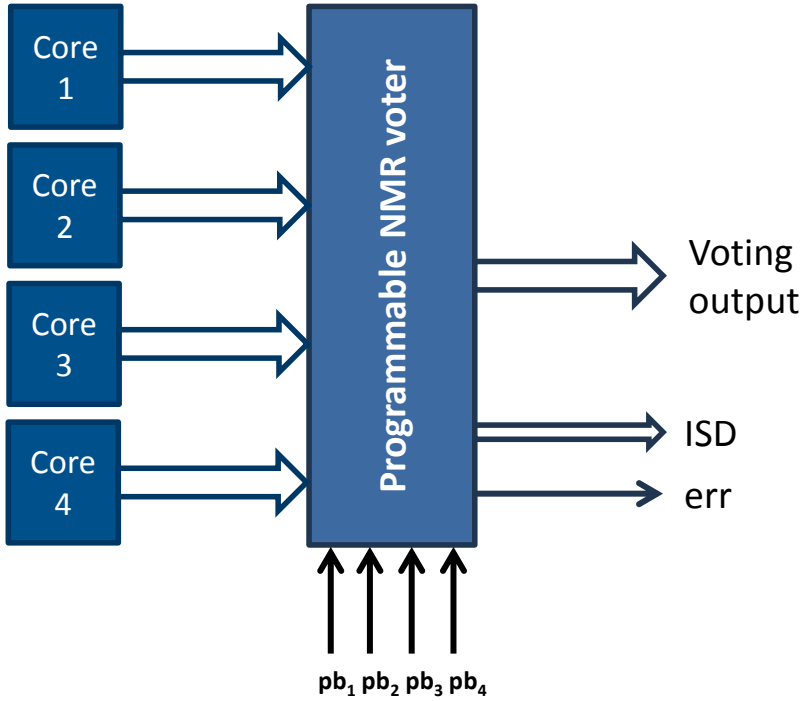
De-stress mode (2 active cores)





Fault-tolerant mode

- Core-level NMR – voting in each clock cycle !
- Masking faults, no need for instant recoveries for N>2
- Dynamic reconfiguration – NMR on-demand

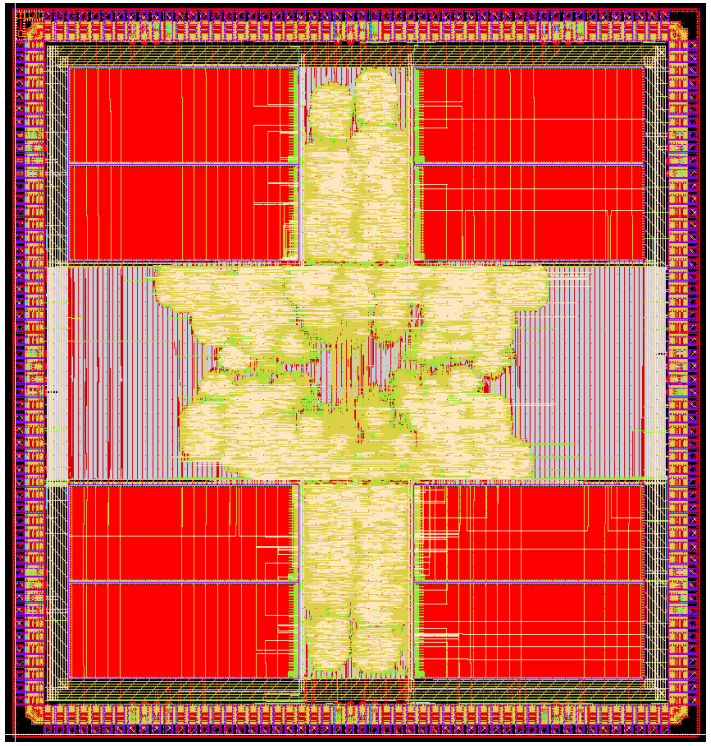


Implementation and Results

Test ASIC named FMP implemented and tested

- 8-core system based on 32-bit internal processor
- Fully functional in IHP 130 nm technology

- Youngest-First Scheduling Methodology (YFSM) could increase the system lifetime up to 31%



A. Simevski, R. Kraemer, M. Krstic, Investigating Core-Level N-Modular Redundancy in Multiprocessors, IEEE MCSoC-14

Resilience methods

What is Resilience?

Resilience - „an ability to recover from or adjust easily to change” (Merriam-Webster)

What can be this change in our digital systems?

Environmental changes:

- Voltage/Temperature variations
- External effects (Radiation (SEEs))
- Ageing and manufacturing issues
- Security threats (side channel attacks)

- We need some measures to address those changes

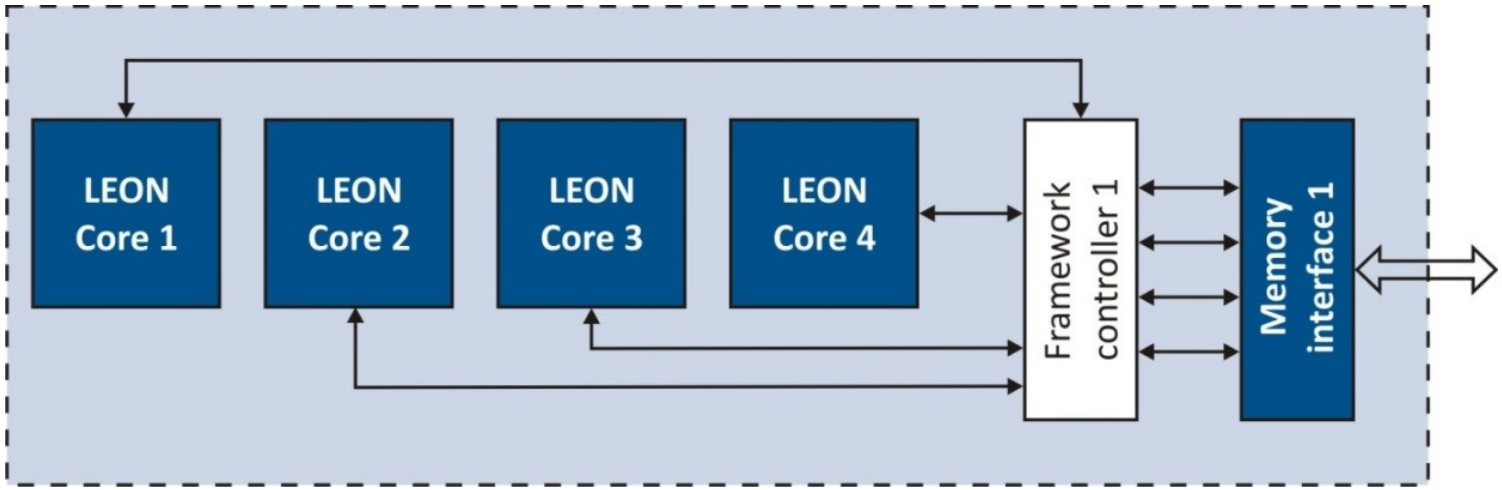
- We already know that addressing faults will cause some overhead
  - However, addressing the other aspects also leads to overhead
  - Example: Supply management unit and its overhead

- Synergy needed in addressing those challenges!
  - In this way the **optimization of the overhead** need to be performed

Example: PISA System
Power robust IC design for Space Applications

- Leon-based multiprocessor using IHP's framework
  - De-stress (Power Gating, Clock Gating, Adaptive Voltage Scaling)
  - Fault-tolerant (Core-level NMR-on-Demand, ECC)
  - High-performance

  - Addressing at the same time
    - Soft errors induced by particle hits
    - Voltage variation induced errors



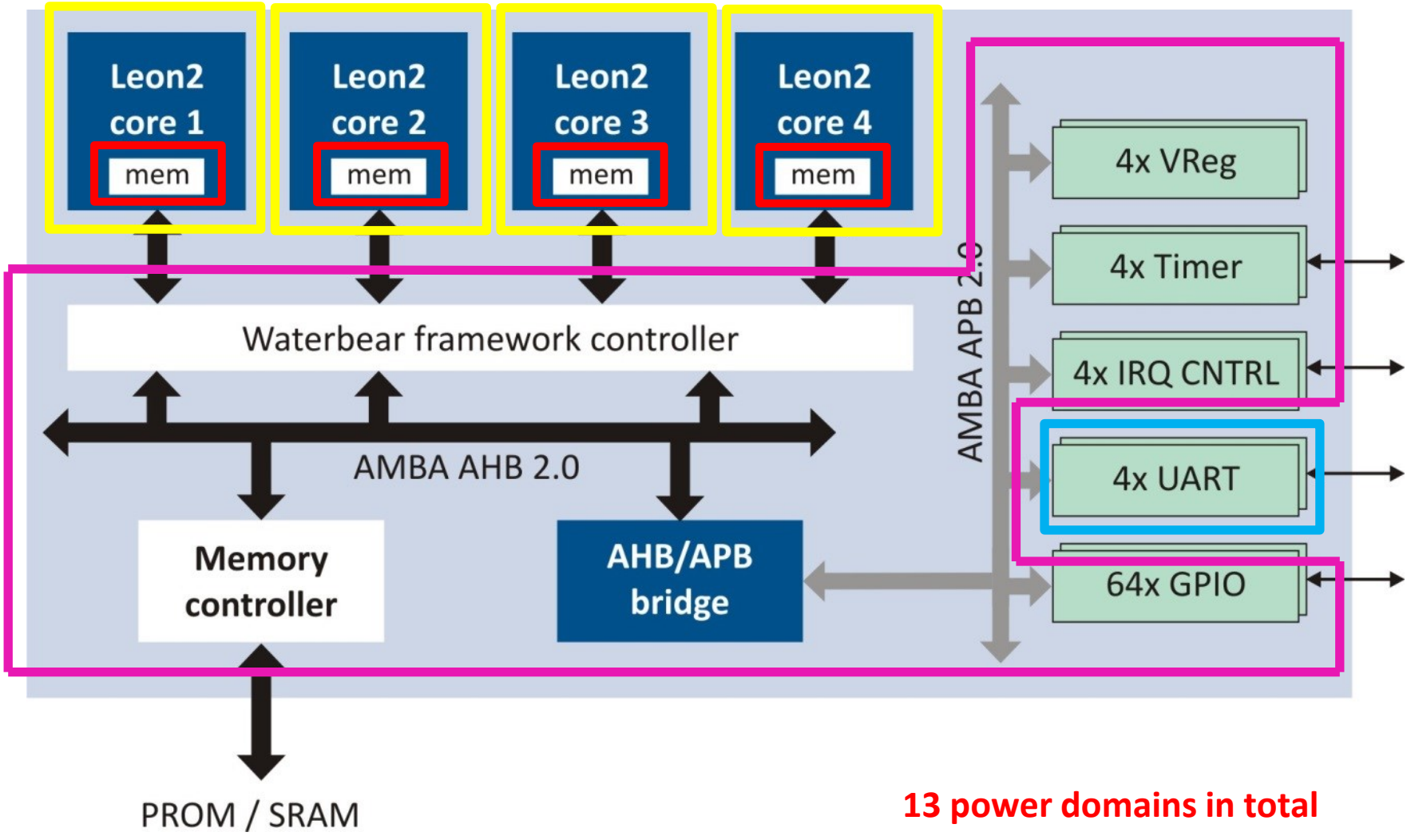
Waterbear framework controller

- Waterbear framework controller
  - Power management
  - Clock management
  - Framework control (e.g., modes: de-stress, fault-tolerant, hi-performance)
  - Error management (both from fault-tolerant mode and ECC)
  - Aging observation and control (aging monitors)
  - Temperature sensors
  - Other management functions (AHB priority, SRAM enable/disable, …)

  - **Synergetic integration of the different fault detection and correction mechanisms**
  - **Overhead optimization**

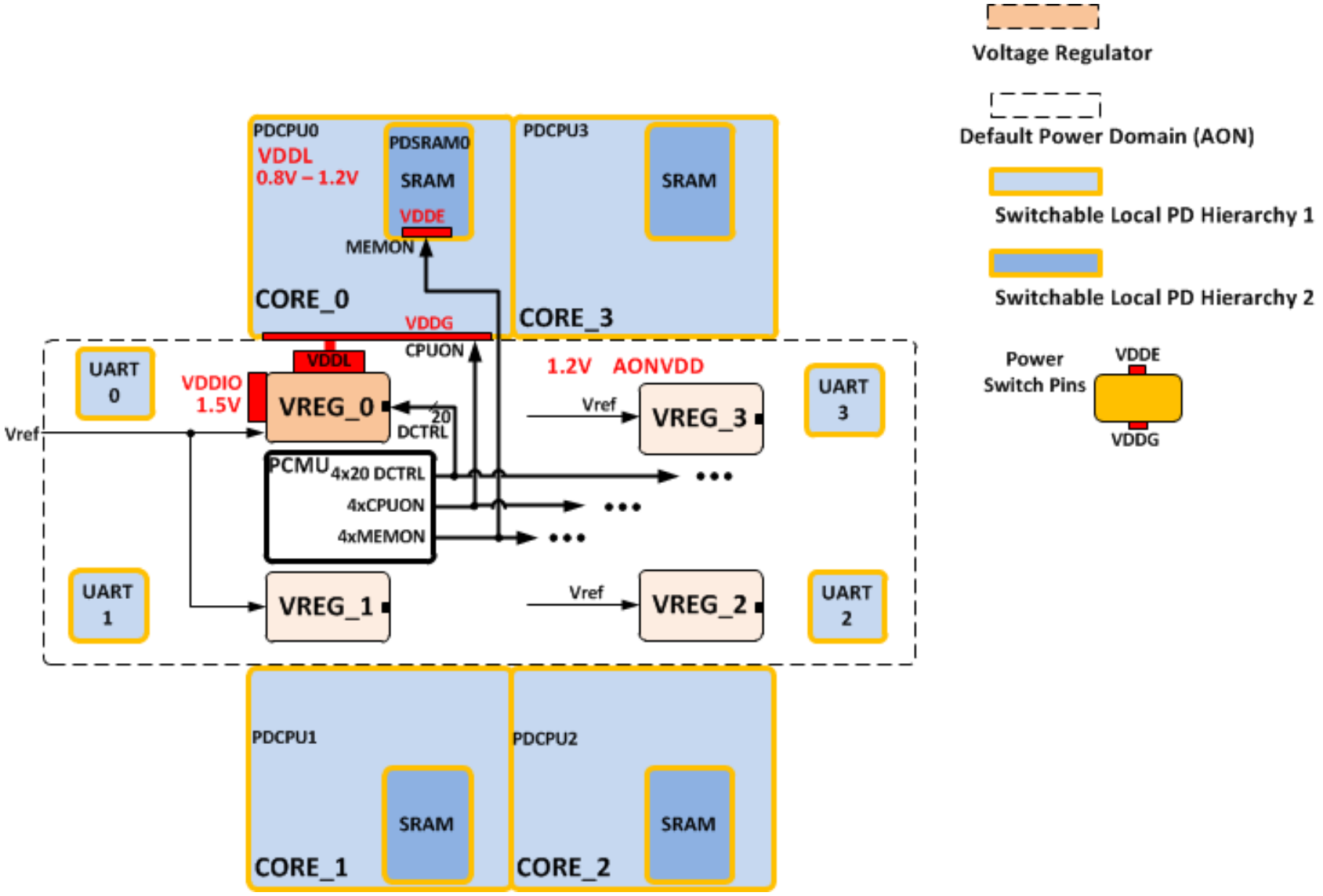
Target chip – power domains

Each core powered by own Voltage Regulator

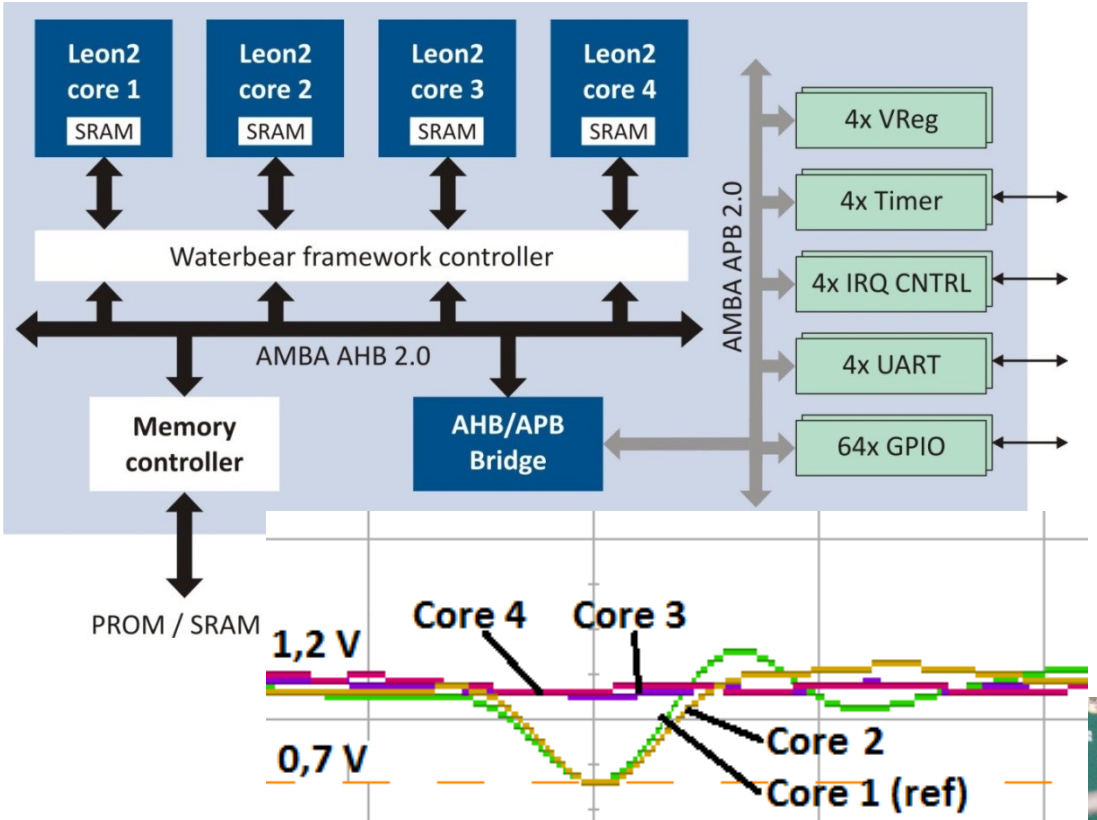


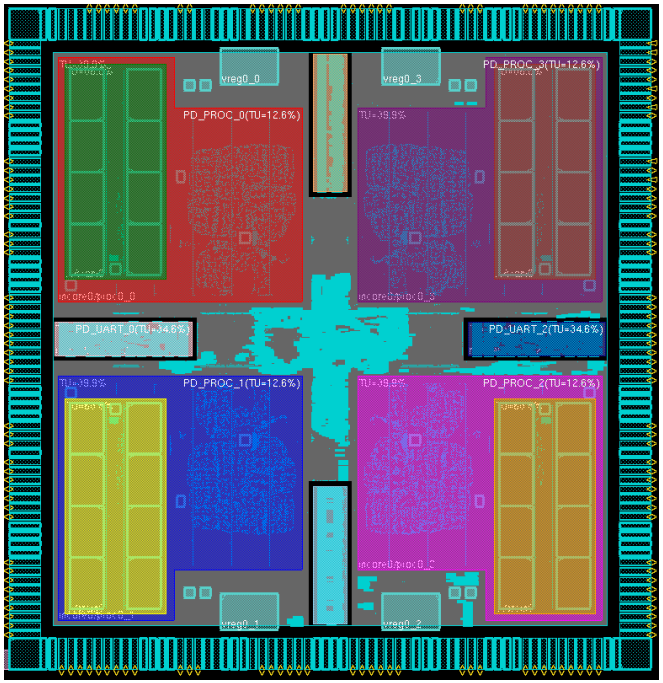
13 power domains in total

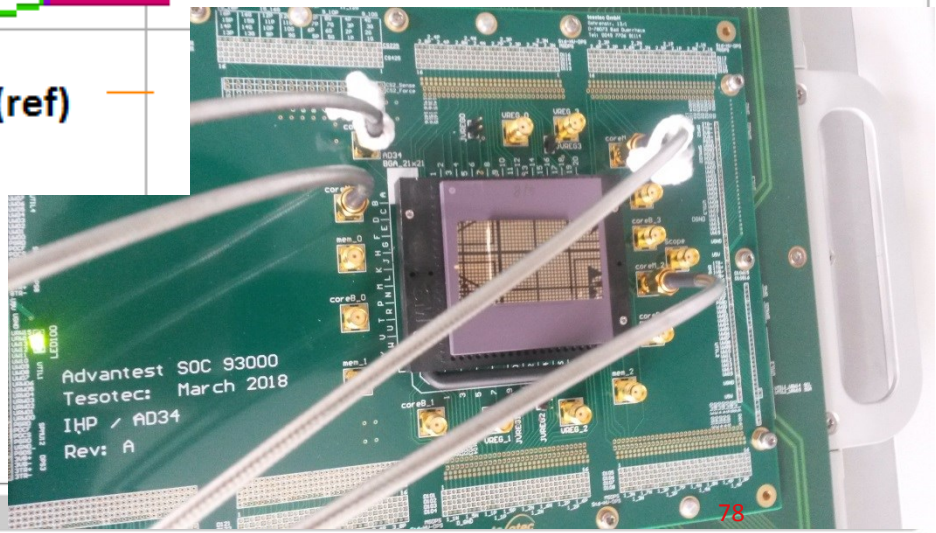
Power domains on Chip



PISA IC – Error Resilient Multi-Processor Chip







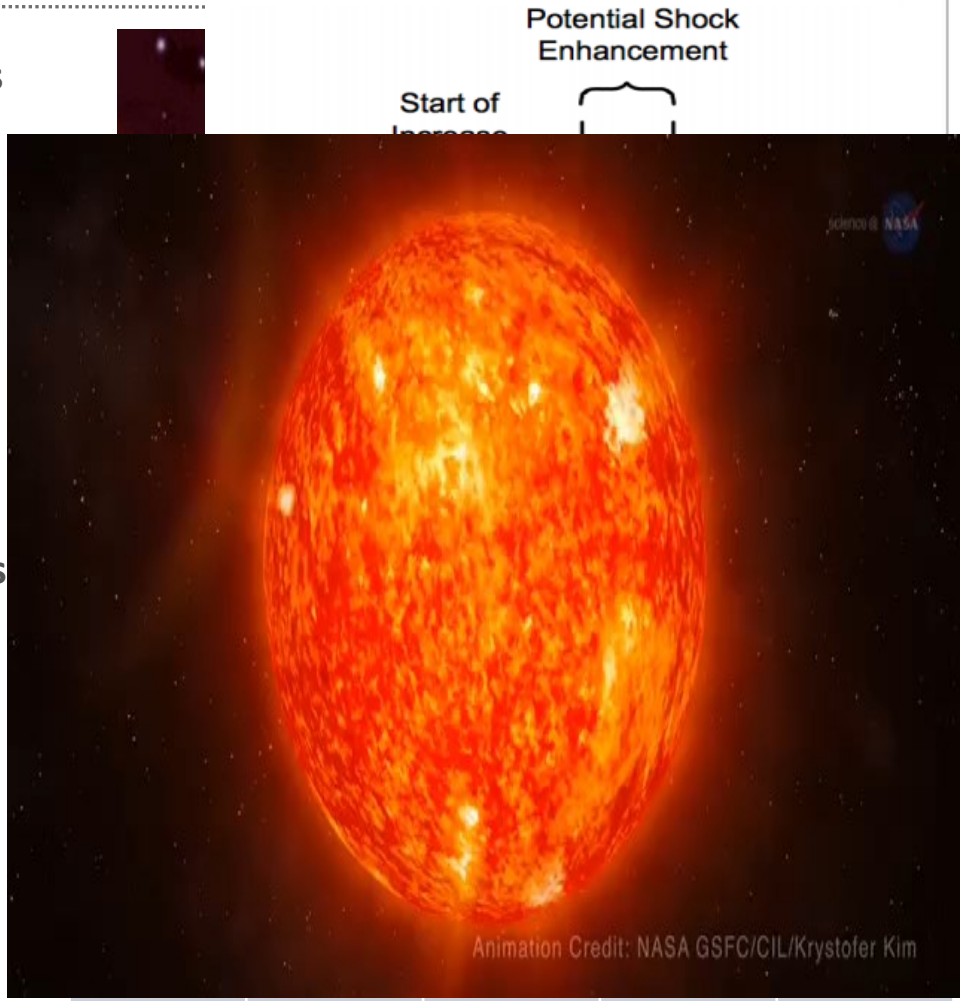
- 4-core Leon2 multiprocessor in 130 nm IHP process
- Exploring CAD tool for obtaining robust power grid
- AVS (Adaptive Voltage Scaling) capability
- Radhard library, Power Management Flow
- ~50 mm^2, 300mW @ 50 MHz (tape-out: Aug. 2017)
- Fully functionally validated in Apr./Mai 2018

Intelligent Sensing: Background

- **Two main groups of space radiation particles**
  1) Trapped by planetary magnetospheres (e.g. Van Allen belt in earth)
  2) Transient radiation particles:
     - Galactic Cosmic Rays (GCRs)
     - Solar Particle Events (SPEs)

- **Real-time SEU rate monitoring & prediction is vital in space applications**

  Dominate the radiation environment

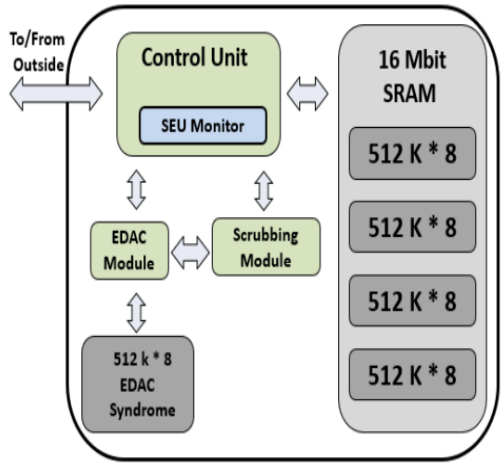


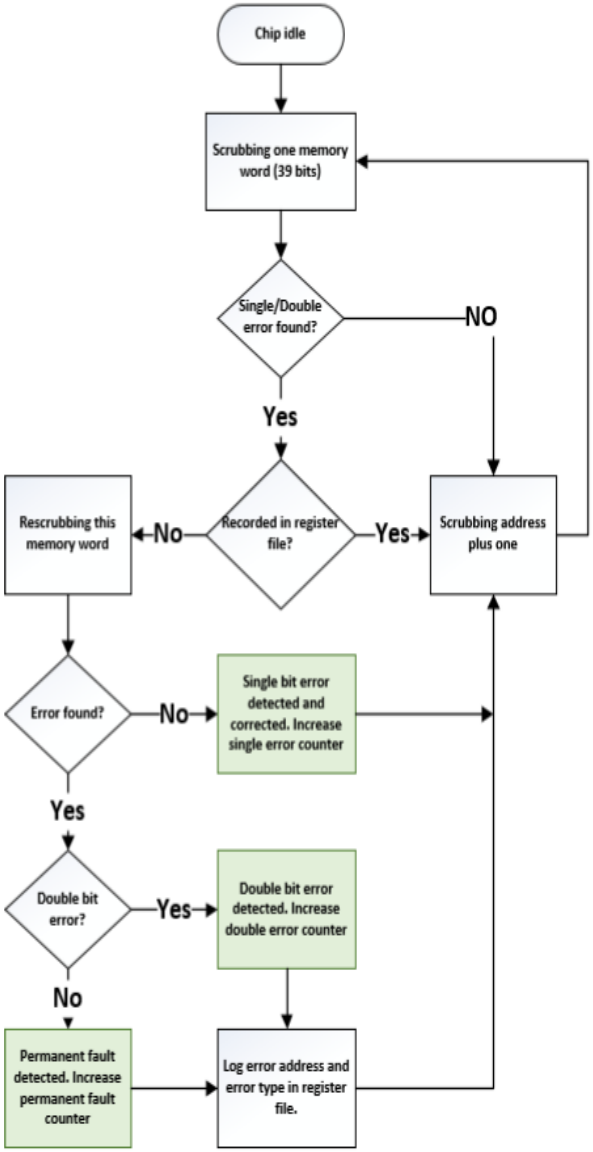
Oct 28,2003	$4.4*10^{-8}$	$2.1*10^{-7}$	$6.1*10^{-7}$	$2.5*10^{-5}$
Jan 20,2005	$8.1*10^{-8}$	$2.3*10^{-7}$	$6.5*10^{-7}$	$2.4*10^{-5}$

SEU rate (upsets/(bit*day)) of a 0.25-um SRAM during 4 large SPEs

Embedded Single Event Upsets (SEUs) Monitor

- Counting SEUs on SRAM, detect permanent faults in memory cells and classify the radiation level
- EDAC (HSIAO (39,32) code), Scrubbing
- Non-standalone SEU monitor
- Combining the SEU monitoring and data storage functions in the same SRAM module
- Negligible cost and overheads (< 1%)

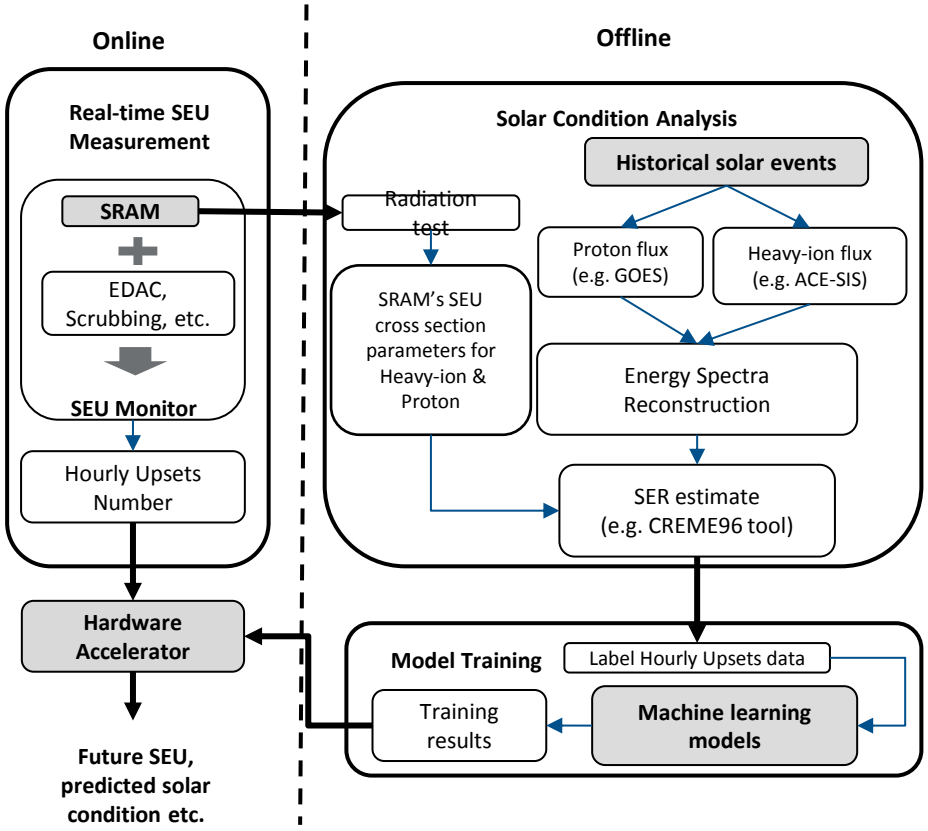


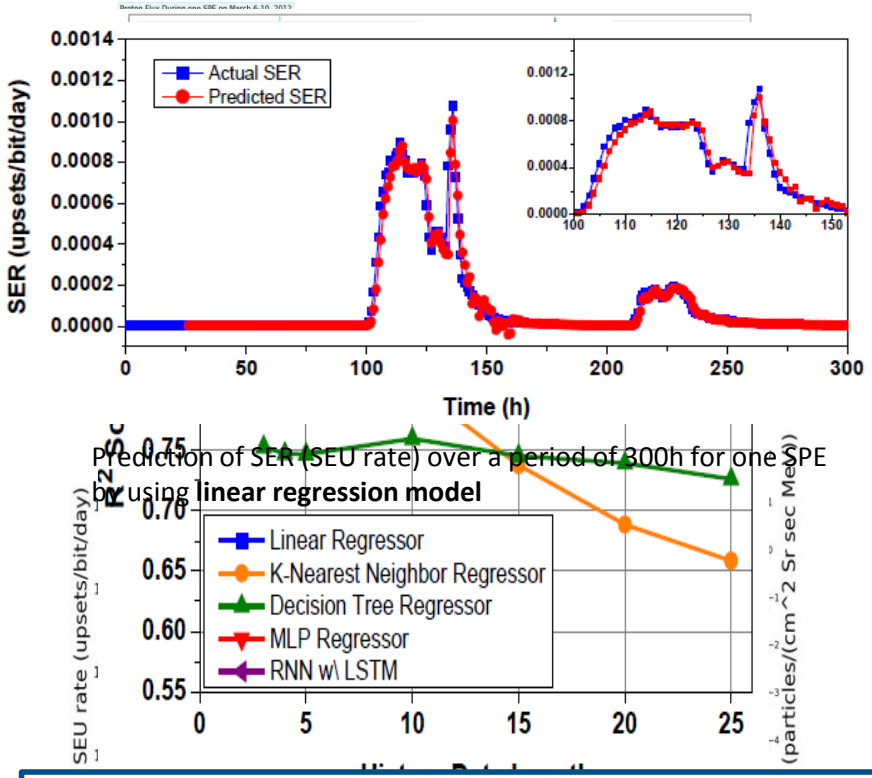


J. Chen, M. Andjelkovic, A. Simevski, Y. Li, P. Skoncej and **M. Krstic**, Design of SRAM-based Low-Cost SEU Monitor for Self-Adaptive Multiprocessing Systems, EUROMICRO Digital System Design Conference (DSD 2019)

Data Analysis – Solar Particle Events (SPEs) Prediction

- Embedded approach for the prediction of SPEs by forecasting in-flight SRAM SERs in space applications
- Combining the SEU monitor, publicly available flux databases and the offline trained machine learning model
- Predicting the SRAM SEU rate one hour in advance and fine-grained hourly tracking of SEU rate variations during SPEs as well as under normal conditions



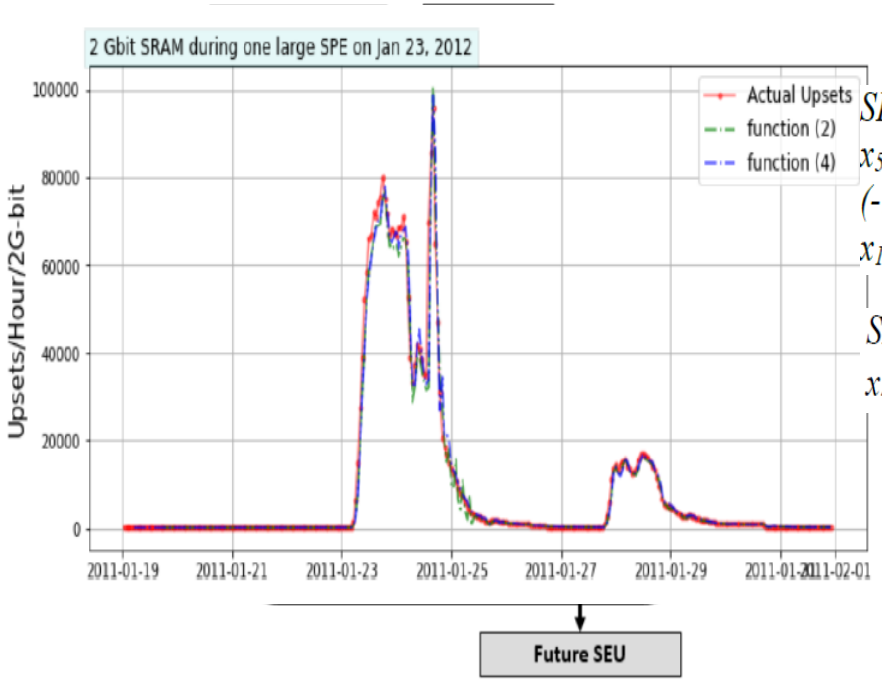


Prediction of SER (SEU rate) over a period of 300h for one SPE by using **linear regression model**

J. Chen, T. Lange, M. Andjelkovic, A. Simevski, M. Krstic, Prediction of Solar Particle Events with SRAM-Based Soft Error Rate Monitor and Supervised Machine Learning, Microelectronics Reliability and ESREF 2020

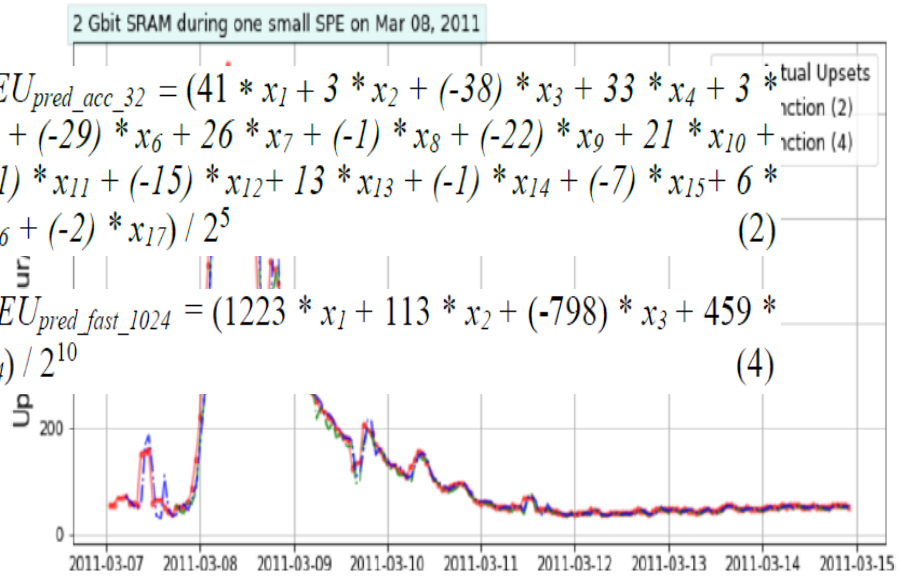
Intelligent Decision Making: Hardware Accelerator Design

- Hardware accelerator for forecasting the in-flight SEU variation
- Implemented the linear regression model as the hardware accelerator with a negligible cost
- Predict the increased radiation levels minimizes the risk that the target system will be exposed to harsh conditions without being sufficiently protected



$$SEU_{pred\_acc\_32} = (41 * x_1 + 3 * x_2 + (-38) * x_3 + 33 * x_4 + 3 * x_5 + (-29) * x_6 + 26 * x_7 + (-1) * x_8 + (-22) * x_9 + 21 * x_{10} + (-1) * x_{11} + (-15) * x_{12} + 13 * x_{13} + (-1) * x_{14} + (-7) * x_{15} + 6 * x_{16} + (-2) * x_{17}) / 2^5 \quad (2)$$

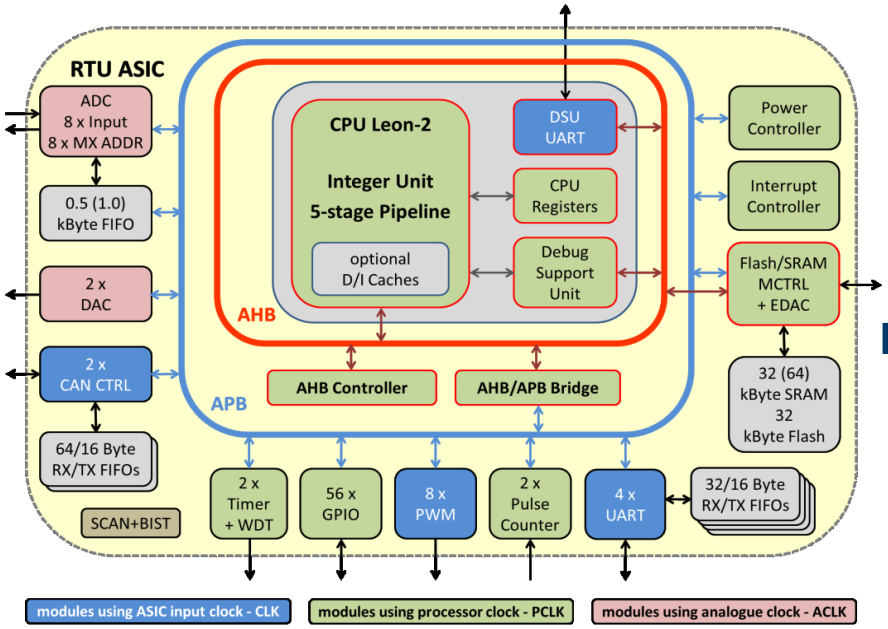
$$SEU_{pred\_fast\_1024} = (1223 * x_1 + 113 * x_2 + (-798) * x_3 + 459 * x_4) / 2^{10} \quad (4)$$

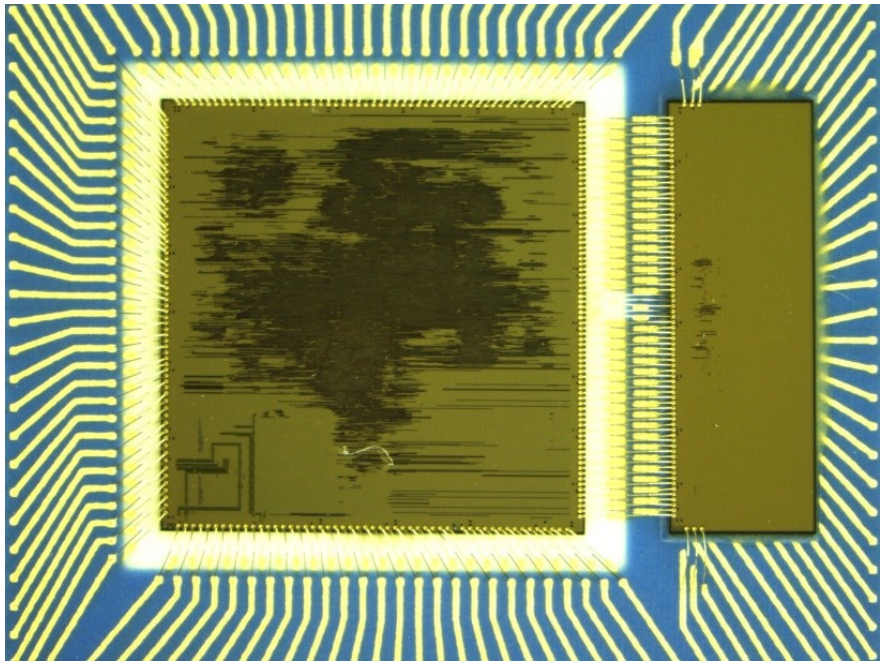


J. Chen, T. Lange, M. Andjelkovic, A. Simevski, M. Krstic, Hardware Accelerator Design with Supervised Machine Learning for Solar Particle Event Prediction, 33rd IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 2020, accepted paper

Example Space ASICs: Development of the RTU ASIC Chip

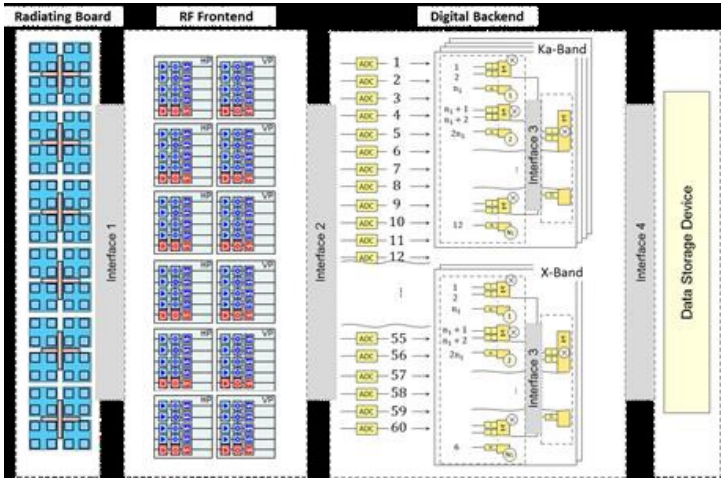
- Remote Terminal Unit ASIC under development for small satellite applications
- Complex mixed-signal dual-chip in package solution
- Target technology – internal 0.25 um CMOS
- Tape out Feb 2015 – fully functional confirmed measurements!
- Radiation hardness based on radhard TMR library of flip-flops
  - TMR approach compatible to the standard design flow



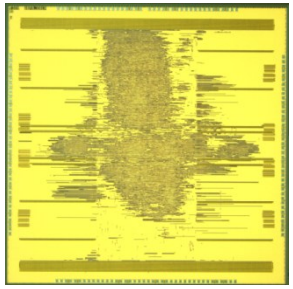


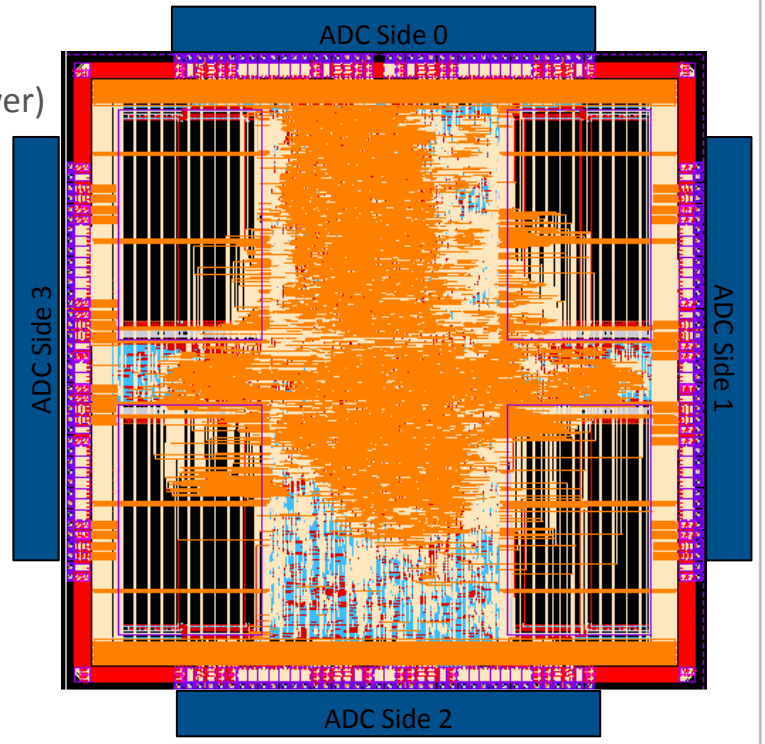
Example Space ASICs:
DBFN Baseband Processor for Synthetic Aperture Radar

- The DIFFERENT project tackles the development of low-cost highly-integrated compact radar for formation flying multistatic SAR applications.
- IHP is designing DFBN baseband chip in SGB25V technology
  - This chip includes high-speed processing and IO interfaces
- Fabrication of digital baseband IC and RF MMICs in IHP technologies
  - DFBN Chip tape-out Aug 2015 – 46 mm2 in SGB25V
  - Tested on wafer and operational up to 250 MHz!
  - Optimized overhead (reduced by 20% in area and 33% in power)
    - radiation hardened flip-flops in control logic
    - Standard flip-flops in datapath



Architecture of RadarModule in DIFFERENT



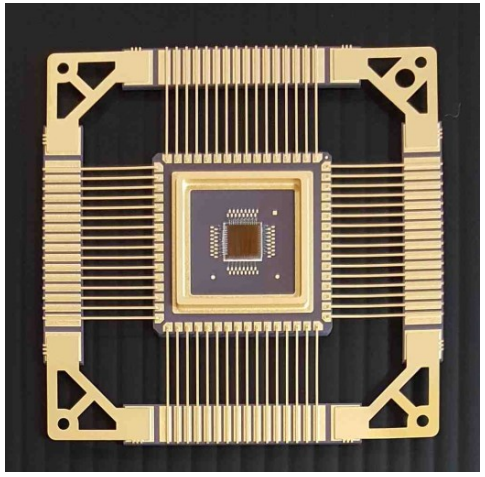


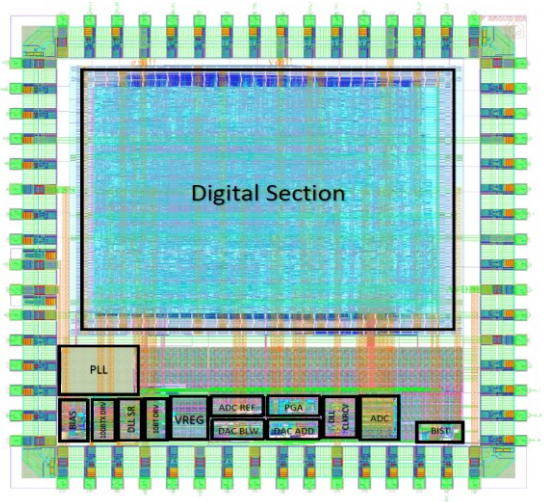
DBFN Baseband Processor - 46mm² in SGB25V, Sep 2015

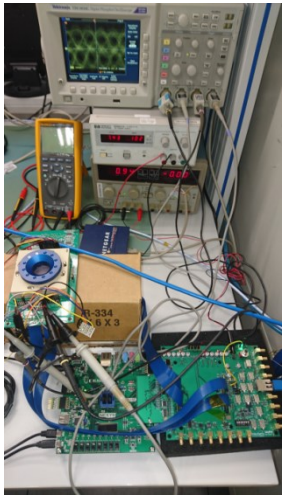
Example Space ASICs:
EU Project SEPHY – Space Ethernet Physical Layer Transceiver

- Radiation hardened 10/100 Ethernet physical layer transceiver for the space market

- SEPHY Chip
  - 150 nm CMOS process, ATMEL radhard PDK
  - IHP responsible for digital IP design and verification
  - **10 BaseT/100BaseTx PHYs fully functional**
  - **Radiation hardness confirmed at the end of 2018**
    - 100 Krad TiD – no effects on BER
    - SEE Tests has shown Mean Time Between Failure (MTBFs) of 940 years
  - **Commercialization steps currently planned with coordinator Arquimea**







Example Space ASICs:
SECHIS - SERDES Chip for Space Applications

Goals

- Development of 1.6-2.5Gbps SERDES IP and corresponding chip for space applications
- First European (ITAR free) implementation of a radiation-hard high-speed SERDES

EUREKA
innovation across borders

Bundesministerium für Bildung und Forschung

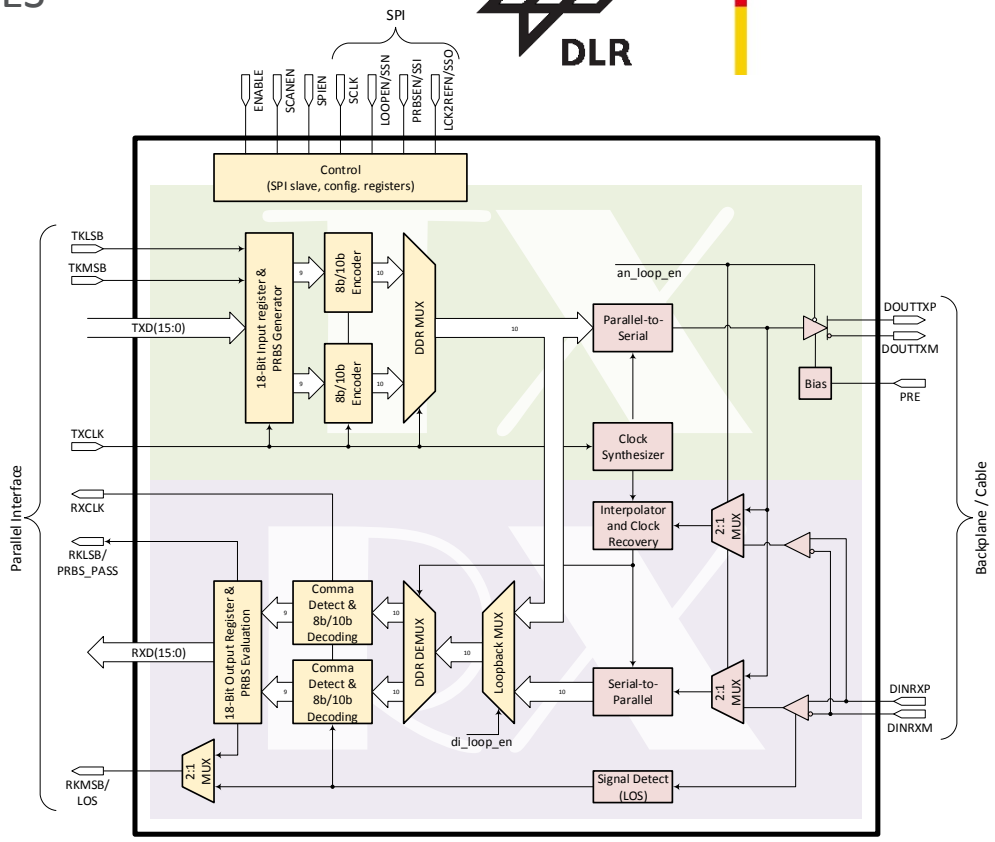
DLR

IHP Tasks

- Digital IP design
- Fabrication & assembly in 130 nm BiCMOS technology of IHP
- Characterization & radiation tests

Challenges

- Combining rad-hard with high-speed design techniques
- High-speed CMOS implementation of 2x 8b/10b-en/decoding and bit-alignment



Example Space ASICs:
SPAD – Development of a SPace-qualified ADC (ProFIT/ILB)

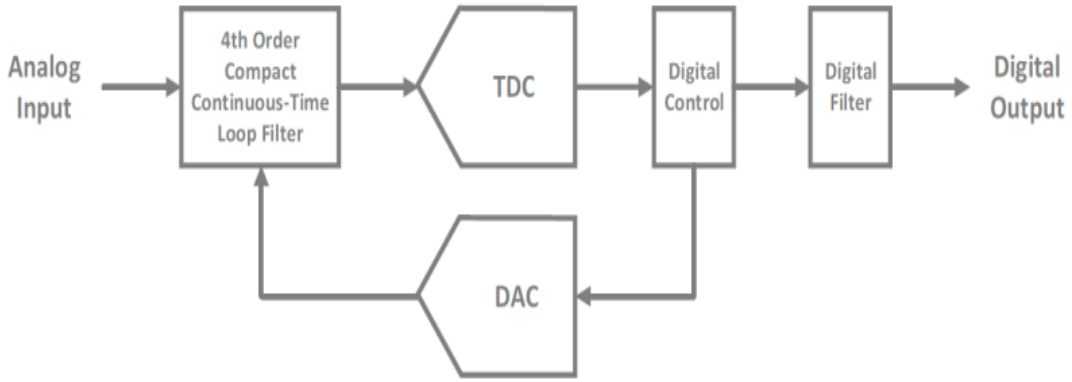
ARQUIMEA
Passion for technology

SPAD's main obective is the development of a radiation-tolerant 14-bit, low-power Analog – to – Digital converter (ADC)

Specification:

- Technology: SG13S, Sampling rate: 10-15 Msps, ENOB 13, APB interface, SPI, System speed: > 125 MHz, Power: < 100 mW
- RH-Robustness: 67 MeV LET (SEU/SEL), 20 MeV LET (SET)

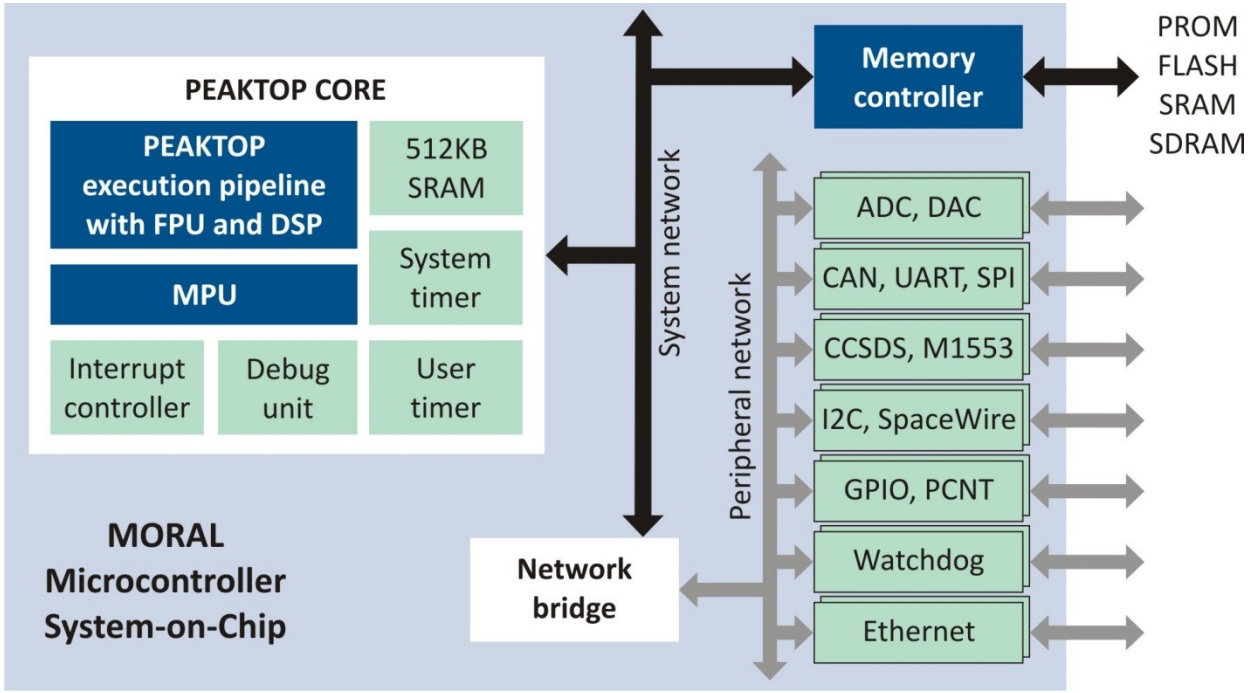
- IHP Responsibilities:
  - RHBD Methodologies ,
  - HDL Development Implementation,
  - Manufacturing
  - Integration, Measurements
  - Radiation-Tests

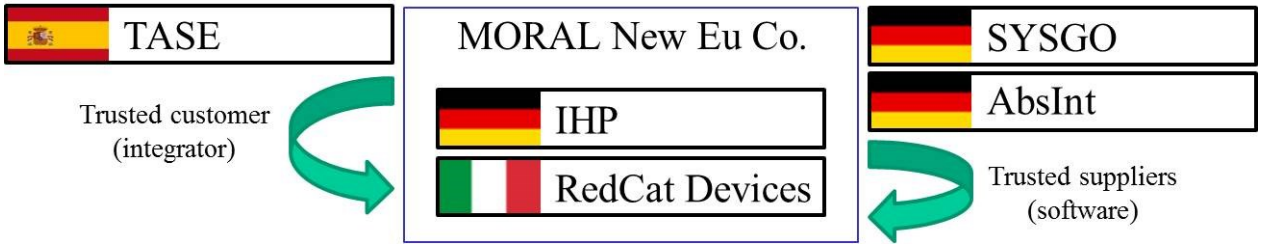


Investitionsbank des Landes Brandenburg ILB
EUROPÄISCHE UNION
Europäischer Fonds für Regionale Entwicklung
www.efre.brandenburg.de

Example Space ASICs:
MORAL - Export-free rad-hard µcontroller for space apps

- Develop a completely European, ITAR-free µcontroller for space apps
- Based on the novel Peaktop architecture (incl. novel ISA)
- Formally-verified C compiler, RTOS and toolchain
- Demonstrator board
- Start-up for selling the microcontroller (and for customer support).





IHP SiGe BiCMOS Technologies for Space Applications

250nm CMOS (V_{DD}=+2.5V ; T_{OX} = 5.8nm)

BEOL : 3 thin + 2 thick metal layers (TM1:2µm, TM2:3µm) + MIM Capacitor Layer

SGB25V
npnVp 95/75/2.4
npnVs 90/40/4.0
npnVh 70/25/7.0

SG25H3
npnVp 180/110/2.3
npnVp 140/120/2.4
npnVs 140/45/5.0
npnVh 80/25/7.0

SG25H1
npnVp 190/190/1.9
npnVp 220/180/1.9
(REPLACED by SG25H4)

SG25H4
npnVp 190/190/1.9
npnVp 220/180/1.9

SGB25RH
npnVp 95/75/2.4
npnVs 90/40/4.0
npnVh 70/25/7.0
EPPL Listed 2018

SG25H_EPIC
SG25H4 + Integrated Photonic

130nm Dual Gate CMOS
(V_{DD}=+1.2V, +3.3V ; T_{OX} = 2nm / 7nm)

BEOL : 5 thin + 2 thick metal layers (TM1:2µm, TM2:3µm) + MIM Capacitor Layer

SG13S
npnVp 340/250/1.7
npnV1 220/180/3.7

SG13G2
npnVp 500/300/1.6

Speed-World-Record
EU-DotFive Project (2009-2012)

SG13RH
npnVp 340/250/1.7
npnVv 220/180/3.7
Under evaluation
Early Access for joint projects

MODULES

-GD
n-LDMOS 18/48/22
p-LDMOS 8/28/-17

-H3P
pnp 120/90/-2.5

-PIC
SI-Photonic Devices
Ge-PD, MZM, etc...

- RFMEMS
Capacitive Switches > 30GHz
IL < 1.0dB / Pull-in ~50V / C_{ON}/C_{OFF} > 10

TSV

LBE

Legend :

Technology
device f_{MAX} / f_T / BV_{CEO}

Stable
Qualified based on JEDEC JP-001
Early Access
In Development
Phased-Out

Status : August 2019

IHP Processes and PDKs for Space Applications

Summary I of III

Status : 2019

	SGB25V/RH	SG13S/RH
■ **Process Description**	SiGe HBTs npn Peak f_T /f_{MAX} 75/95GHz 250nm CMOS (V_{DD}=+2.5V;T_{OX} = 5.8nm)	SiGe HBTs npn Peak f_T /f_{MAX} 220/340GHz 130nm Dual Gate –Oxide CMOS (V_{DD}=+1.2V, +3.3V ; T_{OX} = 2nm / 7nm)
■ **Applications**	Mixed-Signal MMIC/ASICs up to Ku Band	Mixed-Signal MMIC/ASICs up to W-Band
■ **Commercial Qualification** – Based on JEDEC Standard JP001.01 – EPPL/QML/QPL (ESCC QPL, ESCC QML, MIL QPL, JAXA QPL)	**Re-Qualified 2010** **active & stable > 10 years (2005)** **EPPL Listed 2018**	**completed 2014** EPPL under preparation
■ **Radiation Assessment (Analog)** ■ HBT npn (all devices) ■ PMOS ■ NMOS (WG=1µm) ■ ELT-NMOS (RHBD Device)	**completed** PASS TID 800krad(Si) no ELDRS TID > 550krad(Si) PASS TID 100krad(Si) Characterized up to 500krad(Si) TID > 550krad(Si)	**completed** PASS TID >1210krad(Si) no ELDRS TID > 200 (HV) / 500 (LV) krad(Si) PASS TID 50krad(Si) (LV) Characterized up to 500krad(Si) TID > 900krad(Si)

IHP Processes and PDKs for Space Applications

Summary II of III

Status : 2019

	SGB25V/RH	SG13S/RH
■ PDK Availability ■ Access Status	completed NDA/EXPORT License	In development -Early Access NDA/EXPORT License
■ CMOS Std Cell Core and IO Libraries	Dolphin SESAME2-LP core cells + special RHBD cells (IHP) (80 cells) Saphyrion SAGL (25 cells) (Tested for SEU/SEL only)	IHP IXC013RH (~ 90 cells)
■ Radiation Assessment (Digital) ■ TID ■ CMOS Libraries	100krad(Si) – 300krad(Si) SEU/SEL completed SEL Threshold > 65MeV/cm²/mg (RHBD IHP cells) SEU Threshold > 30MeV/cm²/mg (IHP RTMR FF)	100krad(Si) – 300krad(Si) SEU/SEL completed SEL Threshold > 65MeV/cm²/mg (RHBD IHP cells) SEU Threshold > 30MeV/cm²/mg (IHP RTMR FF)

IHP Processes and PDKs for Space Applications

Summary III of III

Status : 2019

	SGB25V/RH	SG13S/RH
■ Evaluation Testing ■ in acc. ESCC No. 2269010	completed	not yet performed
■ Operation Temperature (max rated T_j)	-55°C to +125°C	-55°C to +125°C (TBC)
■ Test Vehicles ■ in acc. ESCC No. 2269010	TCV, DEC-I/-II, RIC	TCV, DEC –I DEC-II(CMOS, Bipolar) RIC in progress
■ Radiation Tests ■ TCV (Devices, analog) ■ DECs (Digital, Analog BiCMOS) ■ RIC (Mixed-Signal IC)	completed „ DEC-I (SEU/SEL), Early structures TID + SEE LO RIC	completed „ DEC-I (SEU/SEL), Early structures planned
■ Endurance Testing HT & RT ■ HBT npn- devices ■ HBT lifetime determination ■ CMOS devices ■ CMOS Core & IO Std Cell Library	passed very stable : no or low drifts characterization available drifts are mesured and defined lifetime determination ~ 20 years	not yet performed
■ Additional Tests (Reliability)	SiGe HBT HCI & Lifetime Estimation	SiGe HBT HCI & Lifetime Estimation

Conclusion

- Designing digital systems for space requires additional design steps
- Changes of the design flow are present from modeling, over library design to the general design flow and used architectures
- Most of the solutions are based on fault tolerance that always causes significant hardware & power overhead
- Different methods how to limit this overhead exist
  - Static techniques for reducing power overhead, but also reducing fault protection
  - Adaptive techniques enabling dynamic trade-off power-reliability
- Design examples have been provided
  - IHP technology is evaluated for the space applications

Special thanks to current and former members of my team that contributed to slides: Vladimir Petrovic, Aleksandar Simevski, Markus Ulbricht, Anselm Breitenreiter, Rizwan Syed, Felipe Kuentzer, Steffen Weidling, Patryk Skoncej, Yuanqing Li, Oliver Schrape, Junchao Chen

Thank you for your attention!

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