Machine Learning Techniques to Estimate the Functional Failure Rate of Complex Circuits

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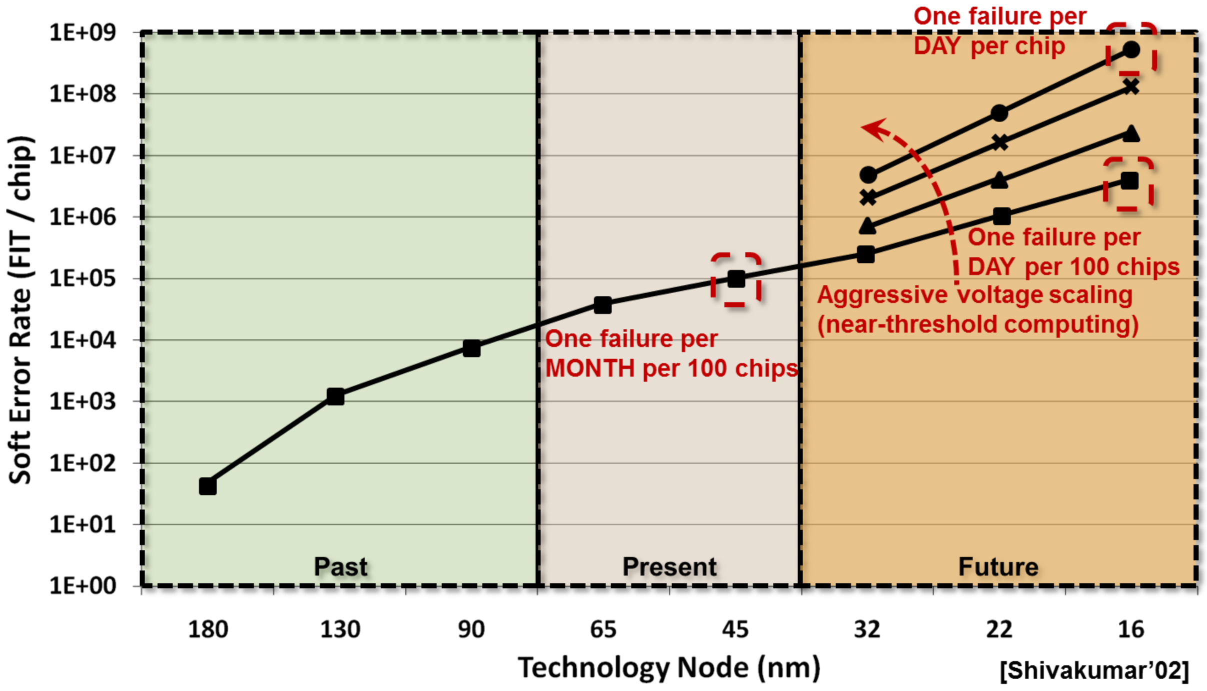
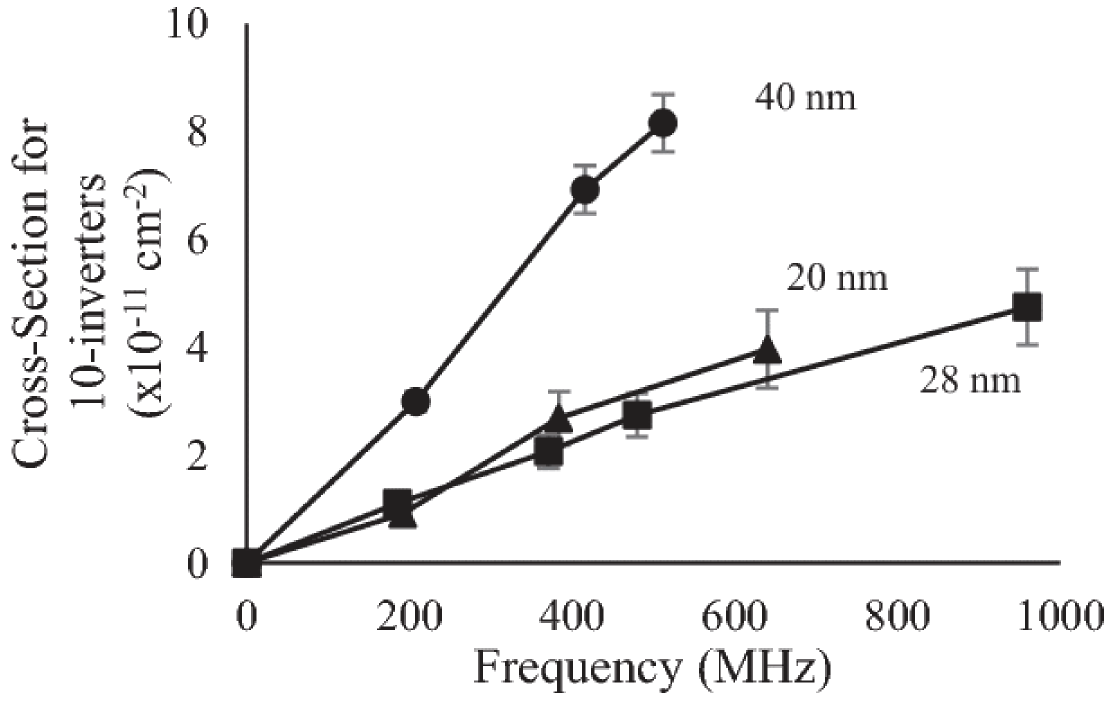
Motivation

- Due to
  - technology scaling,
  - lower supply voltages,
  - higher operating frequencies

  ➥ circuits become more vulnerable to transient faults





Source: http://cccp.eecs.umich.edu/research/reliability.php

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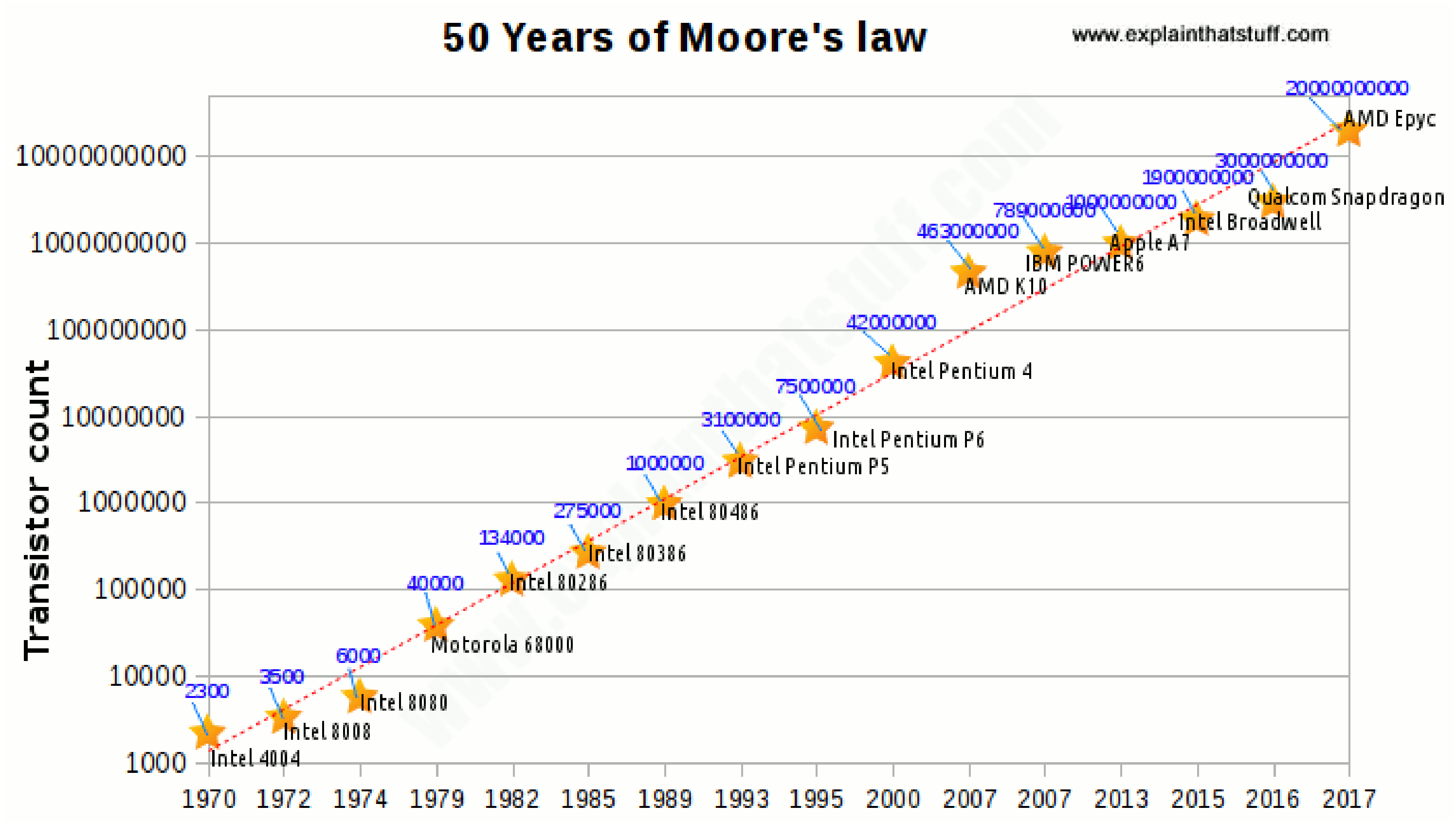
Motivation

- Circuits become more vulnerable to transient faults
- Complexity of today's circuits is increasing
  - ↳cost for reliability analysis is increasing



Source: https://www.explainthatstuff.com/integratedcircuits.html

Motivation

- Circuits become more vulnerable to transient faults
- Complexity of today's circuits is increasing
- Requirements of Functional Safety Standards
    - ⤷failure analysis needs to be performed on applicative level

Table 1: ISO 26262 Target Values for Quantitative Evaluation Metrics

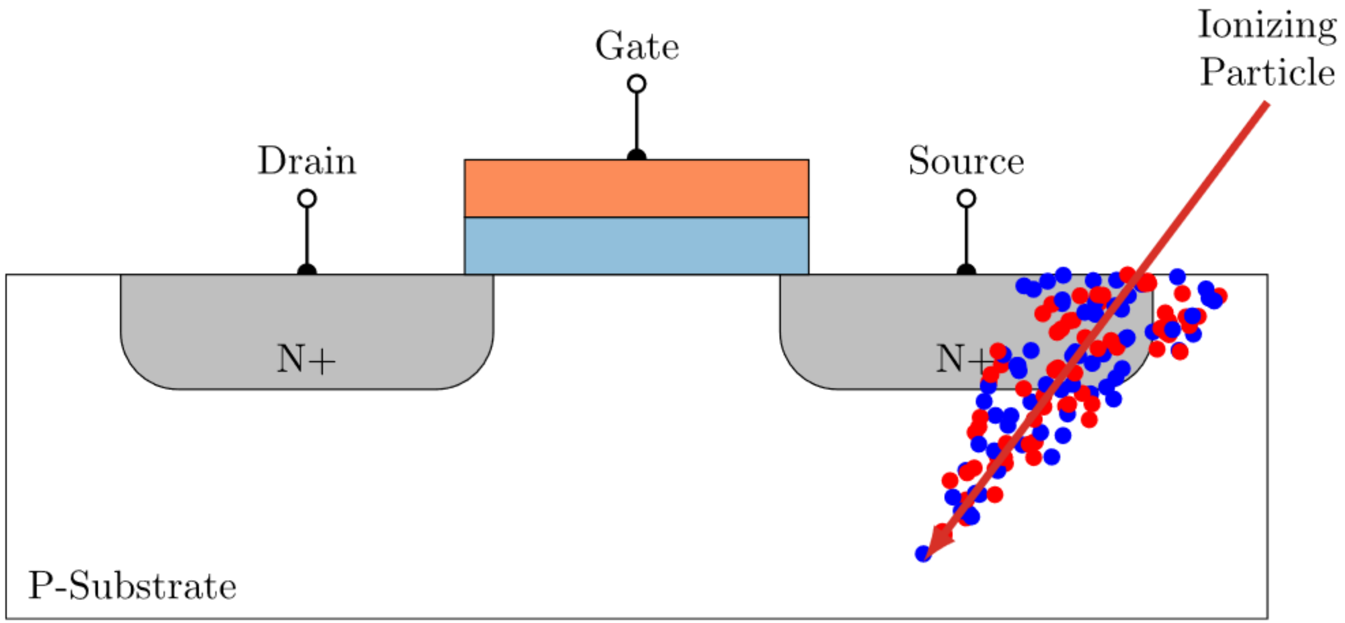
	ASIL-B	ASIL-C	ASIL-D
Random HW Faults	≤ 100 FIT	≤ 100 FIT	≤ 10 FIT
Single Point Fault Metric	≥ 90%	≥ 97%	≥ 99%
Latent Fault Metric	≥ 60%	≥ 80%	≥ 90%

Background

- Transient faults are caused by
  - radiation, noise, power disturbance, etc.

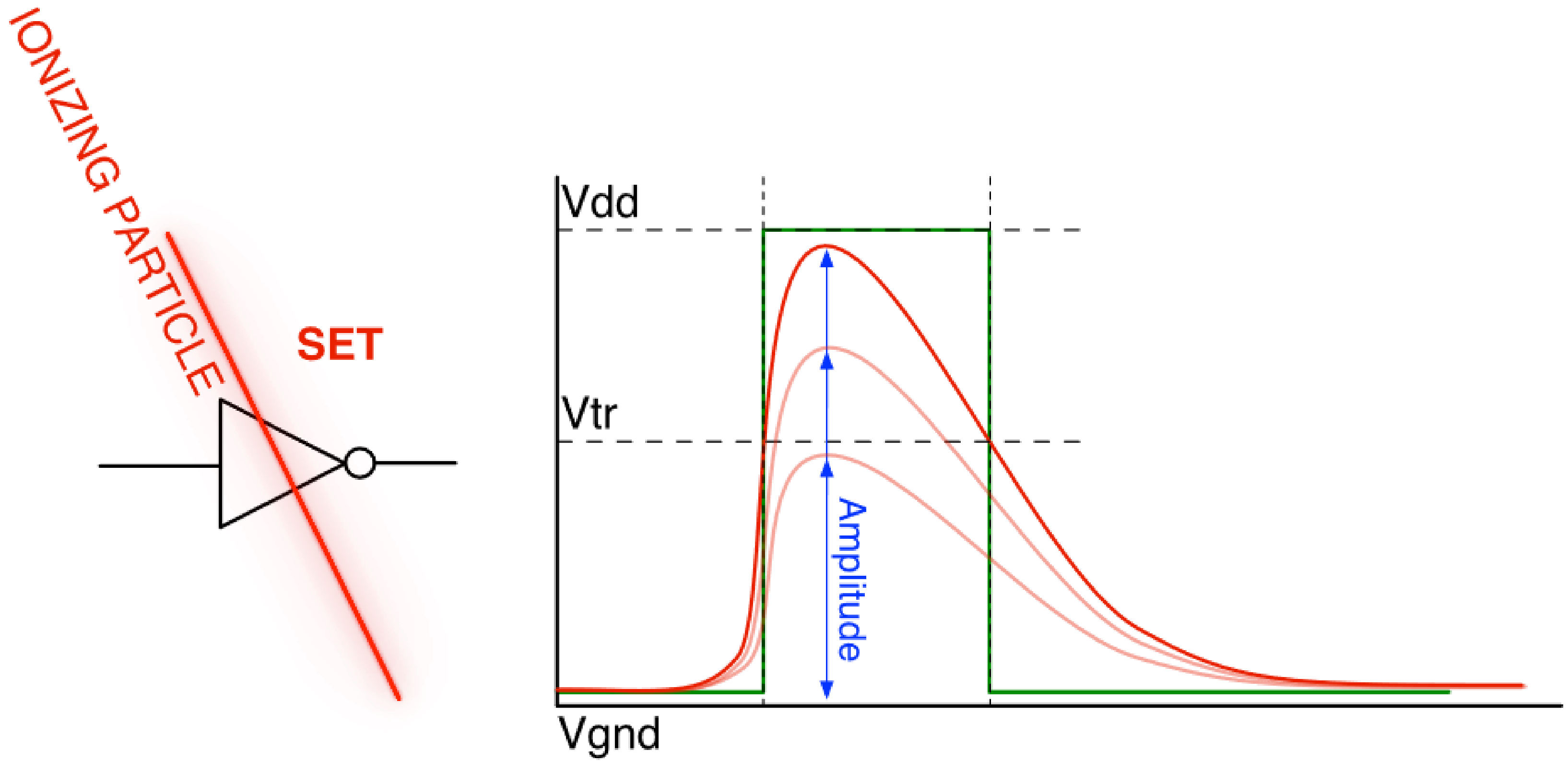
- Not all faults lead to errors or failures

- Fault ➥ Error ➥ Failure
  - Masking Mechanism
    - Electrical Masking
    - Temporal Masking
    - Logical Masking
    - Functional Masking



Background – Masking Mechanism

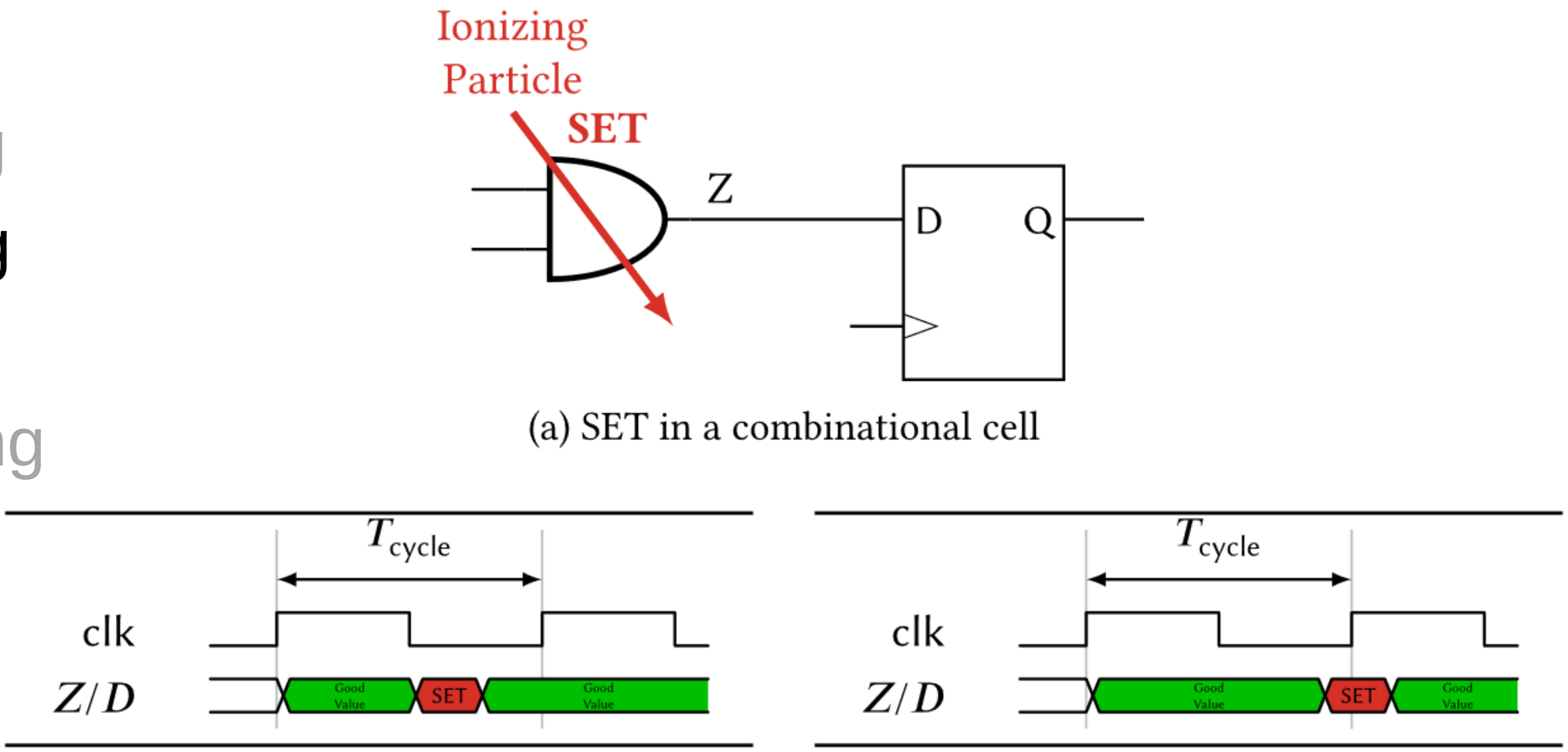
- Electrical Masking
- Temporal Masking
- Logical Masking
- Functional Masking



Source: E. Costenaro – "Techniques for the evaluation and the improvement of emergent technologies' behavior facing random errors," PhD Thesis, Université Grenoble Alpes, 2015.

Background - Masking

- Electrical Masking
- Temporal Masking
- Logical Masking
- Functional Masking



(a) SET in a combinational cell

(b) SET masked

(c) SET sampled (not masked)

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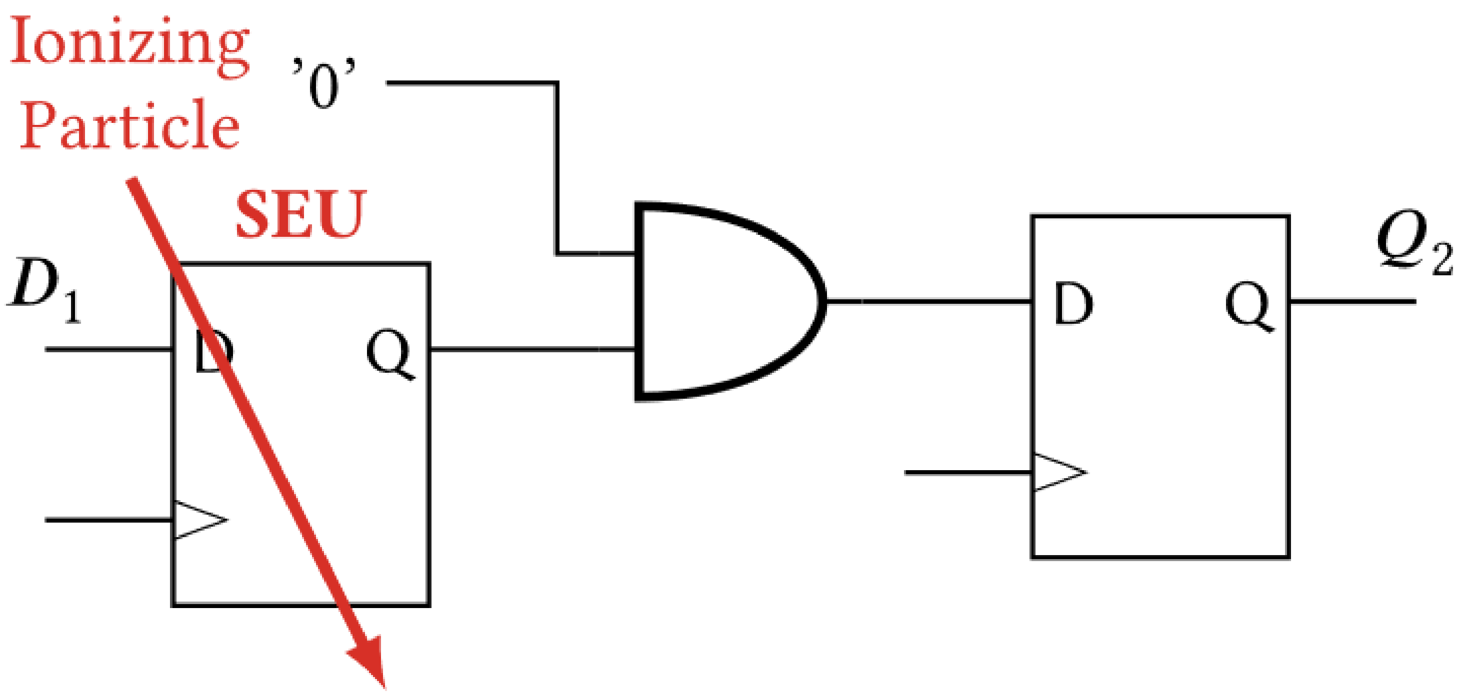
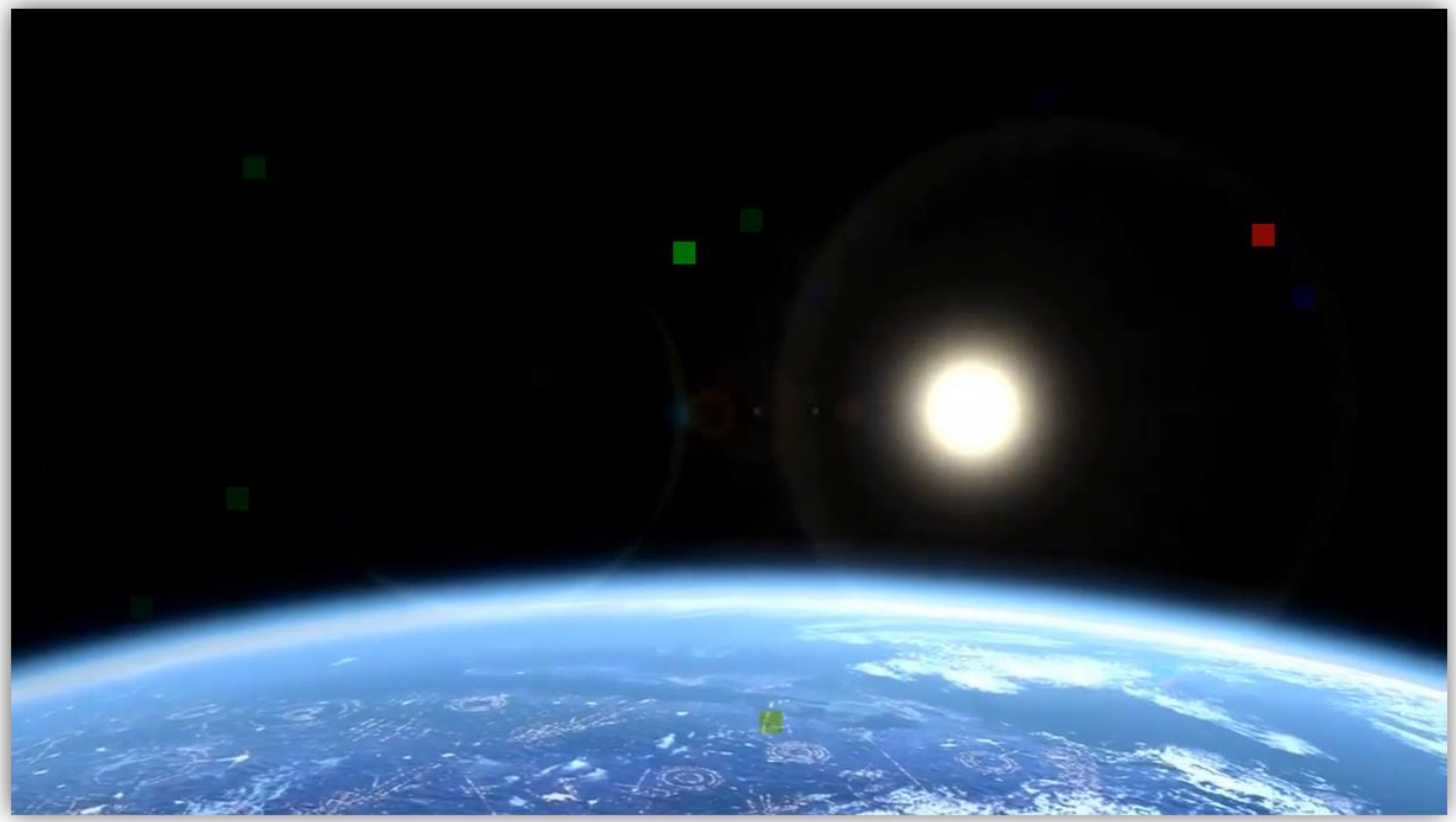
Background - Masking

- Electrical Masking
- Temporal Masking
- Logical Masking
- Functional Masking



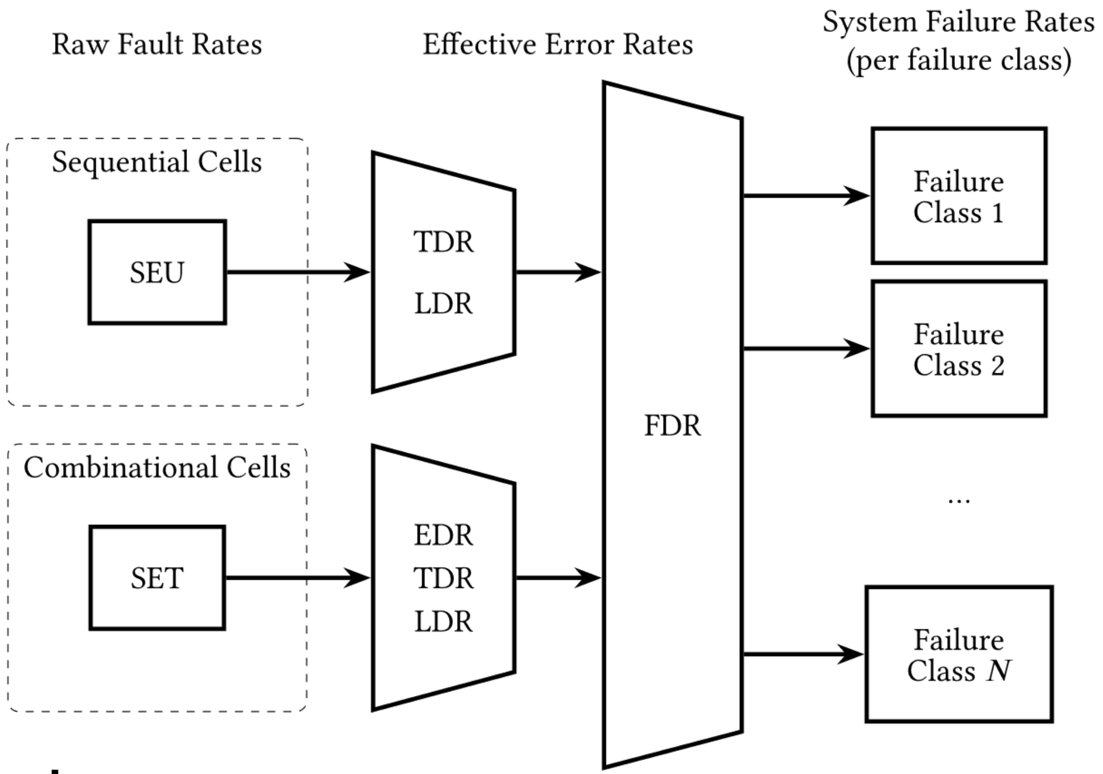
Background - Masking

- Electrical Masking
- Temporal Masking
- Logical Masking
- Functional Masking



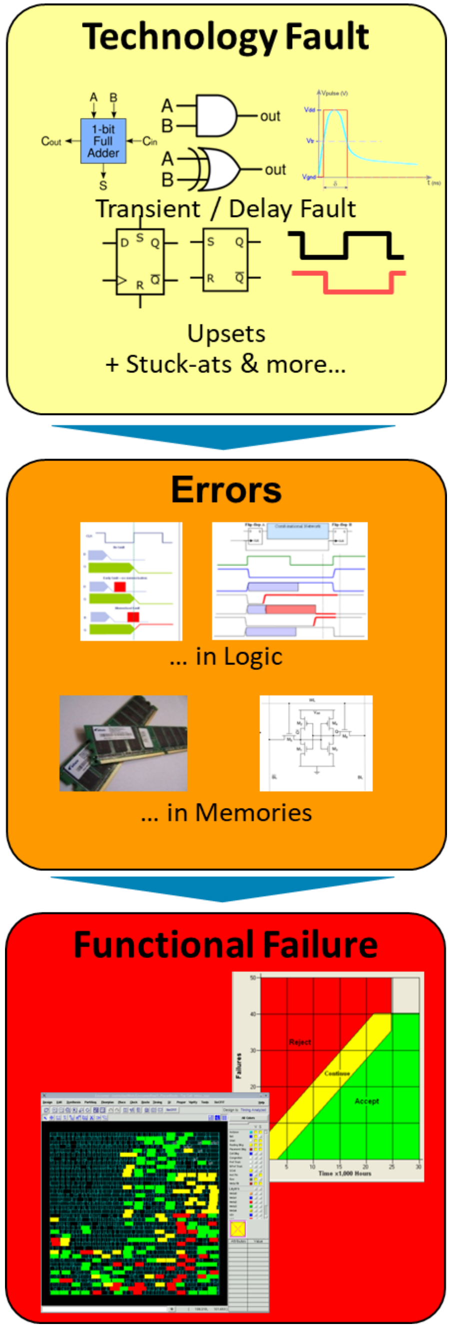
Background

- Fault ⮩ Error ⮩ Failure
  - De-Rating/Vulnerability Factor
    - Electrical De-Rating (EDR)
    - Temporal De-Rating (TDR)
    - Logical De-Rating (LDR)
    - Functional De-Rating (FDR)



- Typical reliability assessment calculation:

$$FIT_{\text{Eff}} = \sum_{\substack{\text{circuit}\\\text{elements}}} FIT_{\text{Tech}} \times \boldsymbol{EDR} \times \boldsymbol{TDR} \times \boldsymbol{LDR} \times \boldsymbol{FDR} \times \begin{cases} \text{failure class } 1 \\ \text{failure class } 2 \\ \dots \\ \text{failure class } n \end{cases}$$



Background

- Fault ➥ Error
  - fault simulation
  - structural design exploration
  - propagation analysis

- Error ➥ Functional Failure
  - accelerated testing
  - simulation based approaches
  - significant costs
    - human efforts
    - processing resources
    - tool licenses

Basic Idea

- Use Machine Learning for the reliability analysis
  ↪reduce the cost

- What are we trying to predict?
  - functional reliability metrics for Flip-Flops (FF)

- How do we do it?
  - gather as much information from the circuit as we can (features)
    - collection needs to be economical
  - obtain Functional De-Rating (FDR) as training/reference data
  - use Machine Learning techniques to train models

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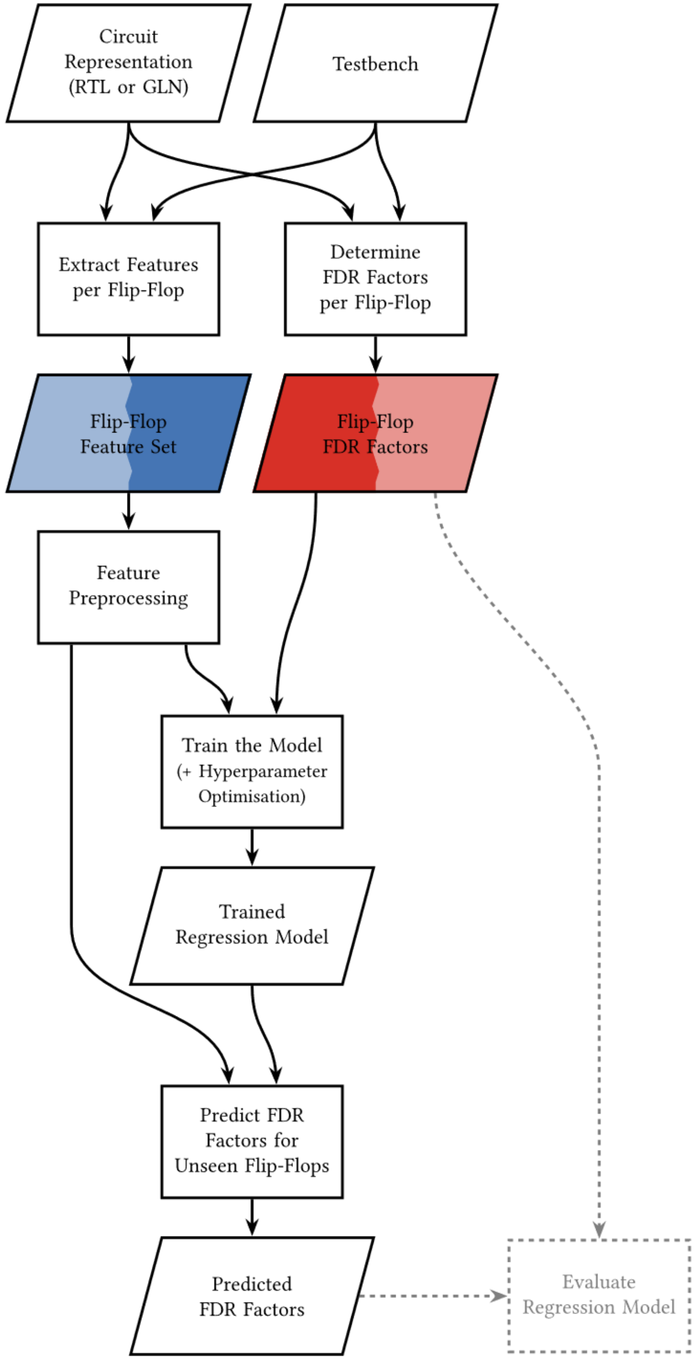

Initial Methodology

- Extract features
  - from Gate-Level Netlist and Testbench/Simulation
- Gather FDR Reference/Training data
  - by fault injection simulation for (parts of) the circuit
- Train a model
  - supervised regression
  - training size: number of training samples
- Predict FDR factors
  - per individual flip-flop instance
- Benchmark/Validate model
  - against reference data
  - cross validation is used

➥Obtain model which is trained for one circuit

Feature Extraction

- The feature set
  - characterizes each FF instance of the circuit
  - contains attributes from
    - static elements
    - dynamic elements
  - is extracted from the Gate-Level Netlist (GLN) and Simulation/Testbench

Feature Name
Structural Related Features
FF at Startpoint/Endpoint
Connections from/to FF
Connections from/to Primary Input/Output
FF Stages to/from Primary Input/Output (max/avg/min)
Constant Drivers
Has Feedback
Feedback Depth
Is Part of Bus
Bus Position
Bus Length
Bus Label
Module Label
Signal Activity Related Features
@0/@1
State Changes
Synthesis Related Features
Drive Strength
Depth Combinatorial Path
Combinatorial Cells at/from Input/Output

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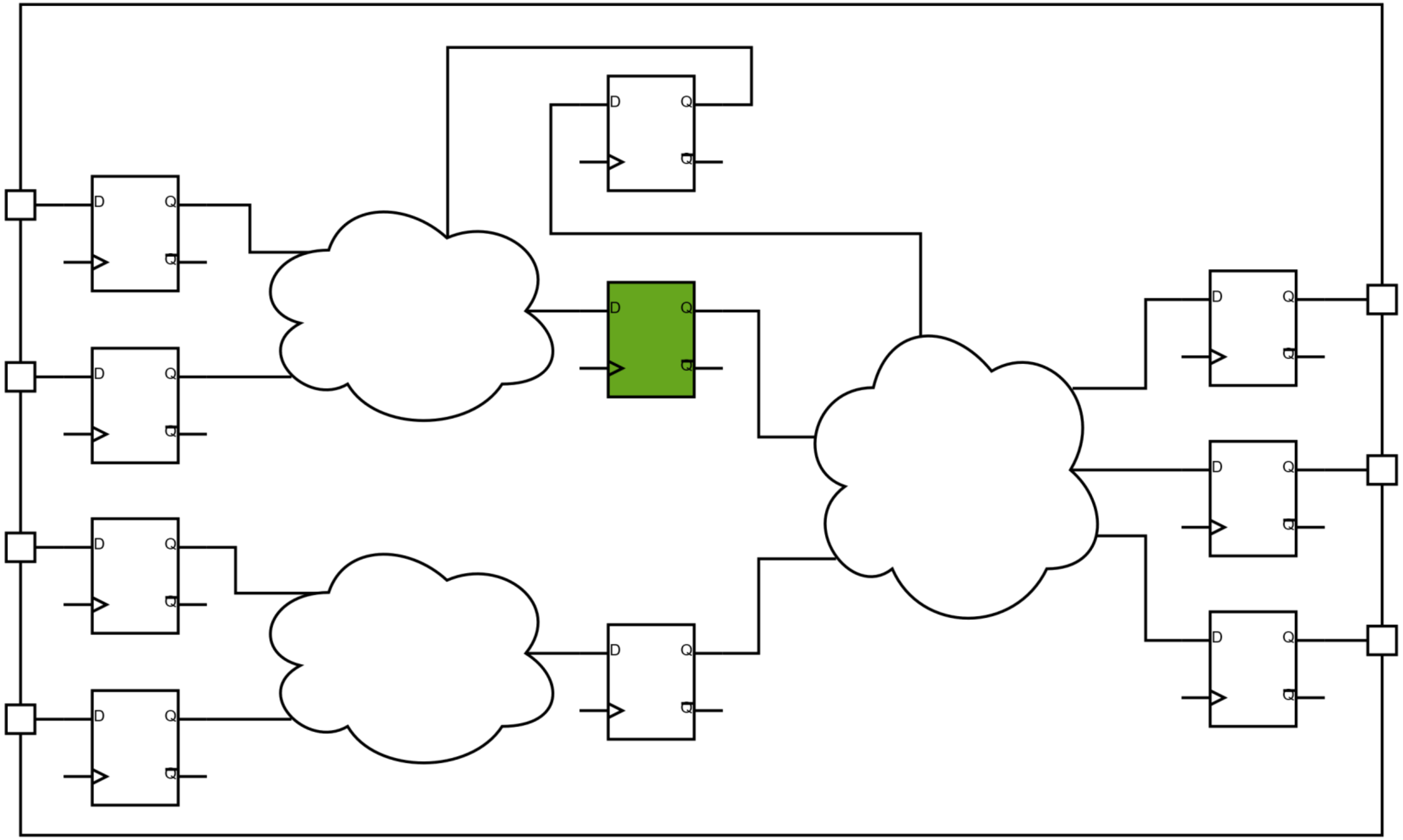
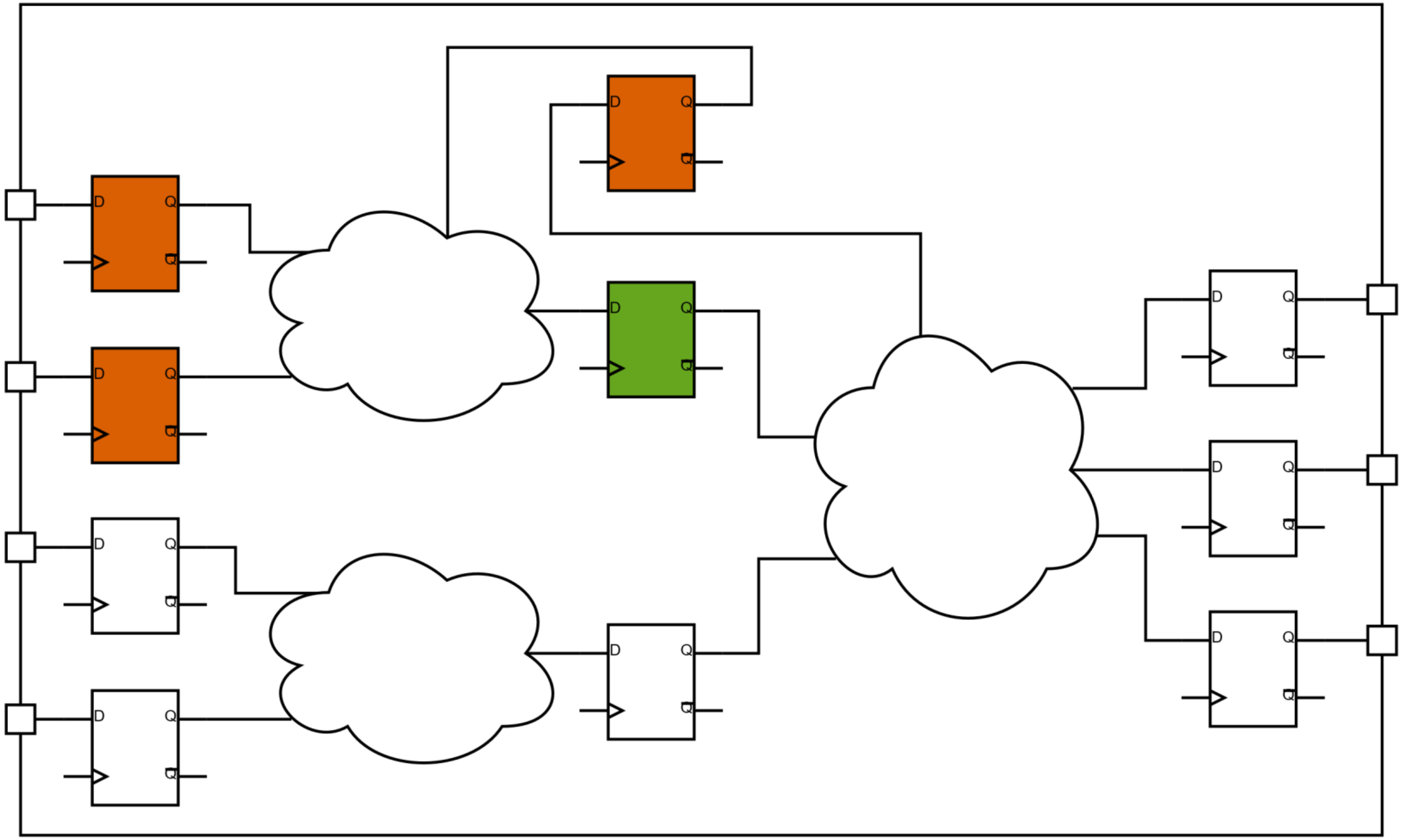
Features

- Target Flip-Flop FF_i



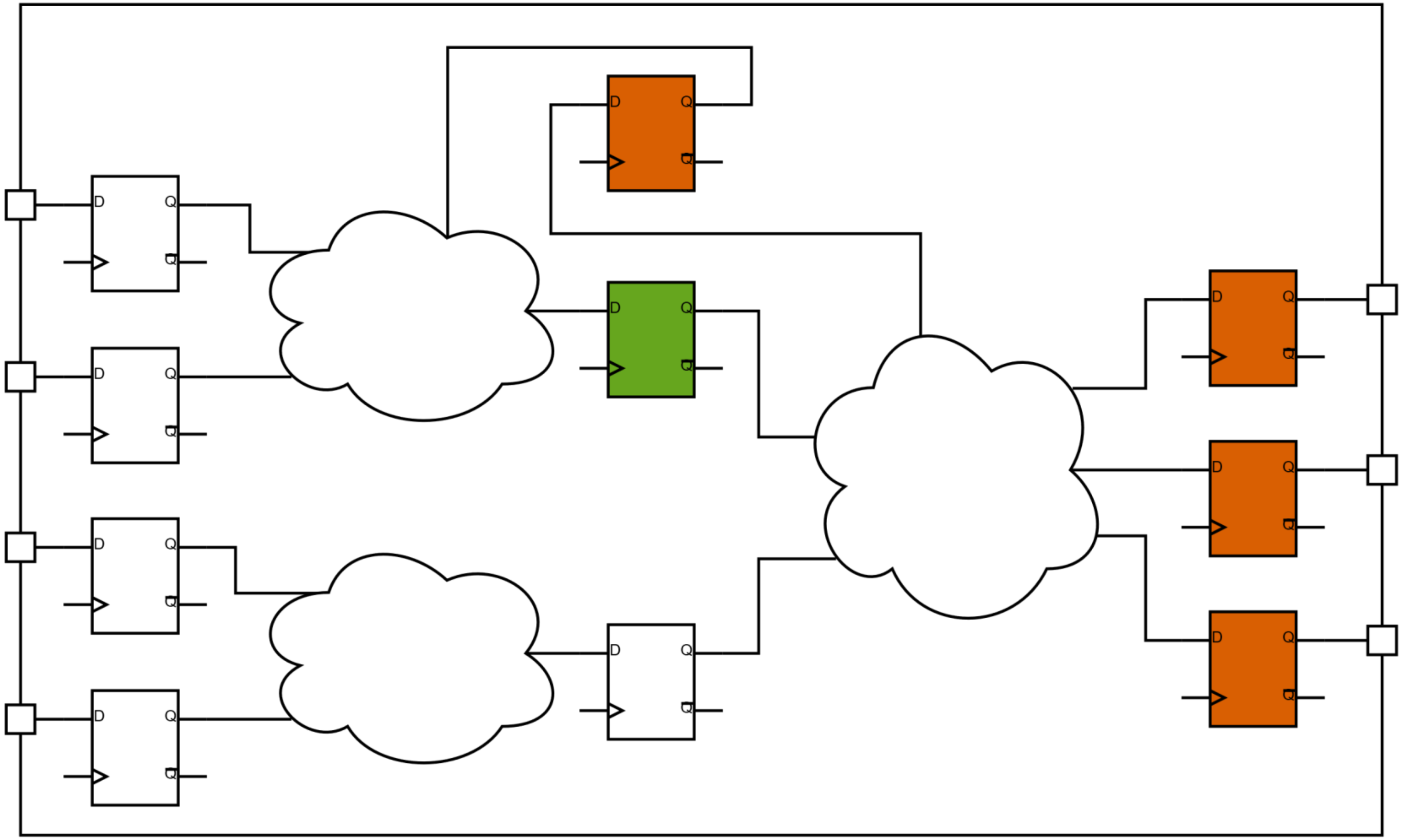
Features

- Feature: FF Fan-In = 3



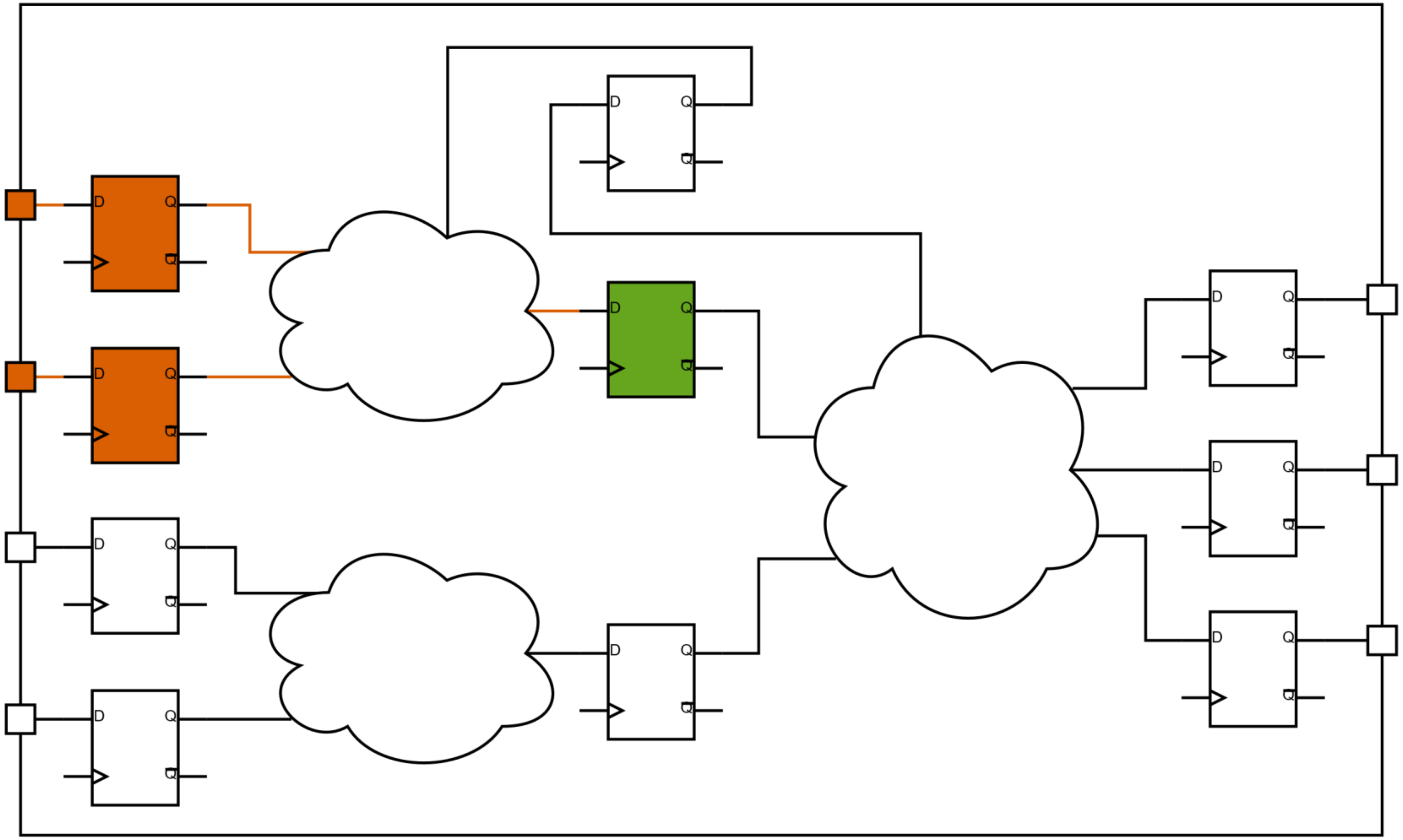
Features

- Feature: FF Fan-Out = 4



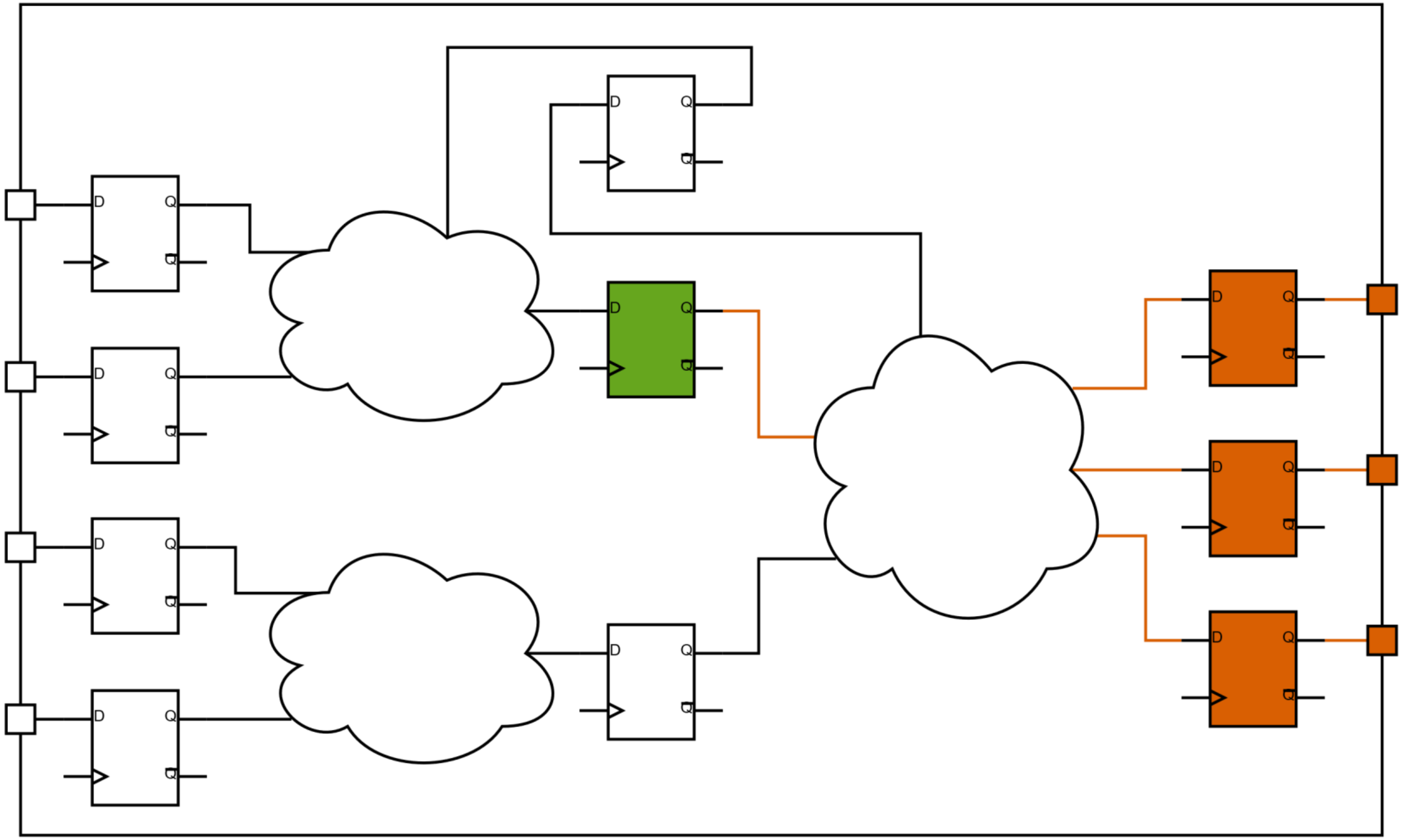
Features

- Feature: Nr of Connections from Primary Inputs = 2
  Proximity from Primary Input (FF Stages) = 1



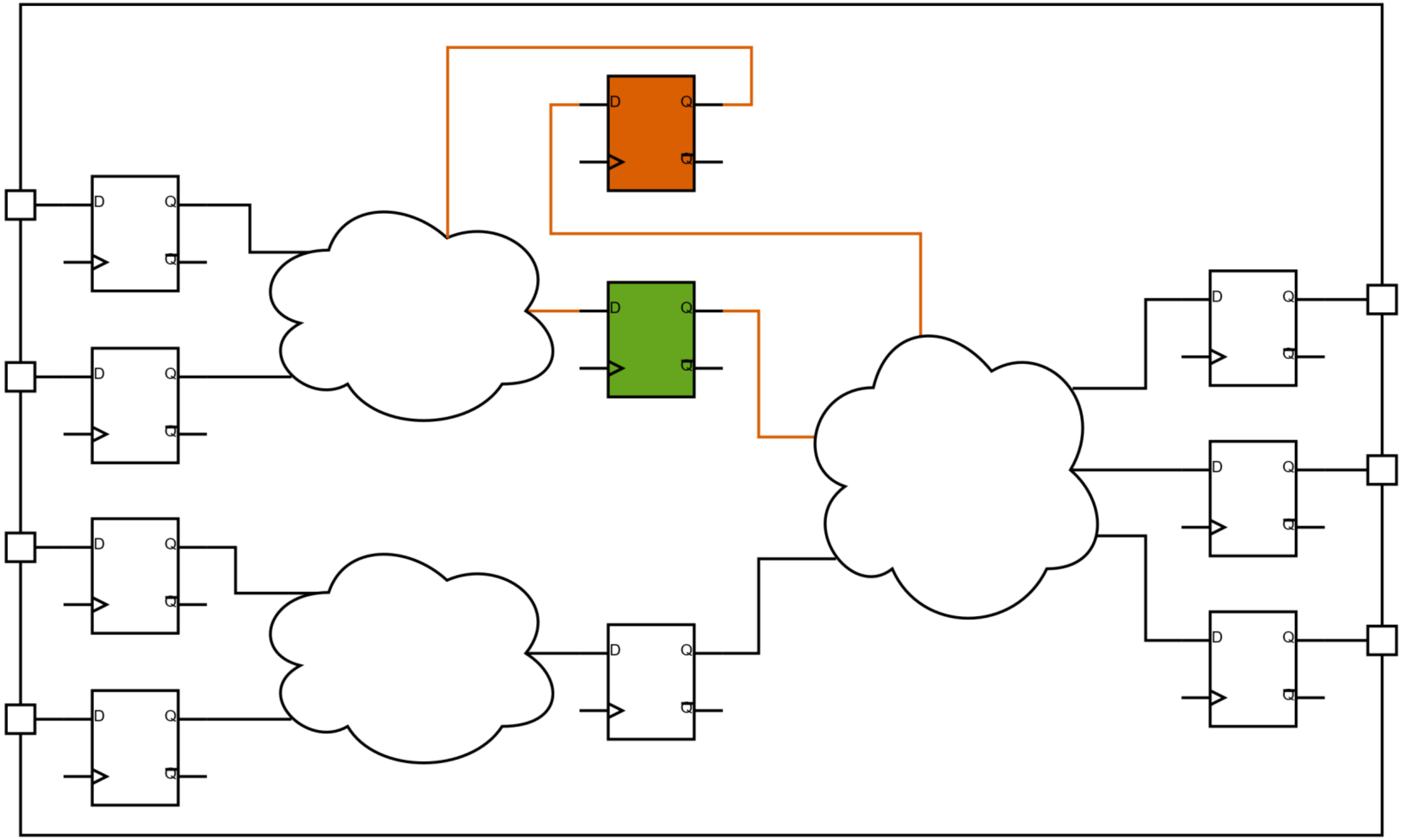
Features

- Feature: Nr of Connections to Primary Outputs = 3
  Proximity to Primary Outputs (FF Stages) = 1



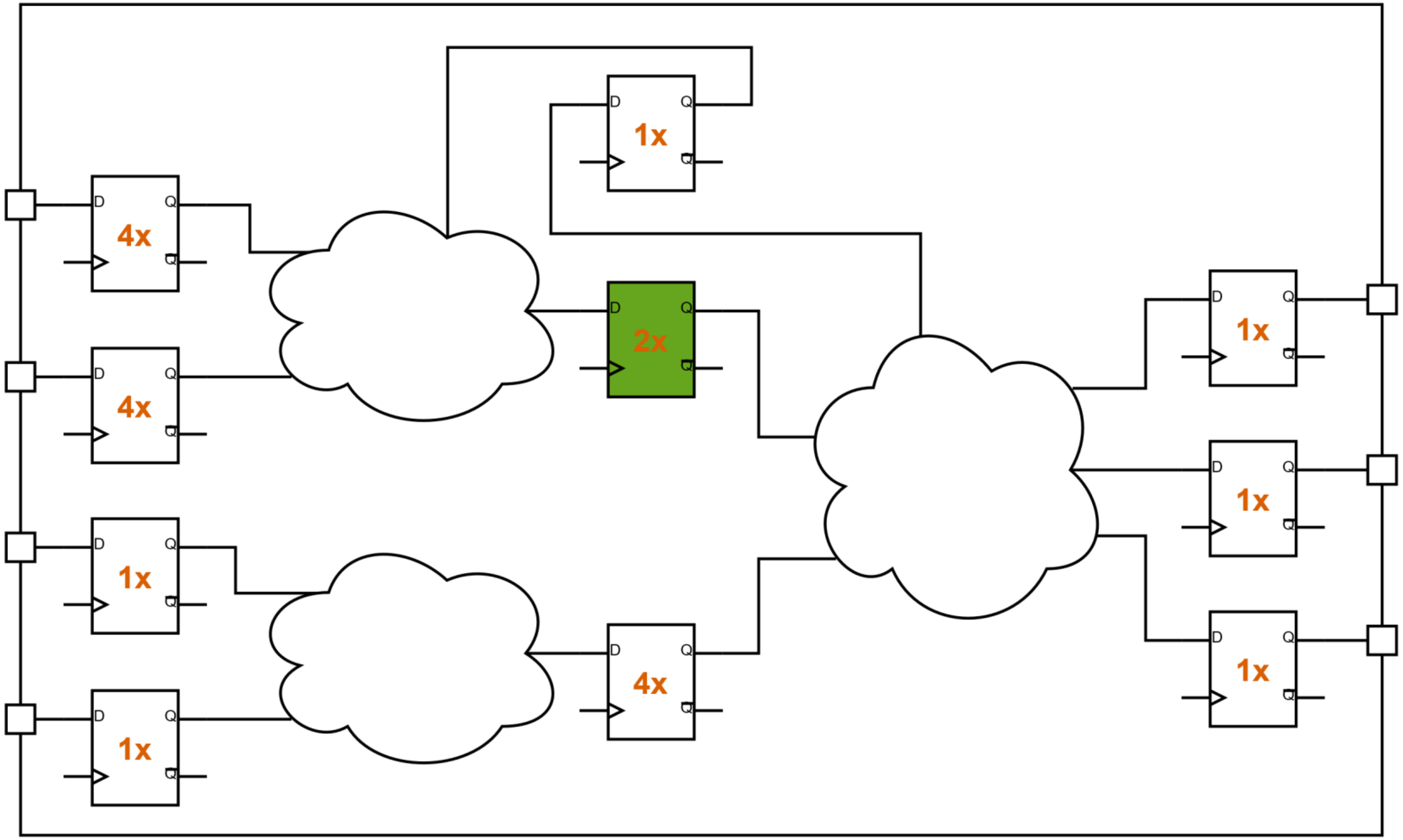
Features

- Feature: Feedback Loop = true
  Feedback Loop Depth (FF Stages)= 1



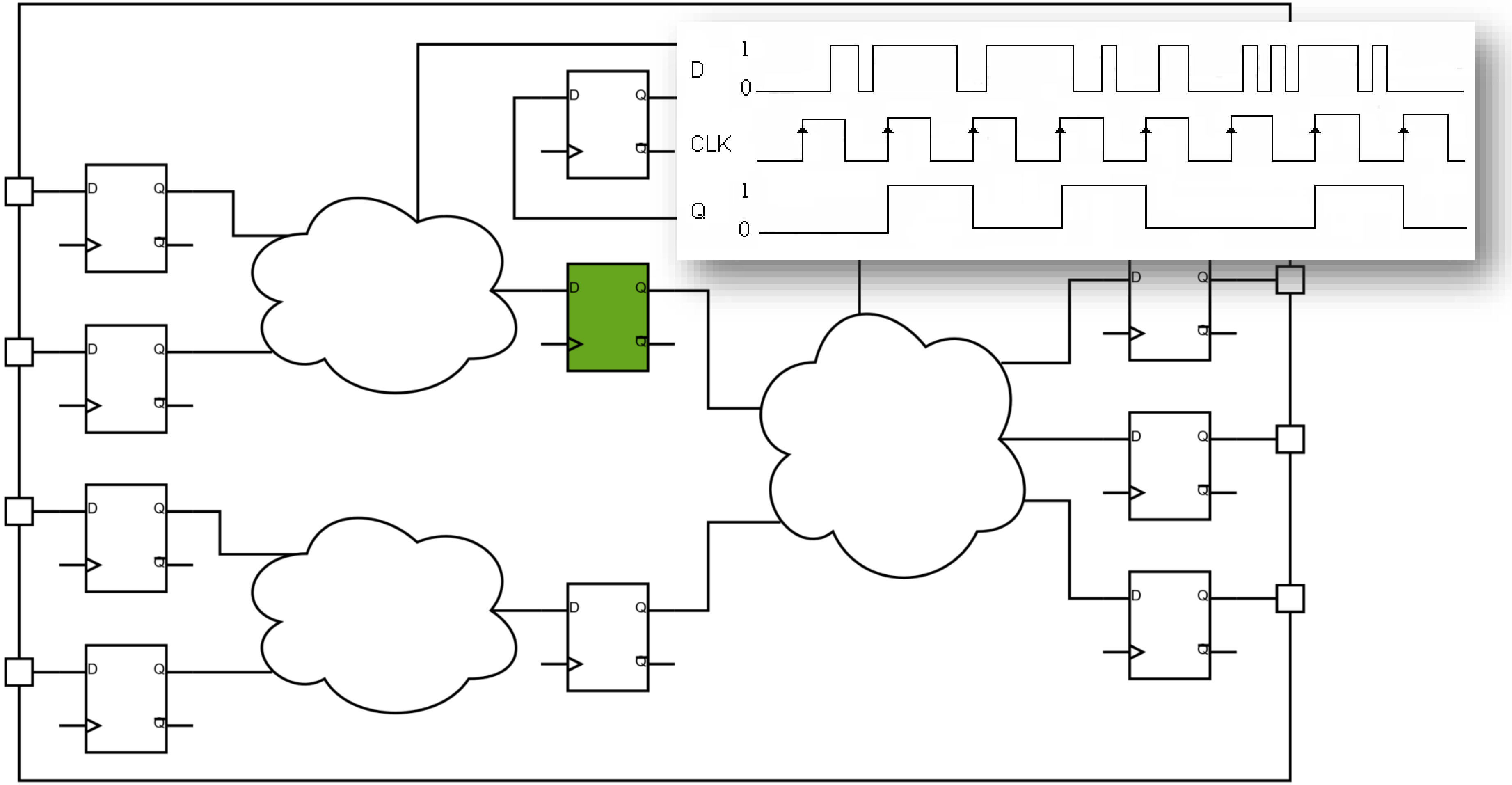
Features

- Feature: Cell Properties – Drive Strength = 2



Features

- Feature: Signal Activity – Transitions @Q = 6
  – At 0/At 1 @Q = 5/3



Model Implementation

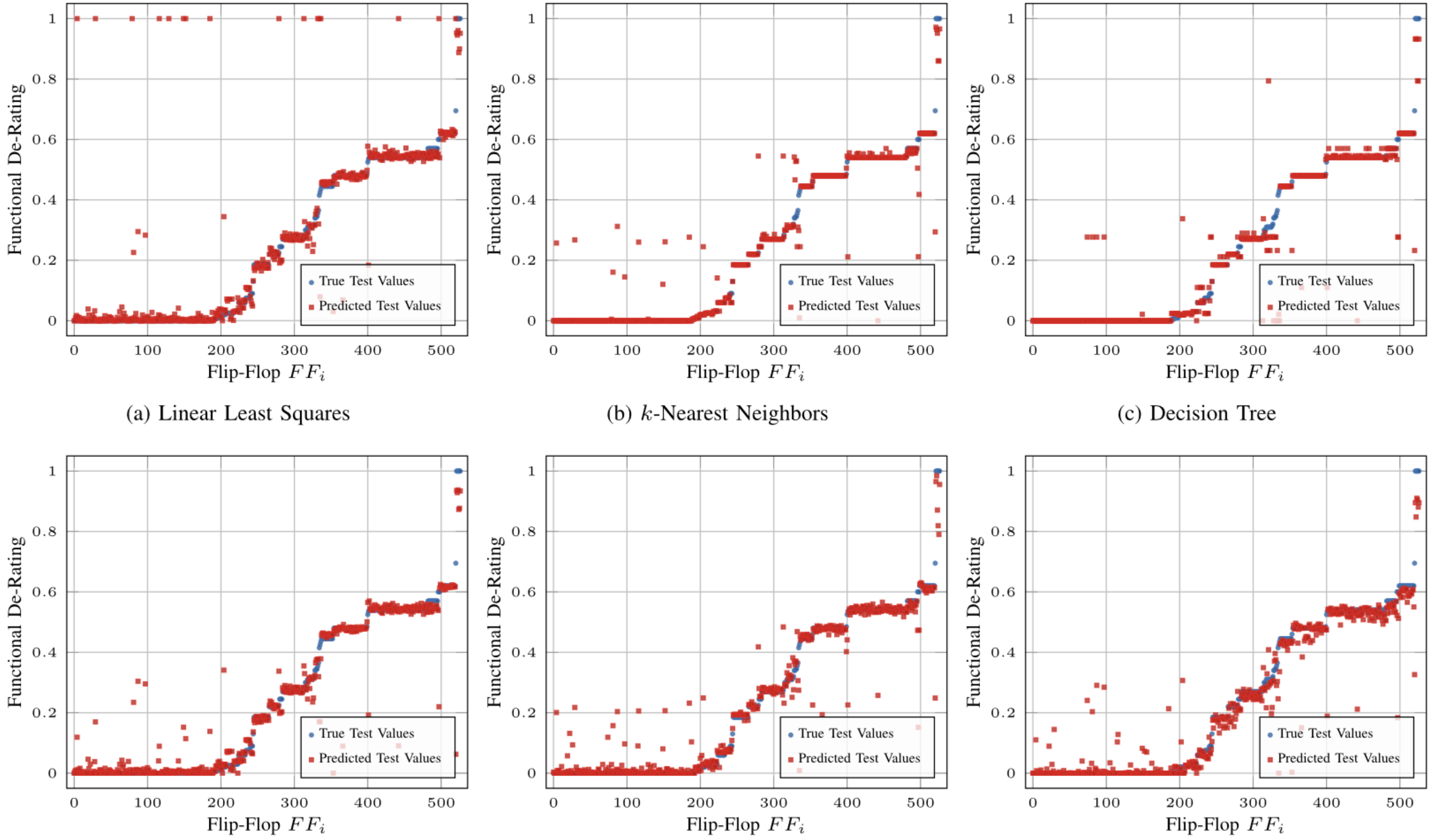
- Models are implemented using Python’s scikit-learn framework
  - No licenses needed

- Several regression models have been evaluated
  - Different performance/error metrics have been applied
    - Coefficient of Determination: $R^2 \in [-\infty, 1]$

- Cross validation fold of 10 and a training size of 50%

Prediction Results – Functional Failure

- Prediction Results (training size = 50%)



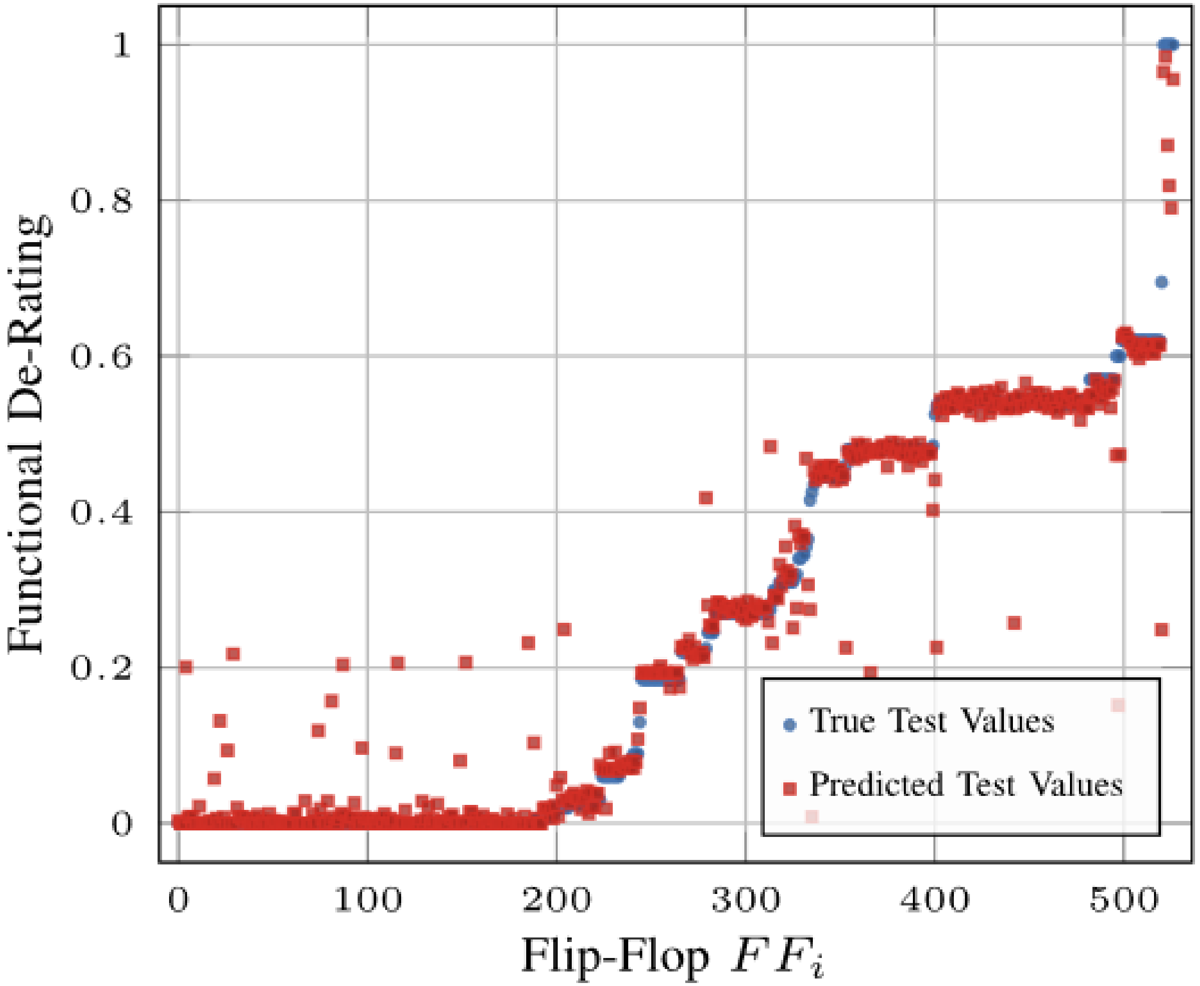
(a) Linear Least Squares (b) *k*-Nearest Neighbors (c) Decision Tree

(d) Ridge w/ Polynomial Kernel (e) SVR w/ RBF Kernel (f) MLP Nerual Network

Prediction Results (Example)

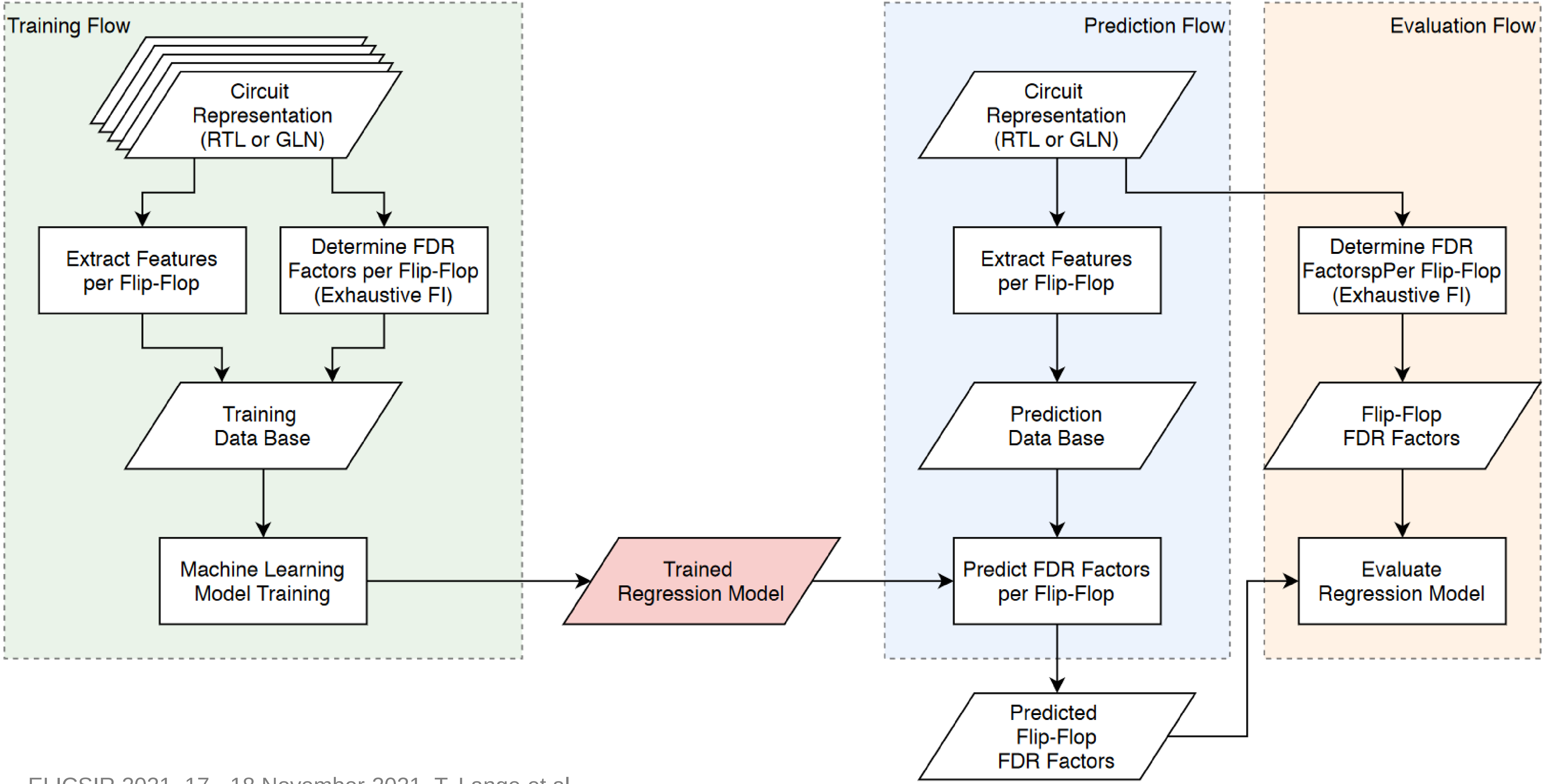
- Prediction Results (training size = 50%)
  - $R^2 = 0.927$

- Model is trained and predicts FDR factors only for **one** circuit!



(e) SVR w/ RBF Kernel

Towards Training of a Universal Model



Considered Circuits

- Benchmark circuits
  - ISCAS'85/89
  - ITC'99
  - IWLS'2005
- OpenCores designs
  - 10GE MAC
  - Double Precision Floating Point
  - Secure Hash Algorithm 3 (SHA-3),
  - Advanced Encryption Standard (AES),
  - USB 2.0 Functional
  - etc.
- RISC-V Processor (picorv32, lowRISC ibex, rocket chip)

Challenges

- Gathering the training and reference data is expensive
  - exhaustive fault injection simulation campaigns need to be performed

- Develop open source fault injection flow
  - based on open source simulators (Icarus Verilog, Verilator, …)
  - better scalability of the simulation campaigns
  - make flow openly accessible (e.g. GitHub)
  - community can adapt and contribute to the collection of the data

➥Obtain large and open fault injection database

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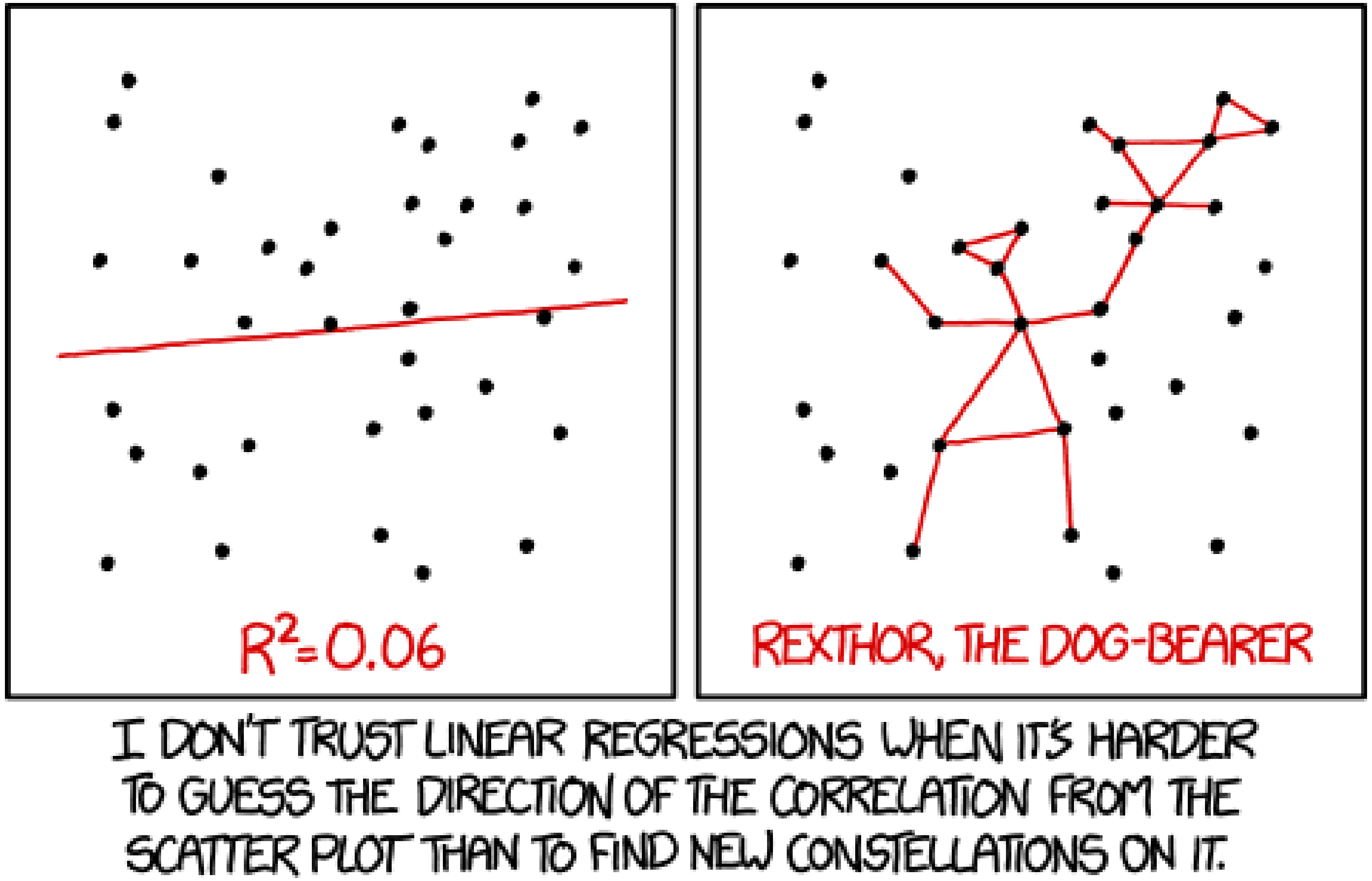
Conclusions and Perspective

- Machine Learning can be used to predict reliability metrics
  - Model is trained and predicts FDR factors for one circuit
- Create a Machine Learning based Reliability Analysis tool
  - train a tool on a variety of circuits, workloads, applications
  - able to predict reliability metrics in seconds on very large circuits
- Future work
  - Improve feature set/Add new feature to increase performance

Q&A



Source: https://xkcd.com/1725/

Thank you!

Questions?

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