An STA CAD Tool for SET Generation and Propagation

CAS (Circuits and Systems) Lab,
University of Thessaly, Greece.

Who we are – CAS Lab @ UTH

Volos, Thessaly, Greece

UNIVERSITY OF THESSALY FOUNDED 1984

University of Thessaly

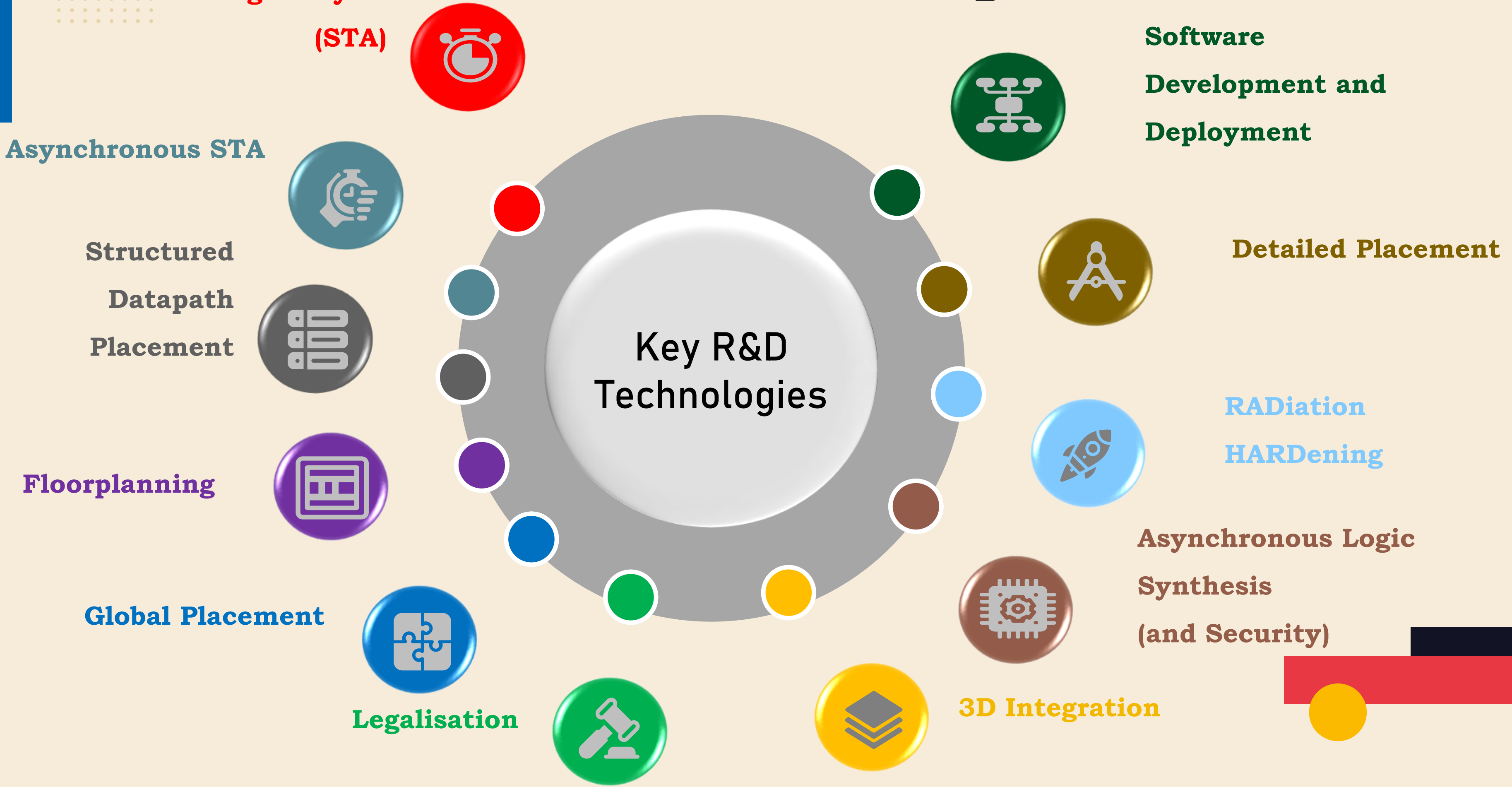
CAS lab
University of Thessaly
Greece

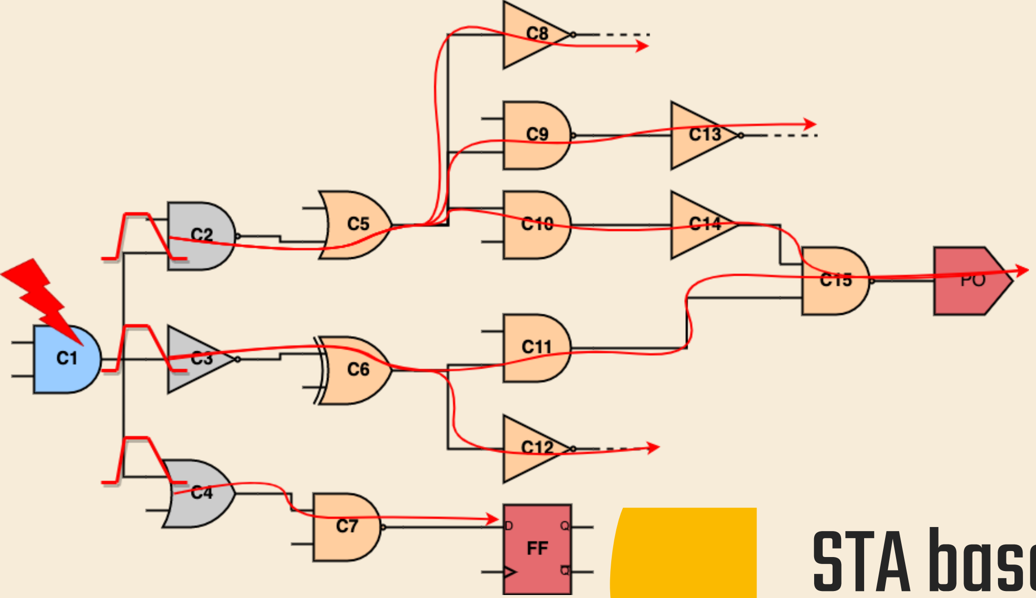
Our Lab

EDA R&D

CONFIDENTIAL

CAS Lab EDA Technologies





STA based

SET GENERATION and PROPAGATION

Technology Overview

What we do

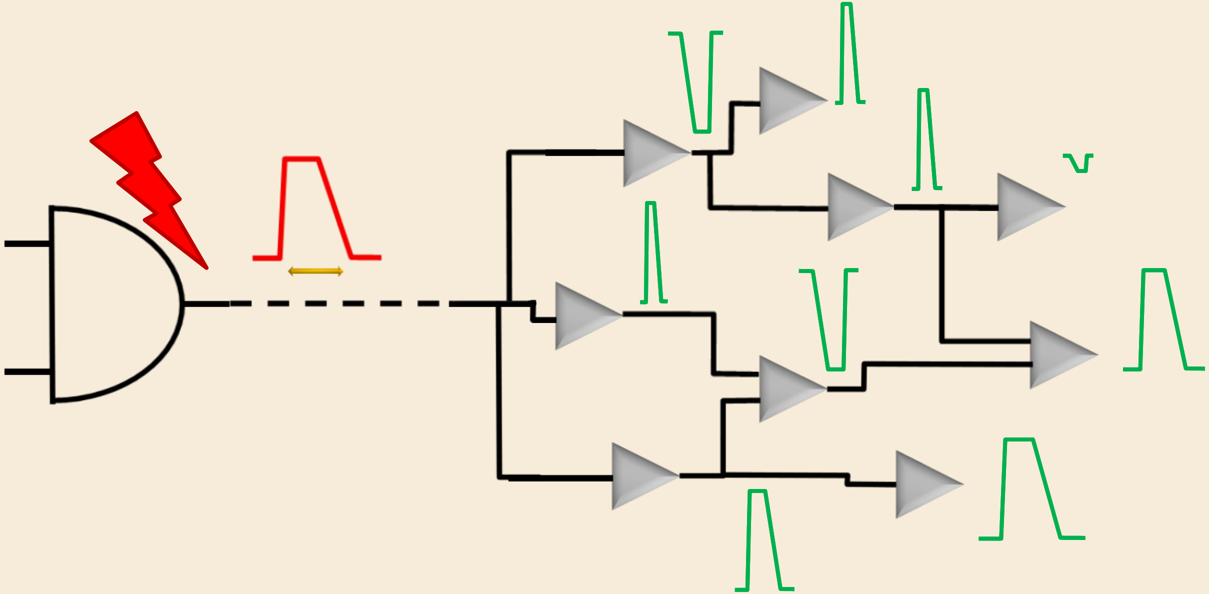
- ❑ SET Generation and Propagation
- ❑ Using State of the Art Static Timing Analysis (STA)
- ❑ SPICE accuracy, with interfaces to SPICE for error calculation at the path or logic cone level
- ❑ Our toolset includes an embedded STA Engine
- ❑ Accurate RC Wire Delay Modelling
- ❑ Can identify the worst FF, with respect to SET pulse width
- ❑ Supports multiple SET Generation current models, *e.g.* Double-Exp
- ❑ Supports internal Case Analysis conditions for SET Pulse Propagation

- ❑ Mitigation part ➔ perform IPO operations to improve SET Propagation ➔ WIP

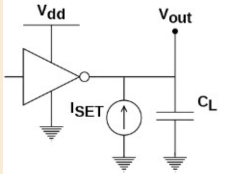
What we don't do

- ❑ NOT transistor/electrical level
- ❑ NOT device level
- ❑ NO Special Library Characterization required, only user-provided Parameters

The Problem - SETs



STA-based RADHARD Flow at a glance



.lib, .lef, .SPEF, .Verilog, .SDC files

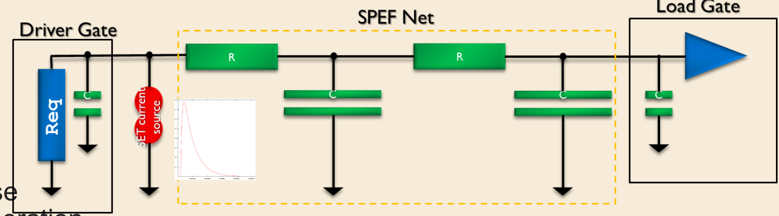
- Load Design Netlist and Physical Representation into Tool

Perform STA

- Analyse Design Timing

SET current model (DEXP), SET location, side inputs ➔ Scenario File

- User-input for SET Generation



Run SET Generation

- Pulse Generation at SET location

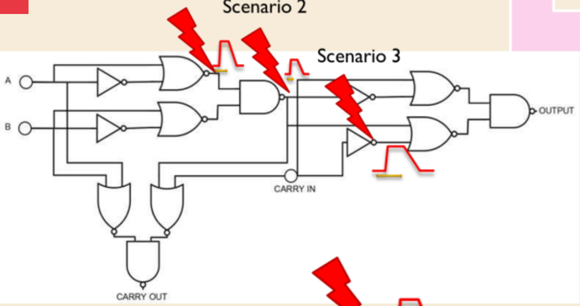
Run SET Propagation

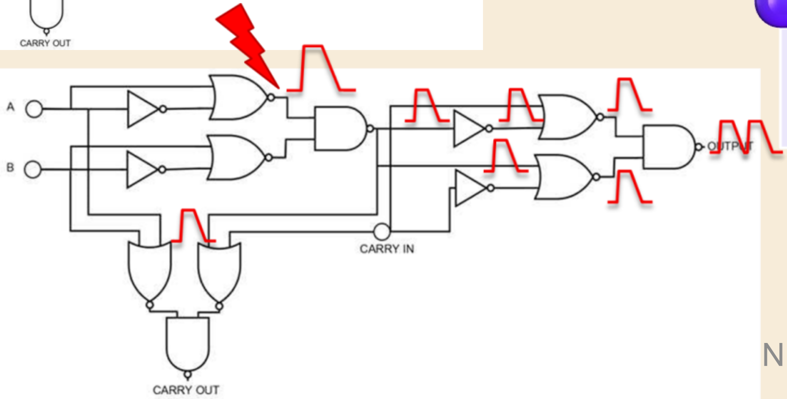
- Propagation at Endpoints (FFs, POs)

SPICE out

Measure Error against SPICE/SPECTRE

MEASUREMENTS in

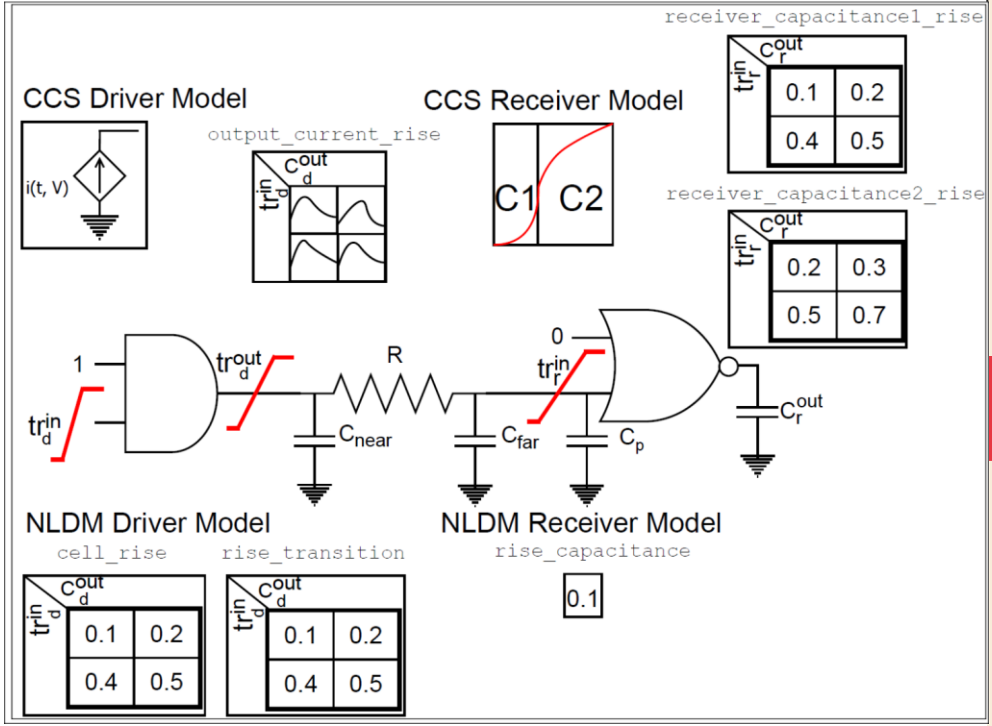




CCS Timing Model

CCS Timing

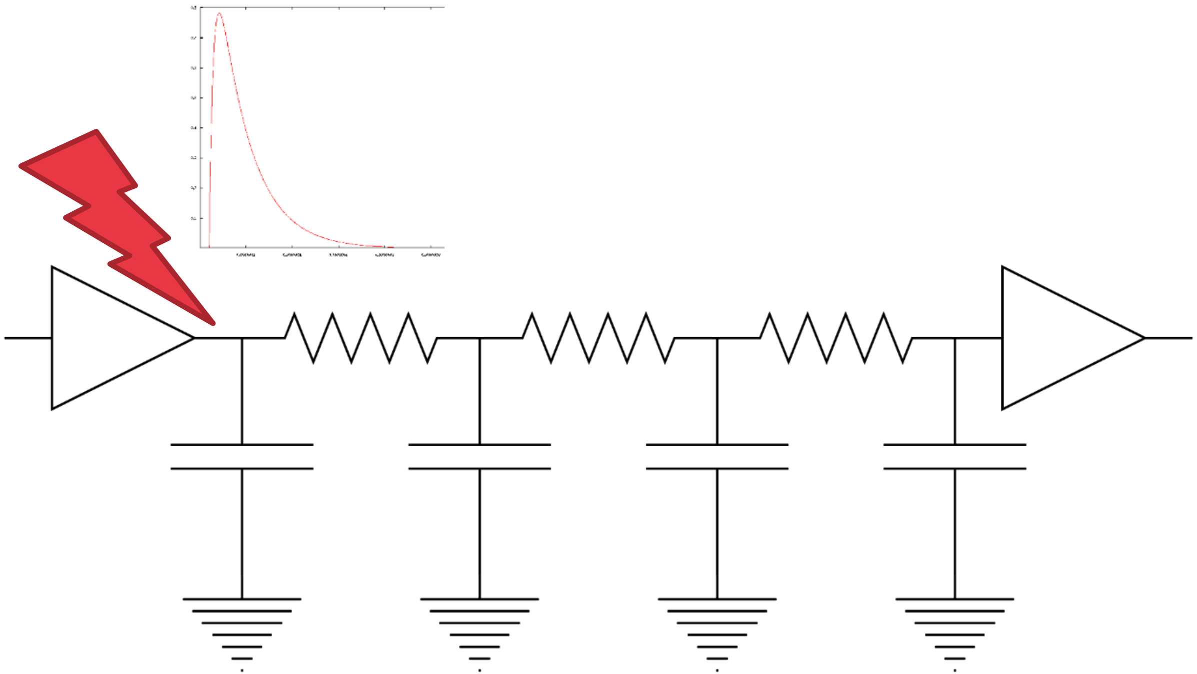
- ❑ **Highly Accurate RC Delays; key for accurate pulse propagation through RC Networks**
- ❑ **Current profiles of CCS gate responses may be used to extract standard-cell information, *e.g.* Reff, Vout, without SPICE or Characterisation**
- ❑ **Good for First/Second-Order SET Generation Approximations**



Set Generation Example

Set Generation Example

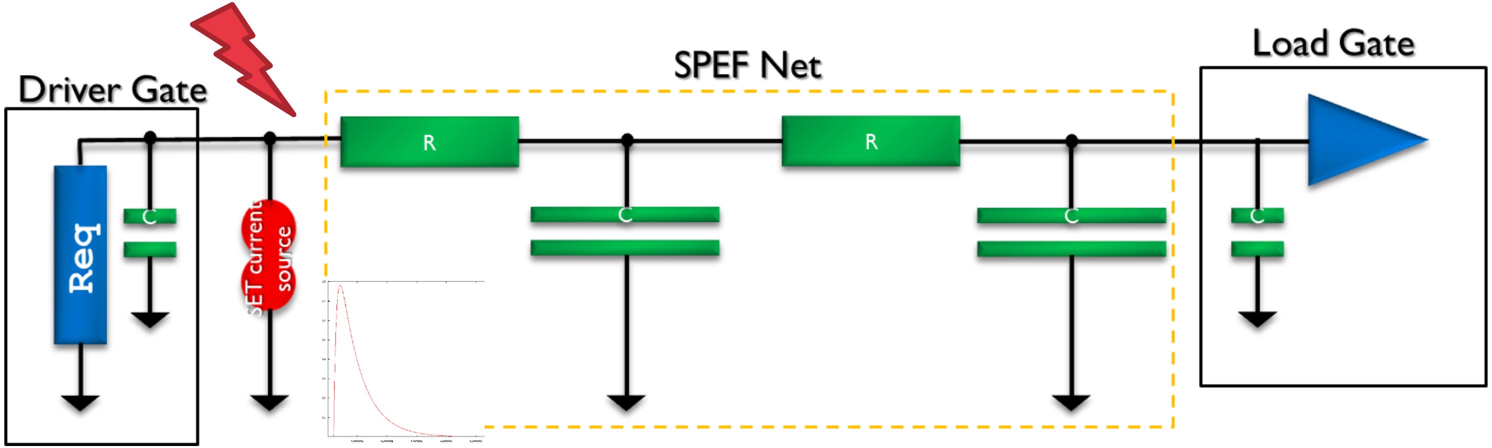
- User provides SET parameters, location, side inputs



Set Generation Example

- User provides SET parameters, location, side inputs
- With an annotated SPEF – this is a First/Second Order Approximation Model
- Pulse has two parameters, slew, delay (AT)
- Delay is MORE critical as (i) slew will be regenerated, (ii) width ←→ delay

SET Generation Model



Set Generation Example

Set Generation Example

- ❑ **ASP Tool Screenshot**

driver_pin

endpoint

Tdelay, tau1, tau2, Q
current parameters

```
generate_SET_glitch -scenario ASU_2bufs/U1/Y ASU_2bufs/U2/A 0.1n  47p  347p  700f -corner 0
DEBUG: vector2Req 0.121528, vector2slew 0.005000, vector2outputcapacitance 0.011520
DEBUG: vector3Req 0.414434, vector3slew 0.010000, vector3outputcapacitance 0.005760
DEBUG: vector4Req 0.183335, vector4slew 0.010000, vector4outputcapacitance 0.011520
DEBUG: Maximum PullDown Resistance: 0.530368 KOhms
DEBUG: Probe Edge Lower Time 1.03884e-10
DEBUG: Probe Edge Delay Time 1.22646e-10
DEBUG: Probe Edge Upper Time 1.62254e-10
DEBUG: Stored Probe Rise Edge (0) Slew 5.83705e-11 and Arrival 1.22646e-10
DEBUG: Probe Edge Upper Time 2.84014e-10
DEBUG: Probe Edge Delay Time 4.9978e-10
DEBUG: Probe Edge Lower Time 1.05848e-09
DEBUG: Stored Probe Fall Edge (0) Slew -7.74464e-10 and Arrival 4.9978e-10
Rise Edges:
--------------------------------------
0. Slew: 0.052236, Arrival: 0.122646
--------------------------------------
Fall Edges:
--------------------------------------
0. Slew: 0.693077, Arrival: 0.499780
--------------------------------------
[73884ece3f7593b47b1ab3d8ab7ef250e93edf5e]%>
```

Set Generation Example

- ASP Tool Screenshot

driver_pin

endpoint

Tdelay, tau1, tau2, Q current parameters

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DEBUG: Probe Edge Lower Time 1.05848e-09
DEBUG: Stored Probe Fall Edge (0) Slew -7.7 ... Arrival 4.9978e-10
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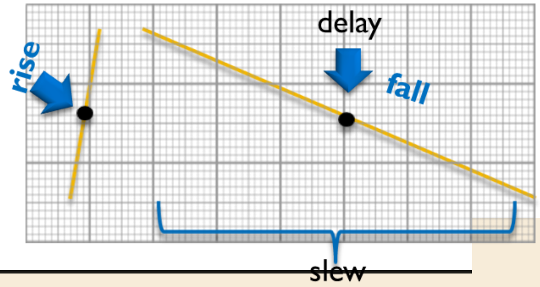
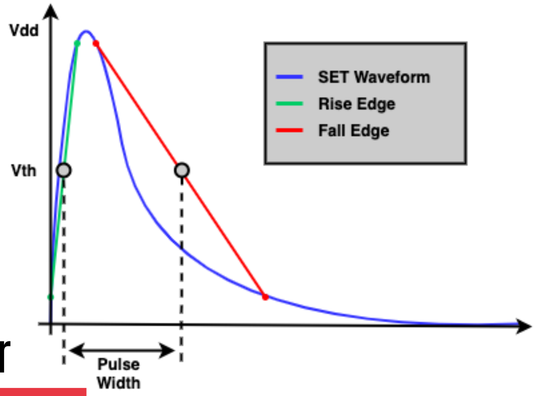
--------------------------------------
[73884ece3f7593b47b1ab3d8ab7ef250e93edf5e]%>
```

Endpoint Measurements



SET Generation Results VS. SPICE



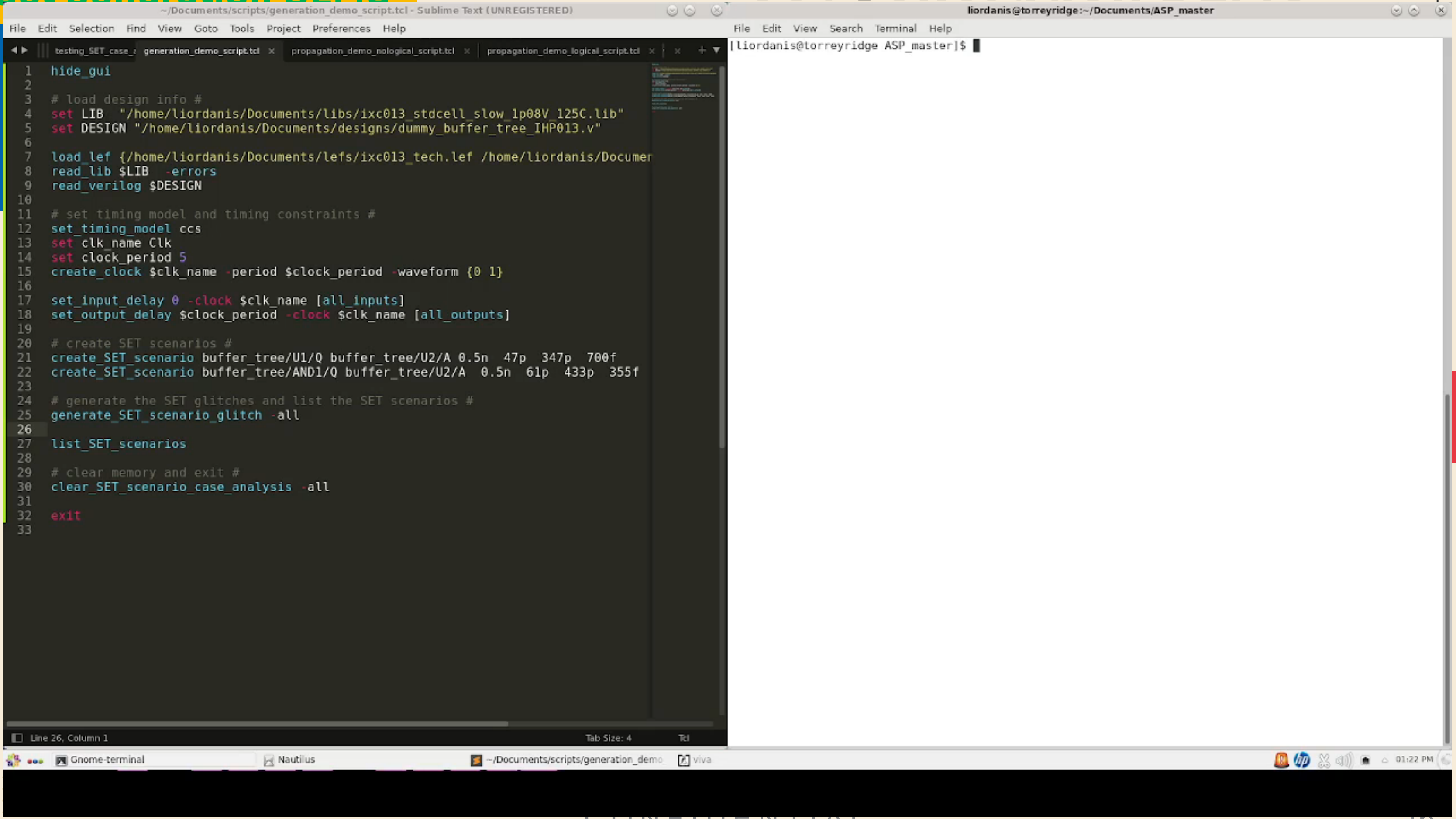
Req Error Analysis

Vdd as Reference Signals (2394 Req Sweep Experiments)	Average error (- = pessimistic, + = optimistic)
Fall Arrival	**-38.41%**
Fall Slew	**-94.63%**
Rise Arrival	**-5.7%**
Rise Slew	**33.5%**

Best Req Error

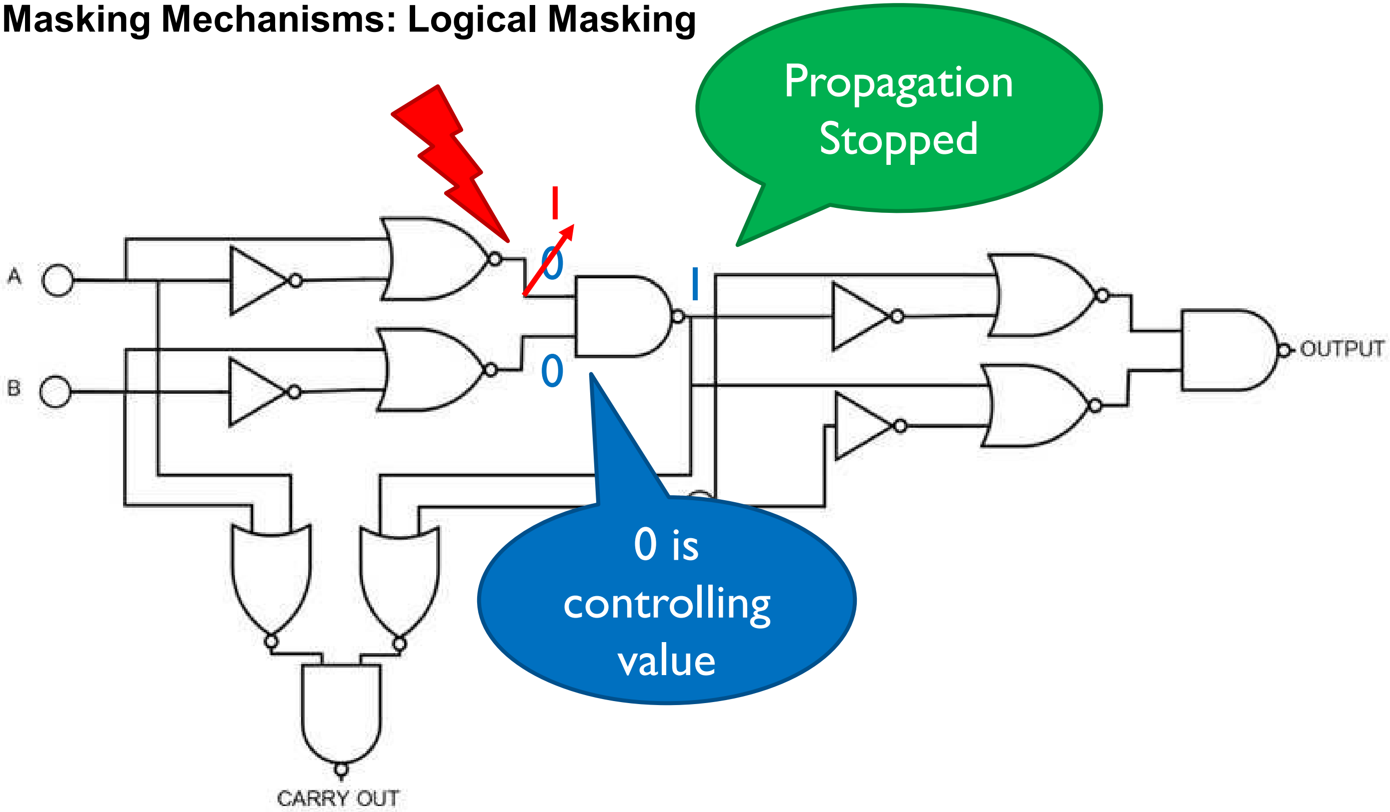
Full Swing Signals	Error vs. SPICE (minimum)
Fall Arrival	**9.28e-04%**
Fall Slew	**-0.144%**
Rise Arrival	**-7.24e-04%**
Rise Slew	**0.07%**

Set Generation DEMO



Set Propagation

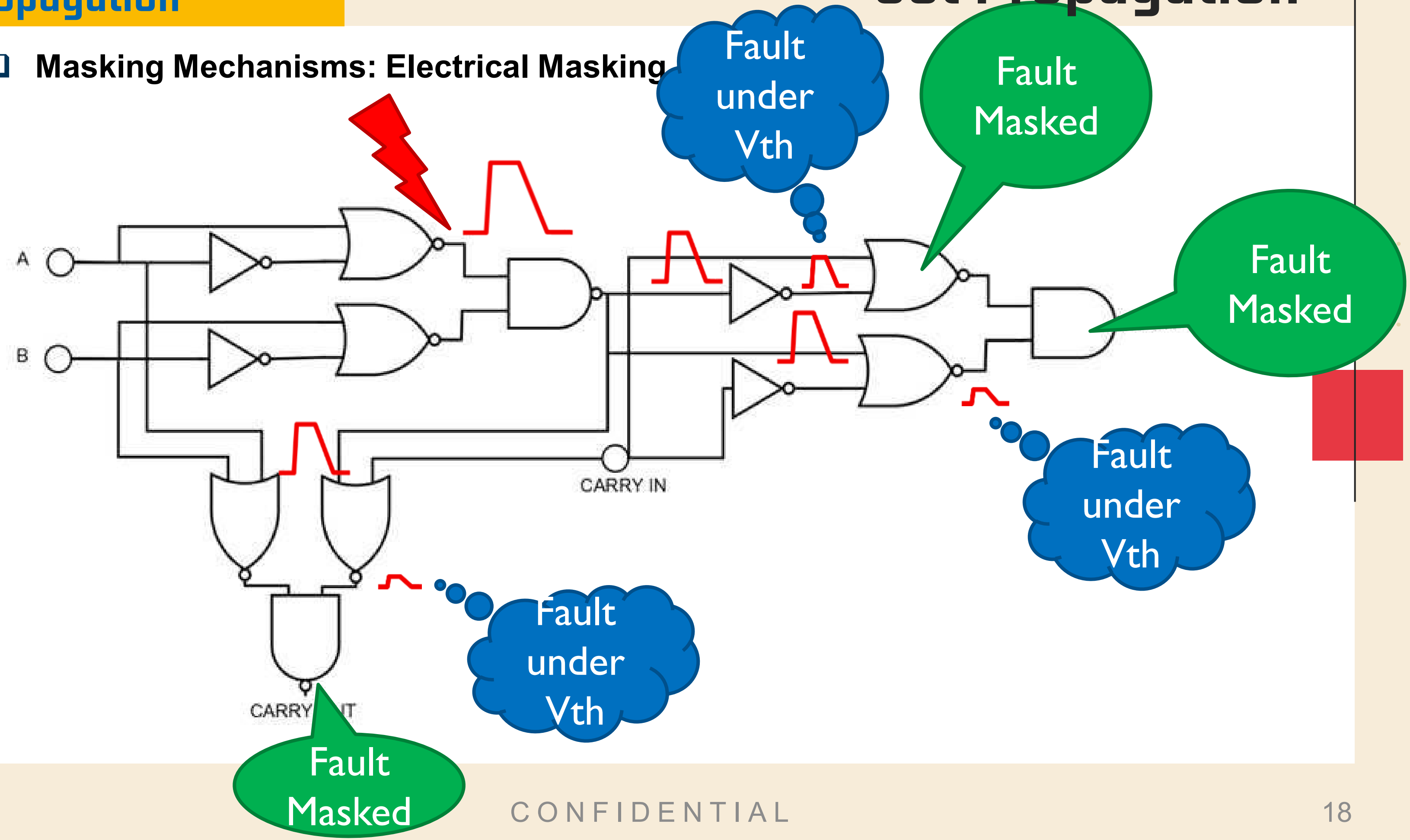
- Masking Mechanisms: Logical Masking



Set Propagation

Set Propagation

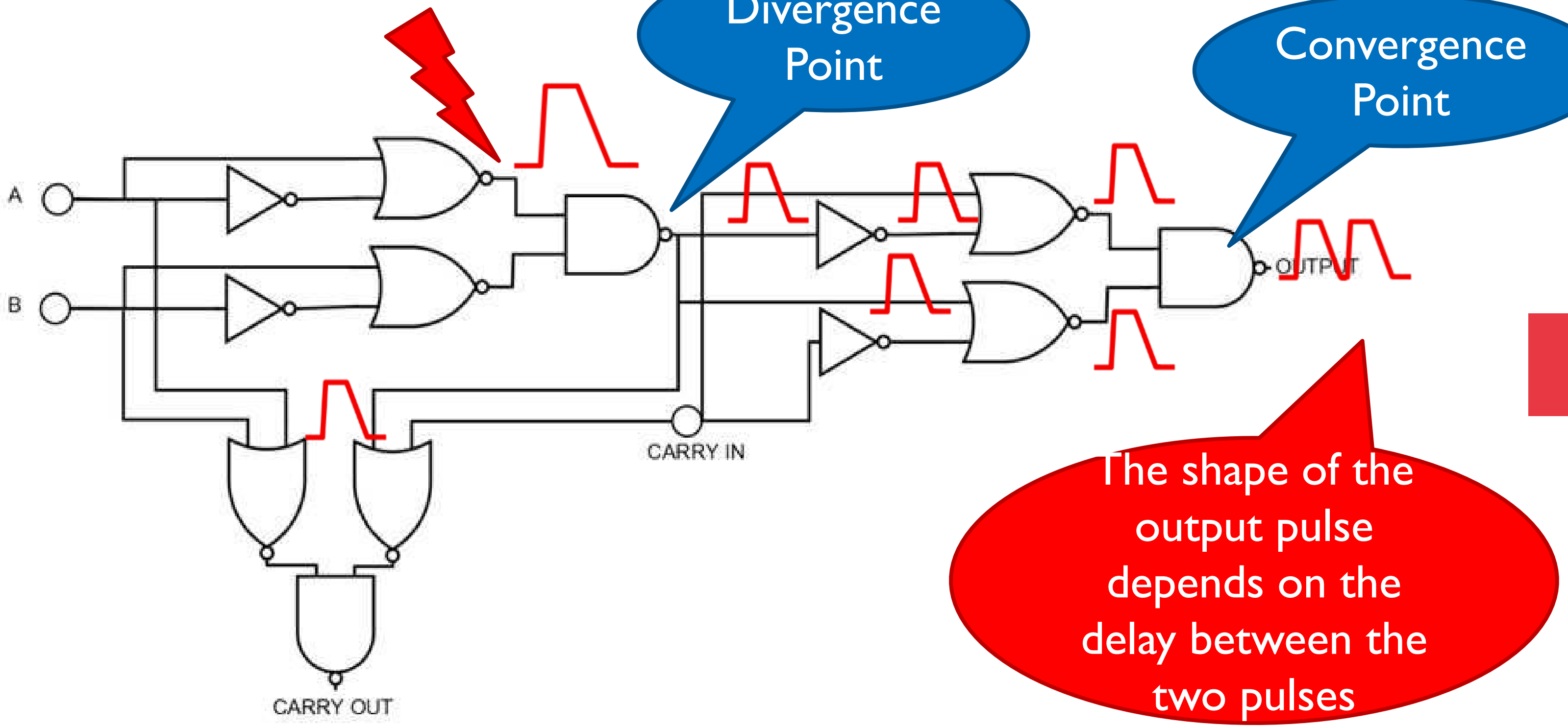
- Masking Mechanisms: Electrical Masking



Set Propagation

Set Propagation + Reconvergence!

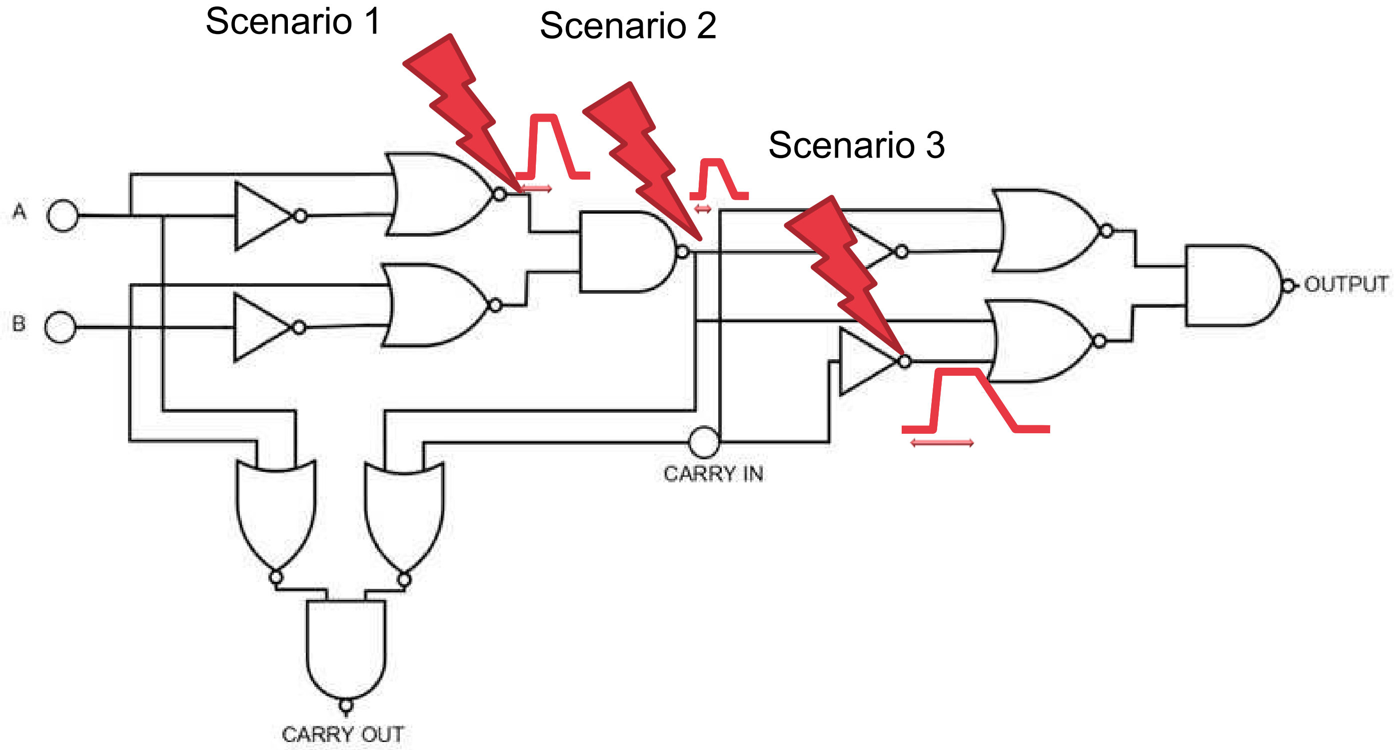
- Masking Mechanisms: Electrical Maski



SET Flow

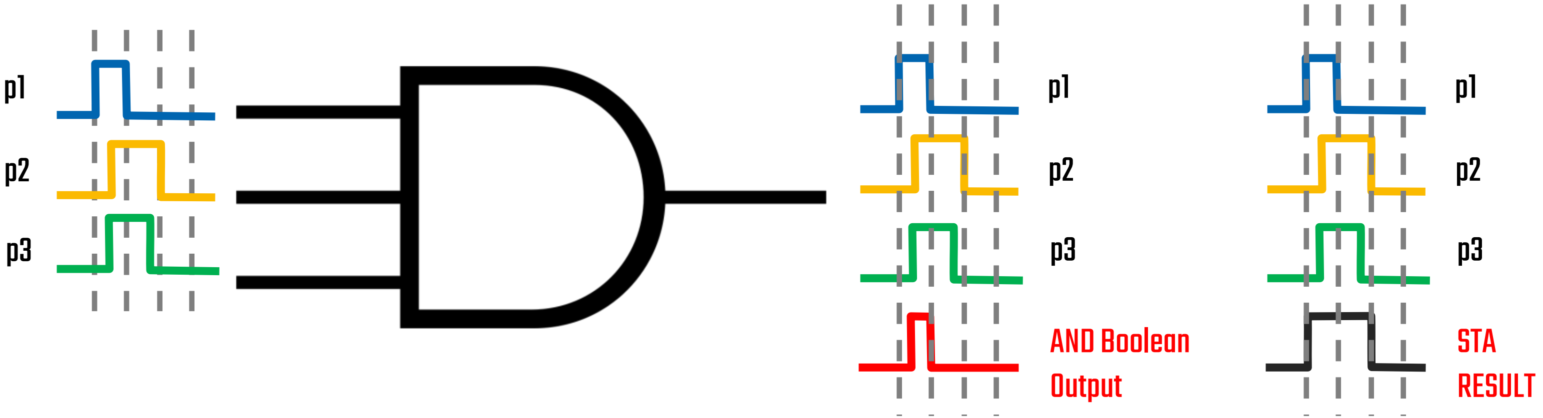
Set Scenarios

- Simulate multiple SETs in the same design
- Different Double Exponential current injection per SET



Set Propagation

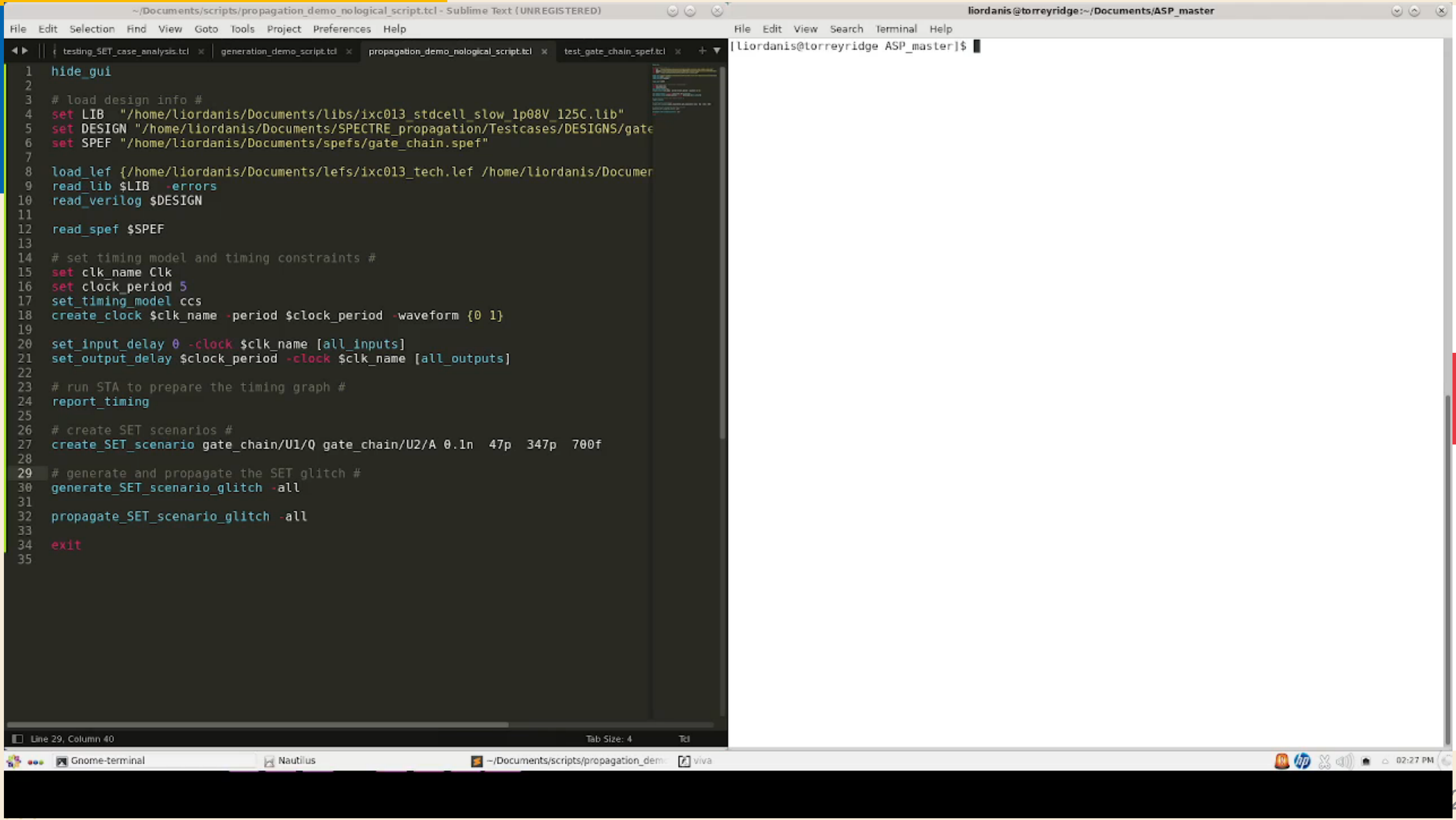
- STA Merges Pulses, based on Worst-case Timing!!!
- Here p1, p2, p3 arrive from SET Generation point @ AND inputs:



- STA does not take into account Boolean values for edge propagation
- Propagates $MAX(earliest\ rise, latest\ fall), MAX(earliest\ fall, latest\ rise)$
- Depending on Gate Unateness

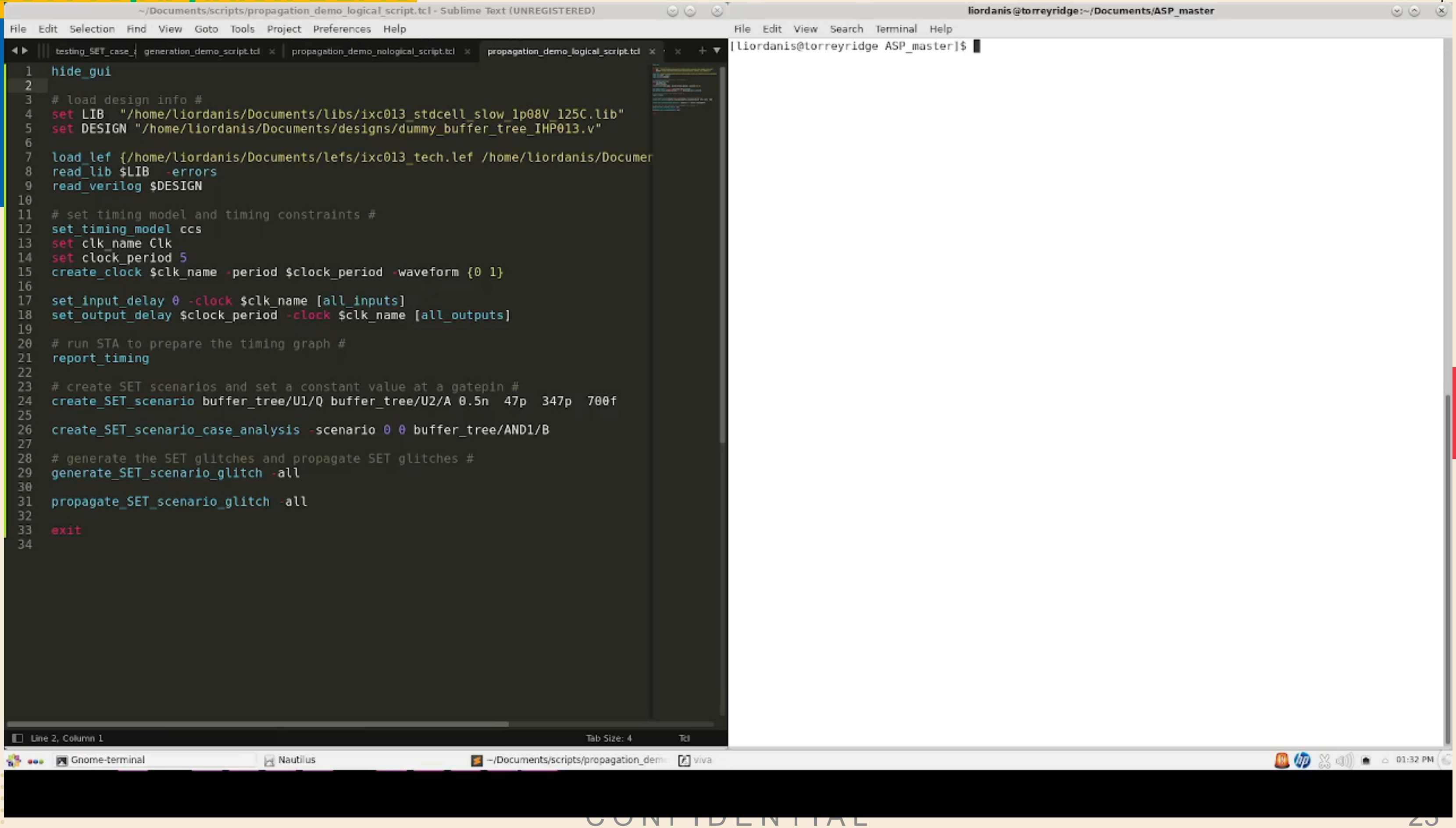
Set Propagation DEMO

Set Propagation DEMO 1 – No Logical Masking



Set Propagation DEMO

Set Propagation DEMO 2 – With Logical Masking



SET Propagation Results VS. SPECTRE - 1

SPECTRE Design	Rise Arrival (ns)	Rise Slew (ns)	Fall Arrival (ns)	Fall Slew (ns)	Pulse Width (ns)	Execution Time
800buf	58,24090	0,01700	72,55300	0,02120	14,31210	2h 17m
300buf	21,80190	0,01640	27,75580	0,01990	5,95390	18m 51s
200buf	14,50600	0,01470	18,79700	0,01630	4,29100	8m 30s
100buf	7,23025	0,01702	9,85192	0,02160	2,62167	2m 14s

ASP Req Design	Rise Arrival (ns)	Rise Slew (ns)	Fall Arrival (ns)	Fall Slew (ns)	Pulse Width (ns)	Execution Time
800buf	54,53018	0,01793	67,83548	0,02167	13,30530	1.730s
300buf	20,42540	0,01703	26,26638	0,02038	5,84098	0.43s
200buf	13,59925	0,01489	17,95487	0,01639	4,35562	0.35s
100buf	6,78687	0,01793	9,64884	0,02167	2,86197	0.21s

SET Propagation Results VS. SPECTRE - 2

SPECTRE Design	Rise Arrival (ns)	Rise Slew (ns)	Fall Arrival (ns)	Fall Slew (ns)	Pulse Width (ns)	Execution Time
800buf	**58,24090**	**0,01700**	**72,55300**	**0,02120**	**14,31210**	2h 17m
300buf	**21,80190**	**0,01640**	**27,75580**	**0,01990**	**5,95390**	18m 51s
200buf	**14,50600**	**0,01470**	**18,79700**	**0,01630**	**4,29100**	8m 30s
100buf	**7,23025**	**0,01702**	**9,85192**	**0,02160**	**2,62167**	2m 14s

ASP SPECTRE Pulse Design	Rise Arrival (ns)	Rise Slew (ns)	Fall Arrival (ns)	Fall Slew (ns)	Pulse Width (ns)	Execution Time
800buf	**54,53580**	**0,01793**	**67,37930**	**0,02167**	**12,84350**	1.640s
300buf	**20,43102**	**0,01703**	**25,81022**	**0,02038**	**5,37920**	0.290s
200buf	**13,60487**	**0,01489**	**17,49871**	**0,01693**	**3,89384**	0.180s
100buf	**6,79249**	**0,01793**	**9,19268**	**0,02167**	**2,40019**	0.04s

SET Propagation Results – AT & Slew Errors

AT Error	ASP rise AT Error	ASP fall AT Error	ASP SPECTRE Pulse rise AT Error	ASP SPECTRE Pulse fall AT Error
800buf	6,37%	6,50%	6,36%	7,13%
300buf	6,31%	5,37%	6,29%	7,01%
200buf	6,25%	4,48%	6,21%	6,91%
100buf	6,13%	2,06%	6,05%	6,69%
Averages	6,27%	4,60%	6,23%	6,93%

Slew Error	ASP rise Slew Error	ASP fall Slew Error	ASP SPECTRE Pulse rise slew Error	ASP SPECTRE Pulse fall slew Error
800buf	-5,44%	-2,24%	-5,44%	-2,24%
300buf	-3,82%	-2,41%	-3,82%	-2,41%
200buf	-1,29%	-0,57%	-1,29%	-3,87%
100buf	-5,32%	-0,34%	-5,32%	-0,32%
Averages	-3,97%	-1,39%	-3,97%	-2,21%

(- = pessimistic, + = optimistic)

SET Propagation Results – PW Errors

Pulse Width Error vs SPETRE	ASP	ASP SPECTRE Pulse
800buf	7,03%	10,26%
300buf	1,90%	9,65%
200buf	-1,51%	9,26%
100buf	-9,17%	8,45%
Averages	-0,44%	9,40%

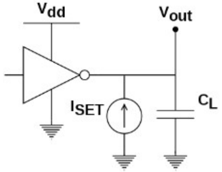
~5000 x

Speedup

ASP VS. PrimeTime *for SETs*

Features	Path-based SET Analysis using PrimeTime	ASP Tool
SET Generation	✗	✓
Pulse Propagation	✗	✓
Constant Node Support	✗	✓
Logical Masking (Primary Inputs Case Analysis)	✓	✓
Electrical Masking	✗	✓
Non Full-Swing Signals	✗	✓
Path Support	✓	✓
Non-Path, Logic Cone Support	✗	✓
Graph Based (High-Capacity)	✗	✓

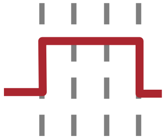
SET Propagation, Simulation Interaction



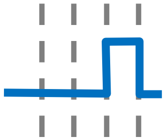
STA-based SET Generation

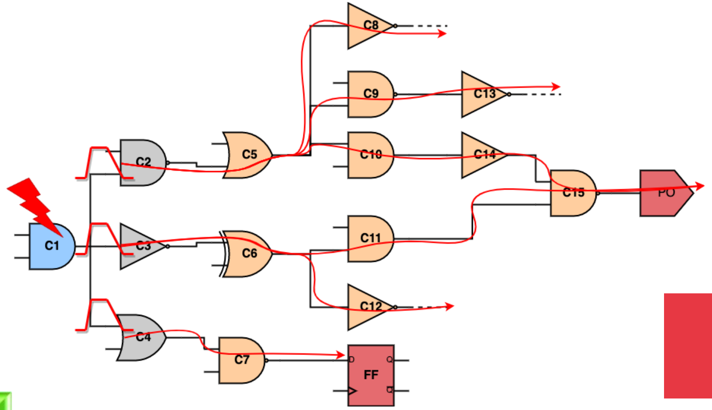
- **Calibration vs. SPICE/SPECTRE**
- **STA-based SET Propagation**
  - **Optimisations to Improve SER; Gate Upsizing, Buffer Insertion, *etc.***
  - **Simulation to Reduce Pulse Width Pessimism**

STA Pulse (WC)



Simulation Pulse
Vector Based





Thank You!

Questions?
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