Characterization of SET Effects in Electronic Integrated Circuits and Systems

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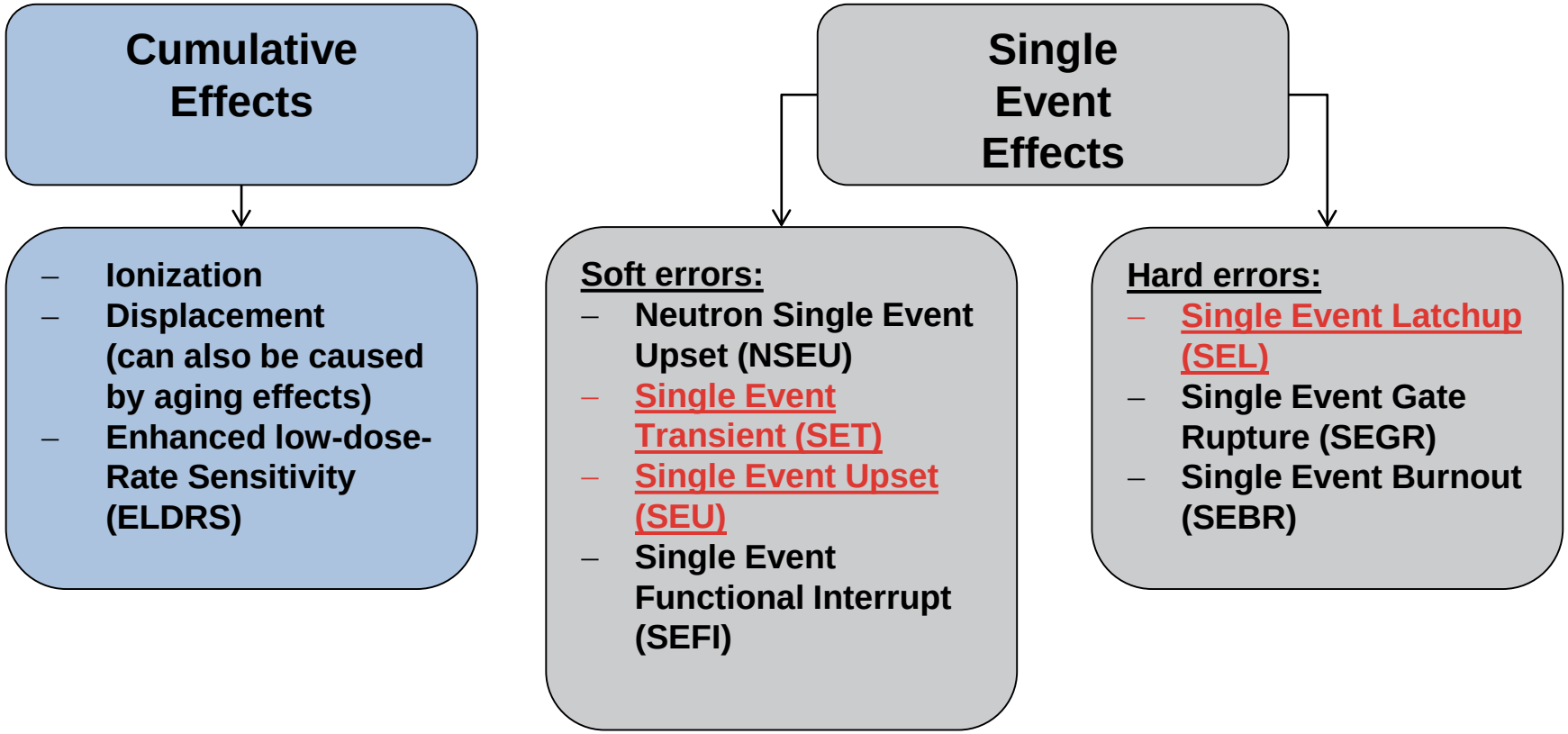
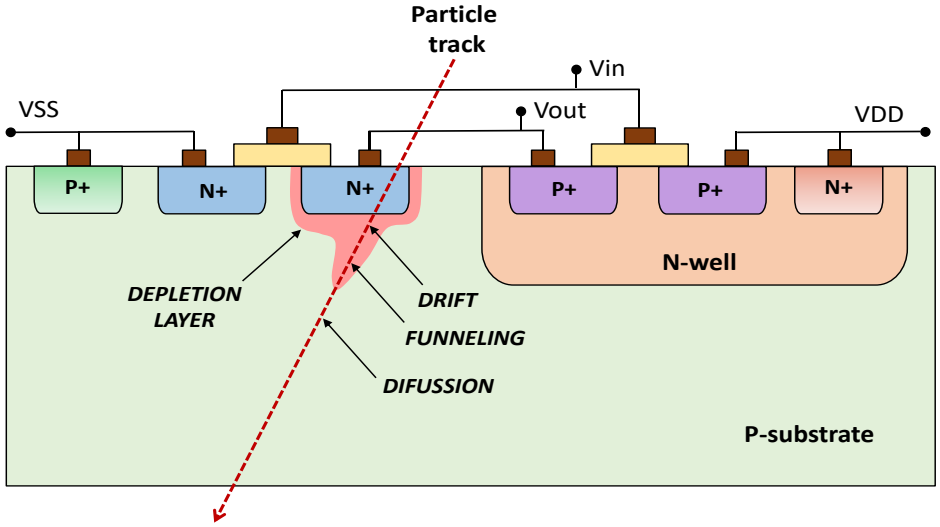
Outline

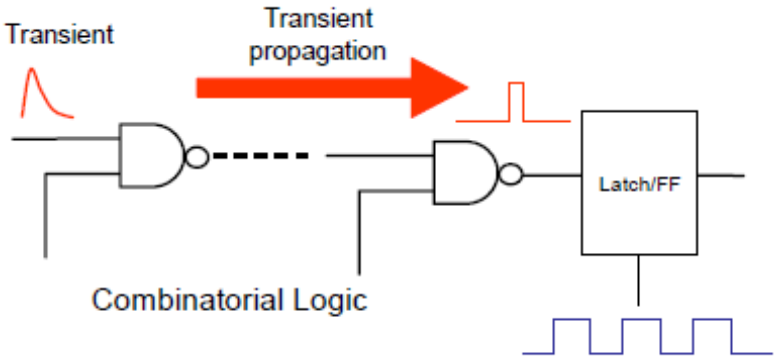
Radiation Effects



SET Effects

- Single event transients (SETs) are one of the major reliability issues for nano-scale integrated circuits operating in radiation environment
- SET is induced by the interaction of a high energy ionizing particle with a sensitive transistors in a combinational circuit



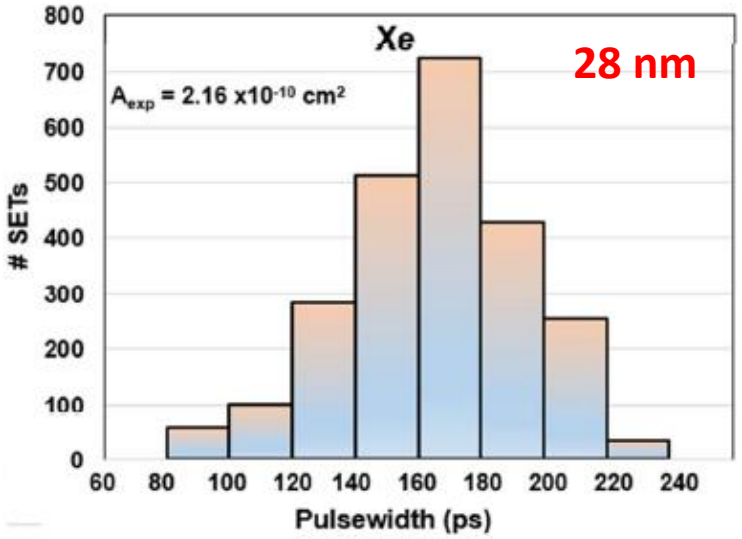


- SET is manifested as a voltage pulse at the output of a combinational gate
- If latched by a sequential element, SET can be transformed into a Single Event Upset (SEU), potentially resulting in data corruption

SET Pulse Width

- SET pulse width ranges from dozens of picoseconds to several nanoseconds
  - Due to random strike locations, it is not possible to obtain exact SET pulse values
  - A distribution of SET pulse widths can be obtained for a given particle energy
- SET pulse width decreases with technology scaling
  - But propagation delay also decreases, increasing the probability of SET propagation

Technology node	Reference	Maximum SET width at LET = 60 MeVcm^{2}mg^{-1}	Average SET width at LET = 60 MeVcm^{2}mg^{-1}
250 nm	Benedetto et al.	1.5 ns	n/a
180 nm	Benedetto et al.	1.5 ns	n/a
130 nm	Benedetto et al.	2.7 ns	n/a
	Narasimhan et al.	1.4 ns	650 ps
90 nm	Narasimhan et al.	1.4 ns	750 ps
65 nm	Gadlage et al.	200 ps	120 ps
	Jagannathan et al.	250 ps	175 ps
28 nm	Jagannathan et al.	230 ps	165 ps

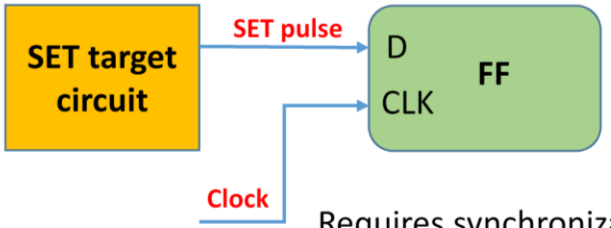


Jagannathan et al., in Proc. IRPS, 2016

SET Pulse Width Characterization

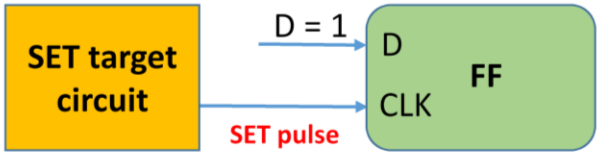
- **Characterization of the SET pulse width in standard cells is essential for evaluating the radiation-hardness of a given standard cell library (technology)**
- SET pulse width is characterized by exposing a target circuit (composed of standard cells) to heavy ion irradiation
- SET pulses generated in the target circuit are measured with a customized processing logic integrated on the same chip with the target circuit
- Two SET measurement approaches
  - Synchronous (requires relatively complex synchronization circuitry)
  - Asynchronous (simpler design) – adopted in this work

Synchronous SET measurement



Requires synchronization between SET pulse and Clock

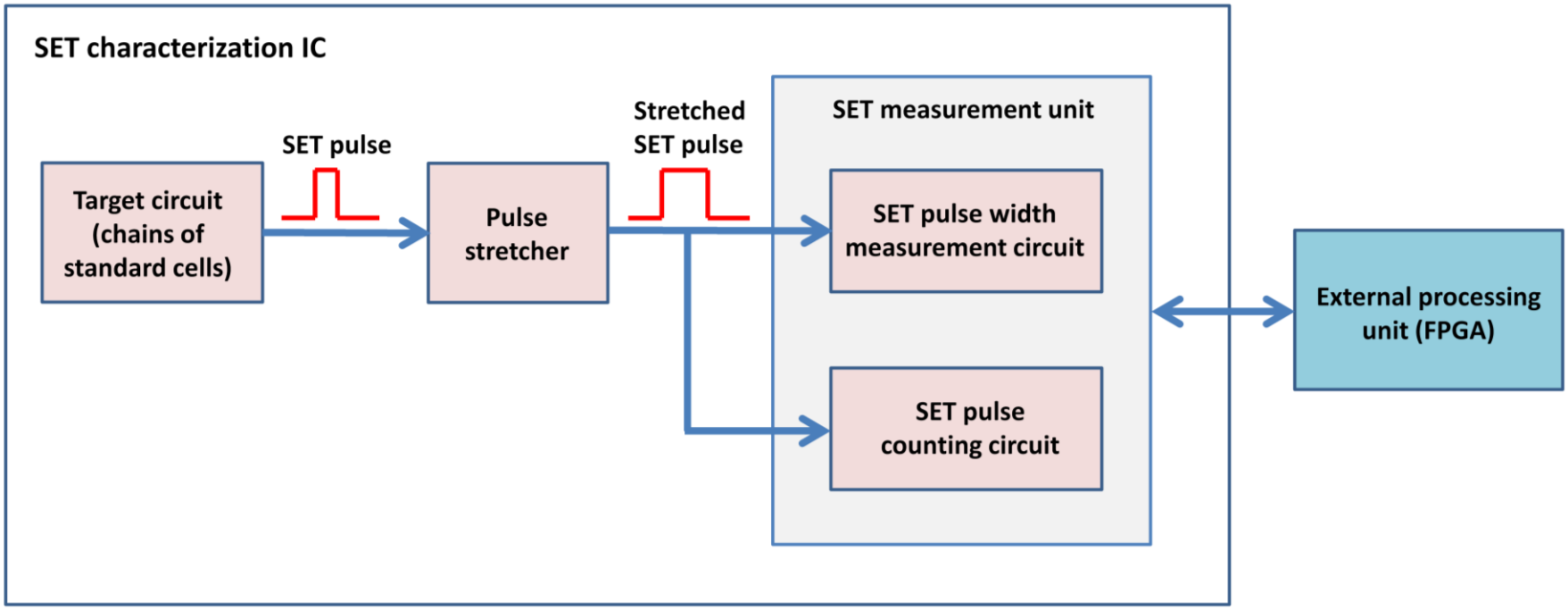
Asynchronous SET measurement



Requires reset after every detected SET pulse

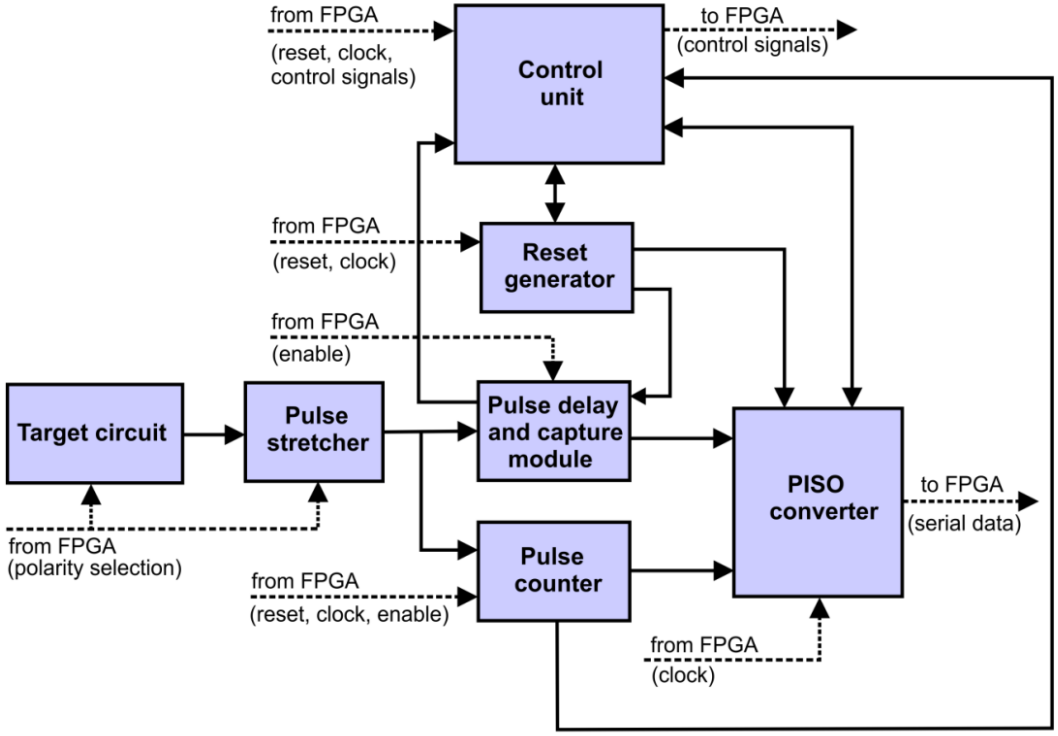
Hardware for SET Characterization (1)

- Main goals of SET characterization in standard cells
  - *Detection of SET pulses in standard cells*
  - *Measurement of SET pulse width*
  - *Counting of the detected SETs*



Hardware for SET Characterization (2)

- The SET pulse width measurement circuit is composed of 3 main functional units:
  - *Target circuit (SET detector)*
  - *Pulse stretcher*
  - *Processing unit*
- Supports the measurement of SET pulse widths from 0.1 ns to 3.5 ns
- Collected data is transferred to an external processing unit (FPGA)



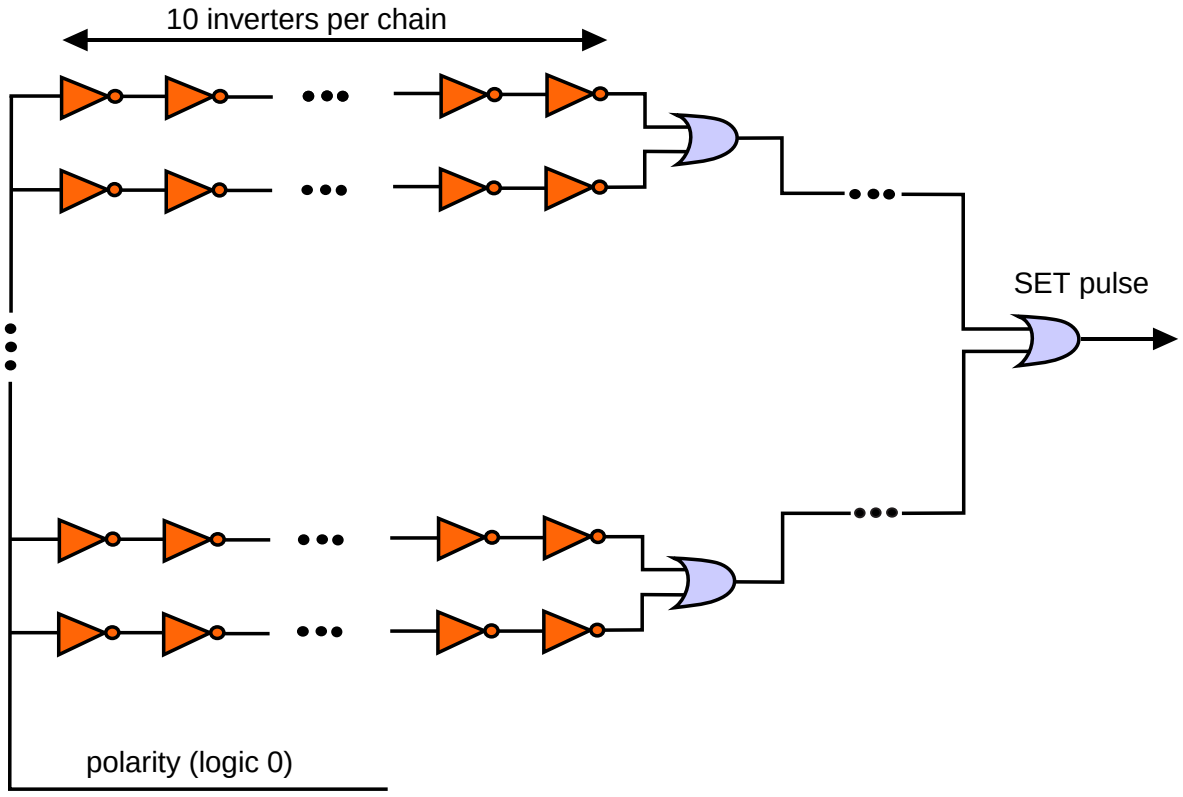
- External processing unit provides the necessary control signals for SET pulse width measurement

Target Circuit (1)

- Target circuit acts as a SET detector
- When hit by a radiation particle, the target circuit generates a voltage pulse at its output
- Target circuit is made of standard logic gates, usually inverters
- Key design requirements for the target circuit
  - *To secure significant detection area, the target circuit should be realized in the form of logic gate chains*
  - *To reduce the propagation-induced pulse broadening, the inverter chains should be as short as possible*
- Propagation-induced pulse broadening depends on technology and path composition
  - *Extensive simulations are necessary to identify the optimal conditions for achieving minimum pulse broadening*

Target Circuit (2)

- The target circuit is composed of 20480 inverters
- Inverters are arranged as 10-inverter chains interconnected by OR gates
- External signal is used to define the polarity of output SET pulse



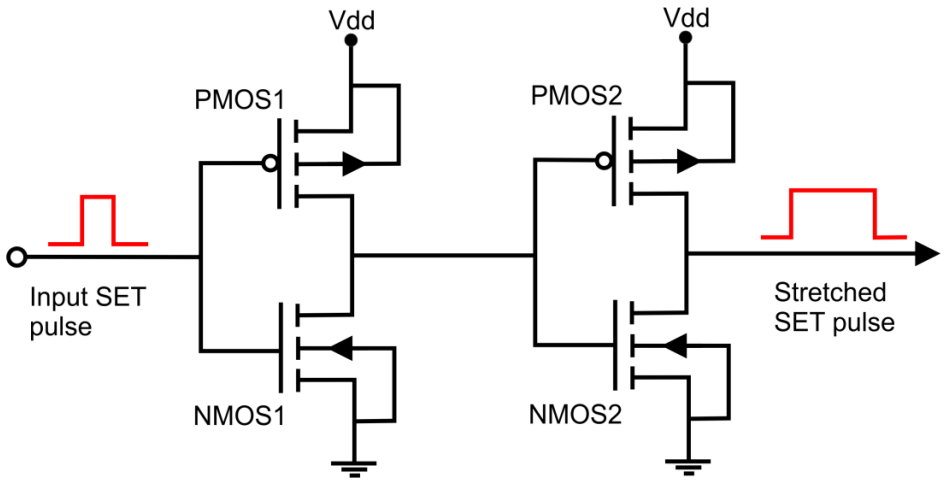
Target Circuit (3)

Gate	Gate area (μm^2)	Number of gates	Area of target circuit (μm^2)
INJILTX1	3.78	40960 (20 per chain x 2048 chains)	154829
INJILTX2	5.67	30720 (15 per chain x 2048 chains)	174182
INJILTX4	9.45	20480 (10 per chain x 2048 chains)	193536
INJILTX8	15.12	12288 (6 per chain x 2048 chains)	185795

Area of OR tree is 9.5 x 2047 = 19446 μm^2 (around 20% of target circuit)

Pulse Stretcher (1)

- To measure short SET pulses (< 200 *ps*), the pulses from the target circuit are stretched by 500 *ps*
- A pulse stretcher based on two asymmetrically sized inverters is used



- Pulse stretcher provides a fixed stretching independently of the input pulse width
- Pulse stretching is determined by
  - *Sizing ratio of the two-inverter stretcher*
  - *Number of cascaded two-inverter stretchers*

Pulse Stretcher (2)

Criteria for transistor sizing for a positive pulse stretcher

$$W_{NMOS1} > W_{PMOS1}$$
$$W_{PMOS2} > W_{NMOS2}$$
$$W_{NMOS1} = W_{PMOS2}$$
$$W_{PMOS1} = W_{NMOS2}$$

Relation between input and output pulse widths

$$T_{OUT} = T_{IN} + \Delta T$$

Pulse stretching

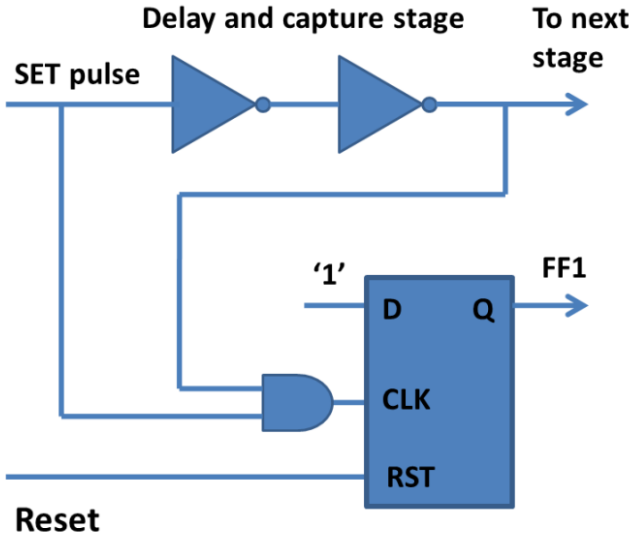
$$\Delta T = k \cdot S$$

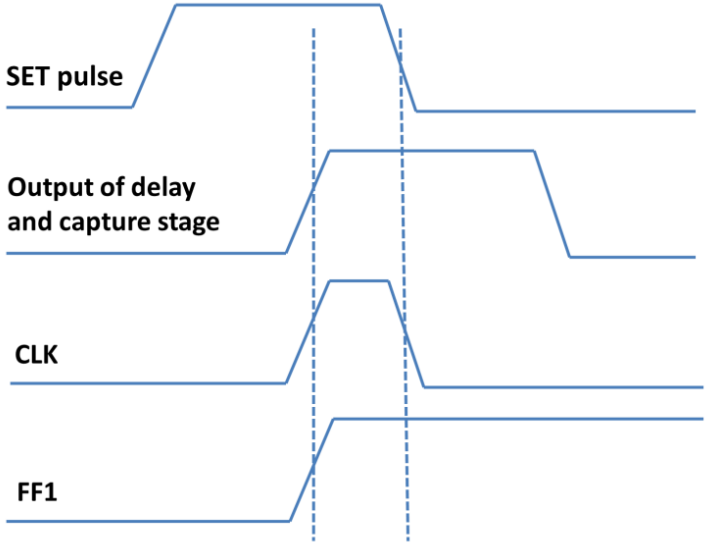
Sizing factor of pulse stretcher

$$S = W_{NMOS1}/W_{PMOS1} = W_{PMOS2}/W_{NMOS2}$$

Delay and Capture Module (1)

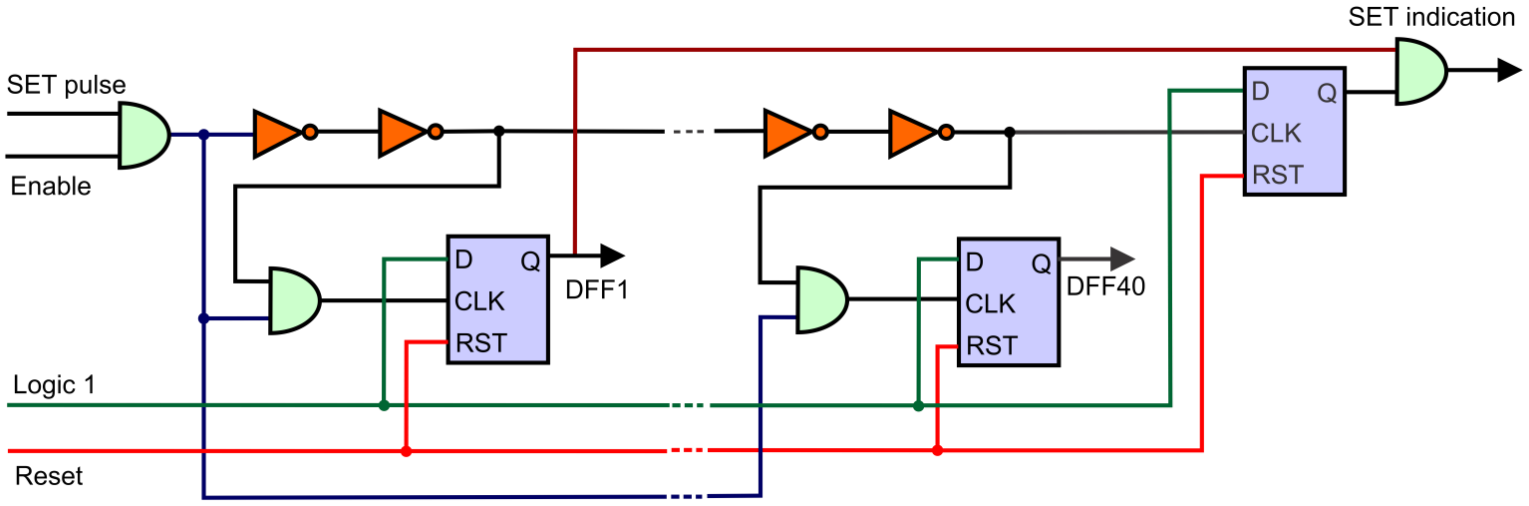
- Delay and capture module measures the width of the stretched SET pulse
- It is composed of cascaded delay inverters and capturing D flip-flops
- SET pulse width is proportional to the number of delay and capture units through which the pulses pass, i.e. number of triggered flip-flops
- Setting the flip-flops' data input D to the high level (logic 1) eliminates the need for additional synchronization circuitry





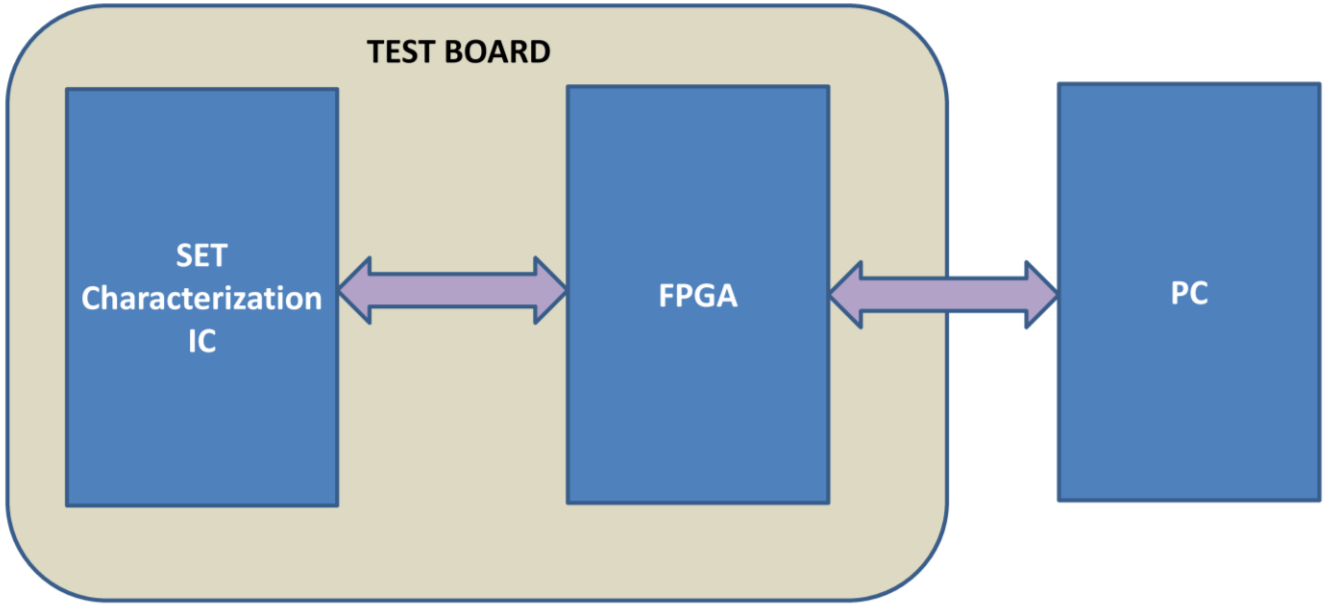
Delay and Capture Module (2)

- Delay and capture module is based on serial filtering approach, which employs fewer elements than parallel filtering approach
- Delay and capture module generates a 40-bit sequence equivalent to the SET pulse width
  - Generated sequence is in the form “11100…0”
  - SETs generated in the delay and capture module can be easily identified
- Measurement resolution is approx. 90 ps (total delay of two inverters with minimum driving strength in IHP’s 250 nm bulk CMOS technology)



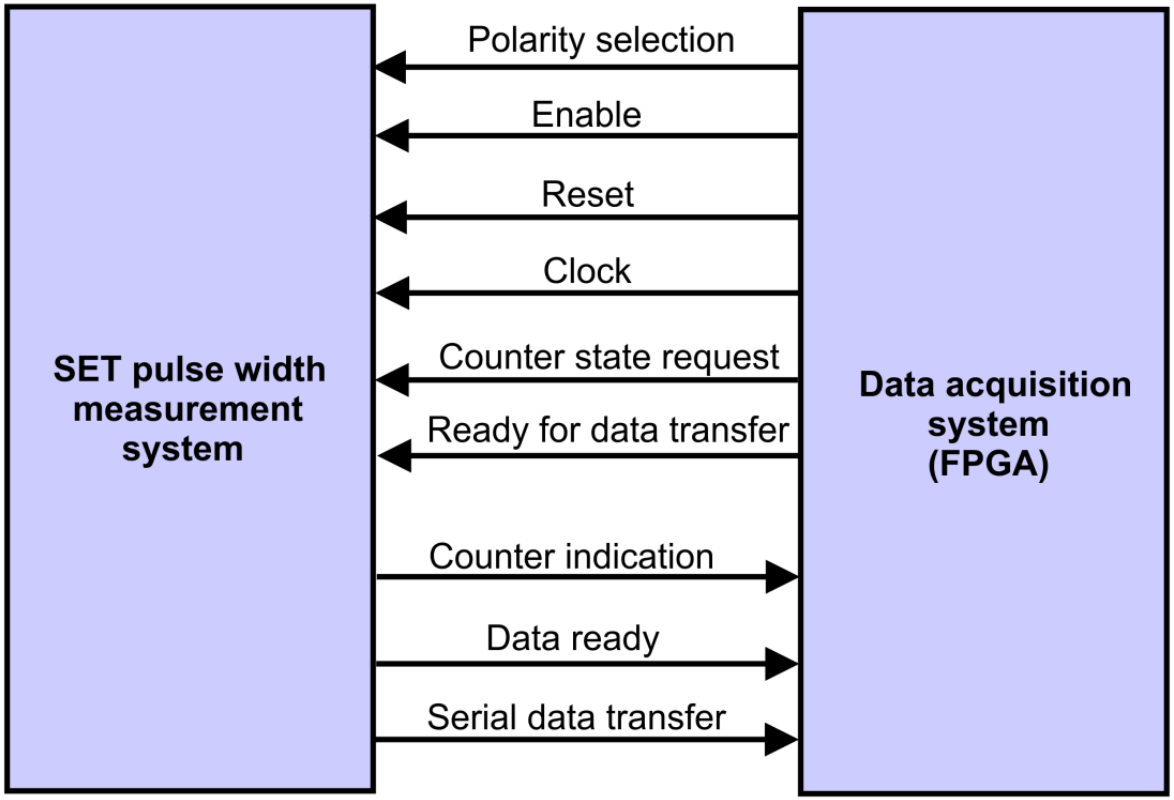
External Processing Unit (1)

- External processing unit is implemented on an FPGA
- FPGA transfers the acquired data (SET pulse width and number of detected SETs) to a PC
- FPGA provides the clock, reset and control signals for the SET pulse width measurement hardware



External Processing Unit (2)

- Data is transferred serially, in 44-bit packets (4-bit preamble + 40-bit data)
- Communication between the SET pulse width measurement hardware and the external data acquisition unit (FPGA) is defined by a handshaking protocol



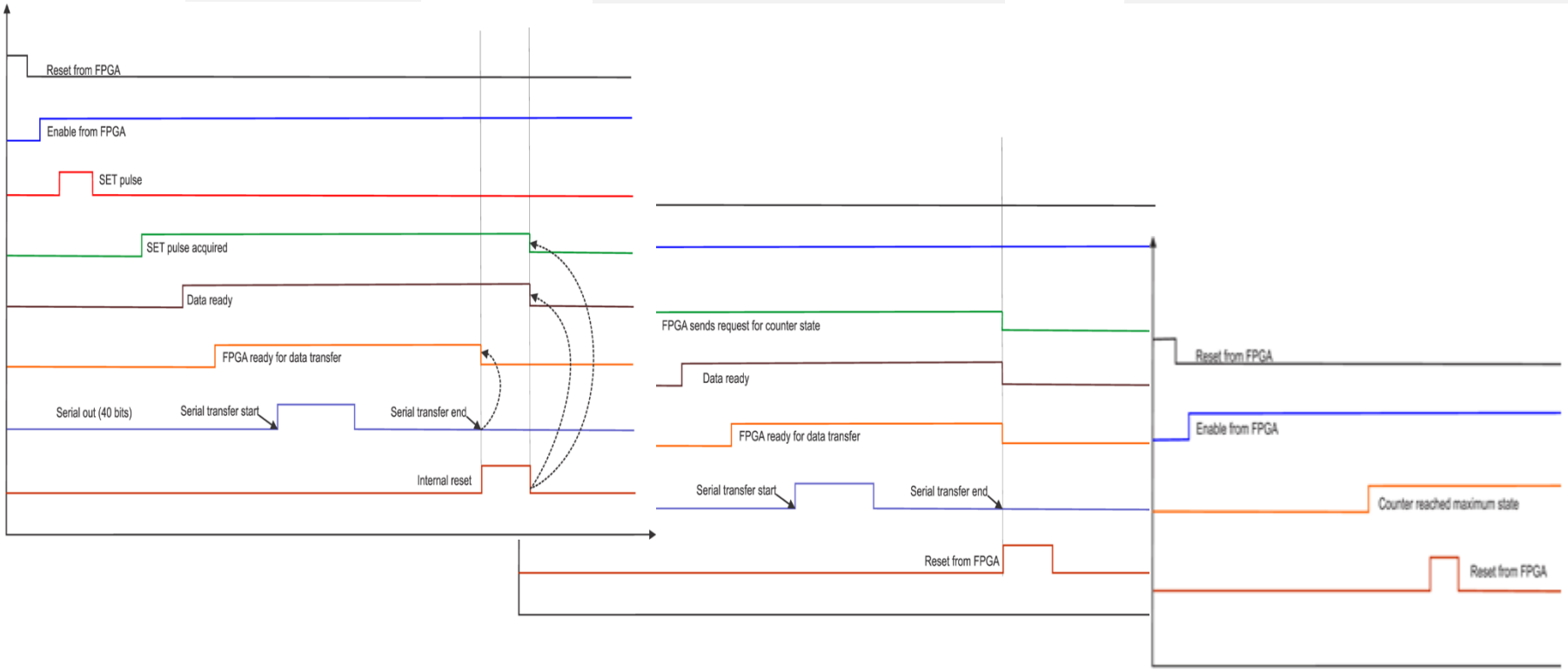
External Processing Unit (3)

- Implemented protocol supports 3 typical scenarios which can occur under real irradiation conditions

Scenario 1
SET is detected

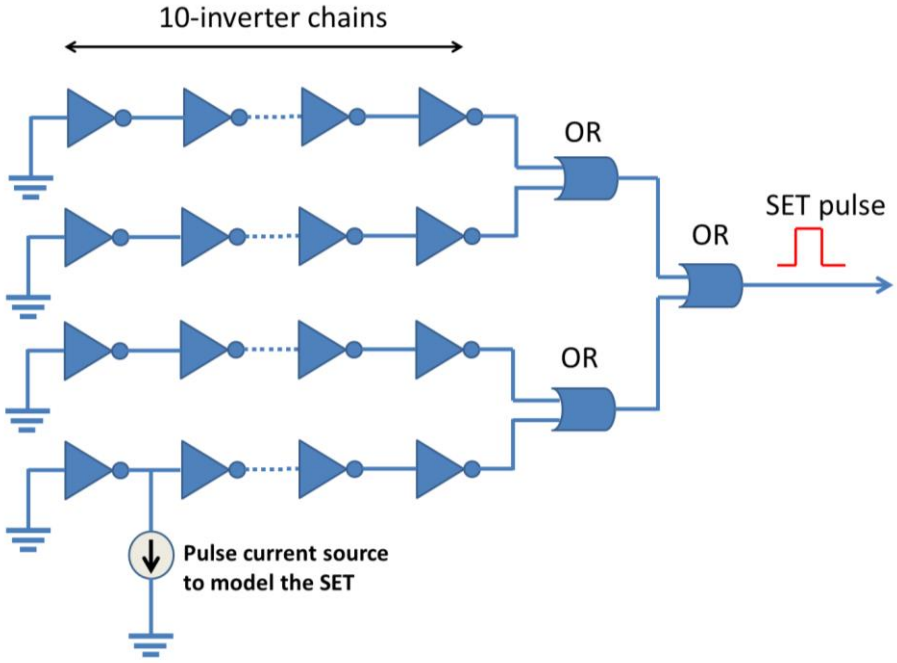
Scenario 2
FPGA requests counter state

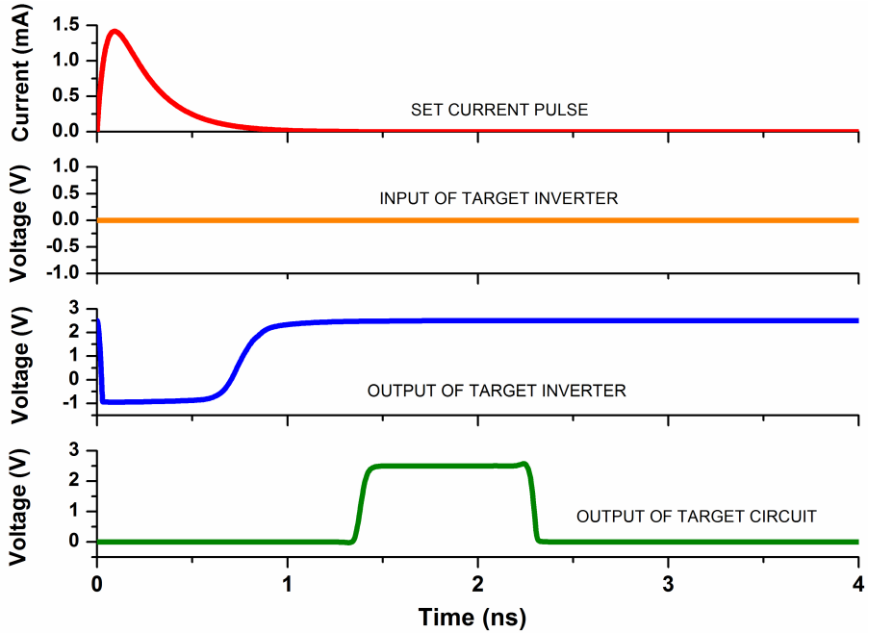
Scenario 3
SET counter reaches maximum



Performance Analysis (1)

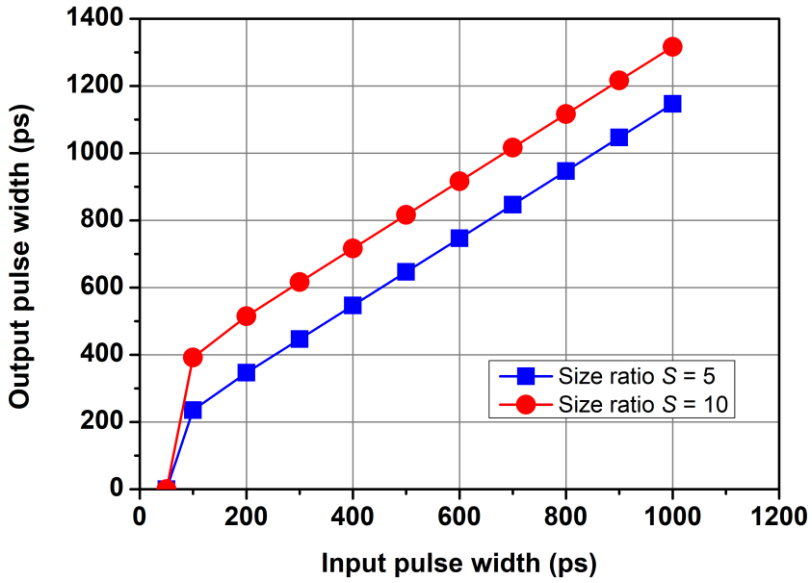
- To evaluate the operation of target circuit, a double exponential current pulse is injected at the output of target inverters
- The shape of the pulse at the output of target circuit is close to rectangular
- Minimum pulse broadening was noticed (due to OR gates)

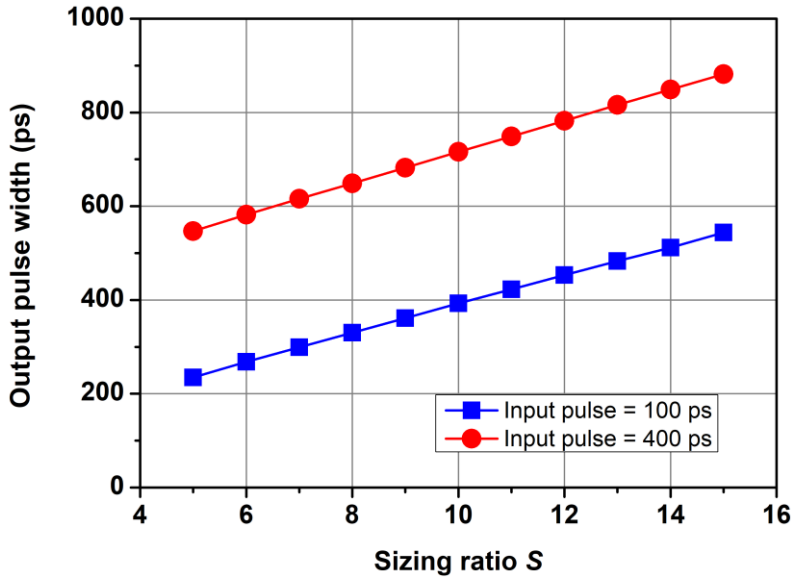




Performance Analysis (2)

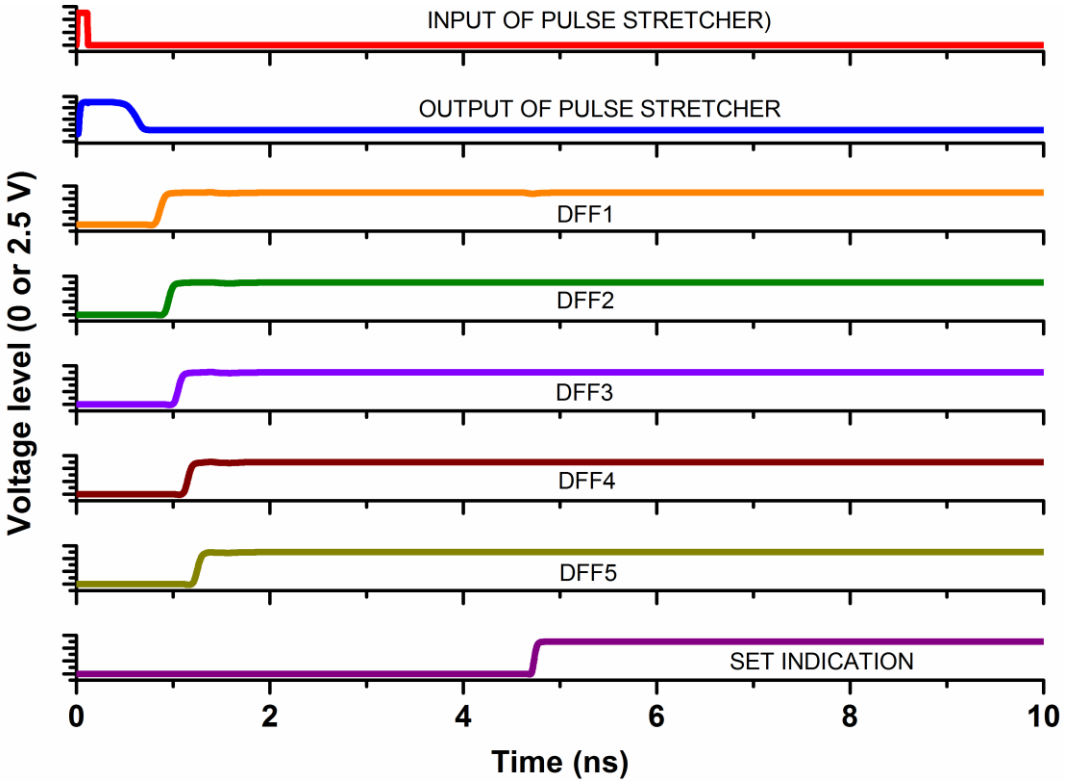
- To evaluate the performance of pulse stretcher, the relation between input and output pulse width in terms of sizing ratio was analyzed
- Pulse stretching is independent of input pulse width
- Output pulse width increases linearly with the sizing factor (transistor size) of pulse stretcher





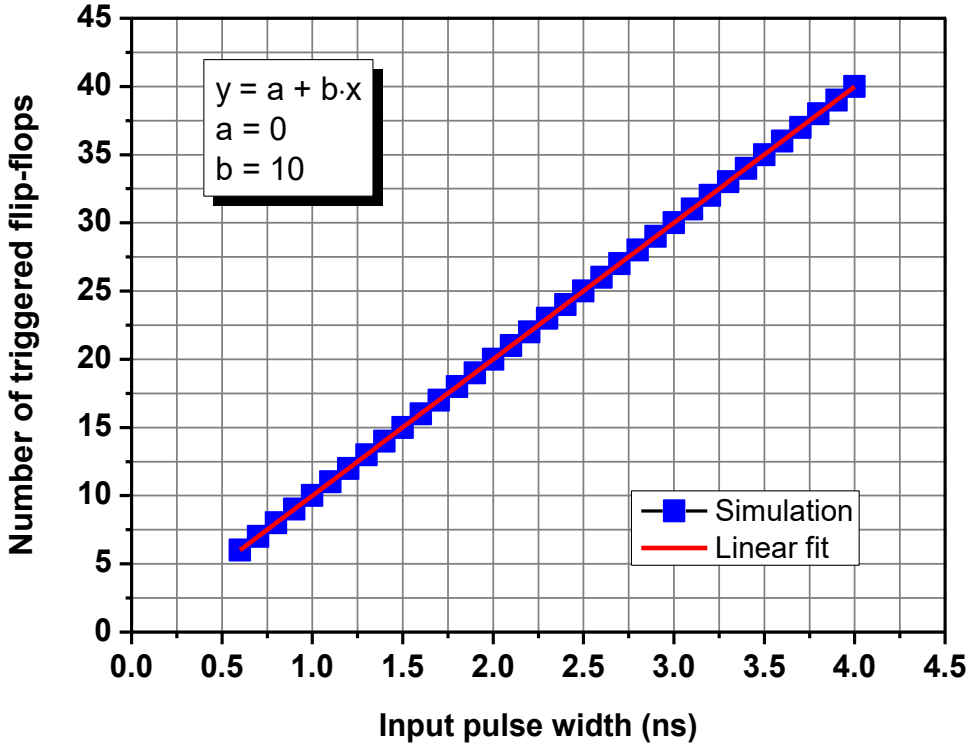
Performance Analysis (3)

- To evaluate the performance of the pulse stretcher and delay and capture module, a rectangular voltage pulse was injected at the input of pulse stretcher
- If at least one flip-flop in the delay and capture module is triggered, an SET indication signal will be issued



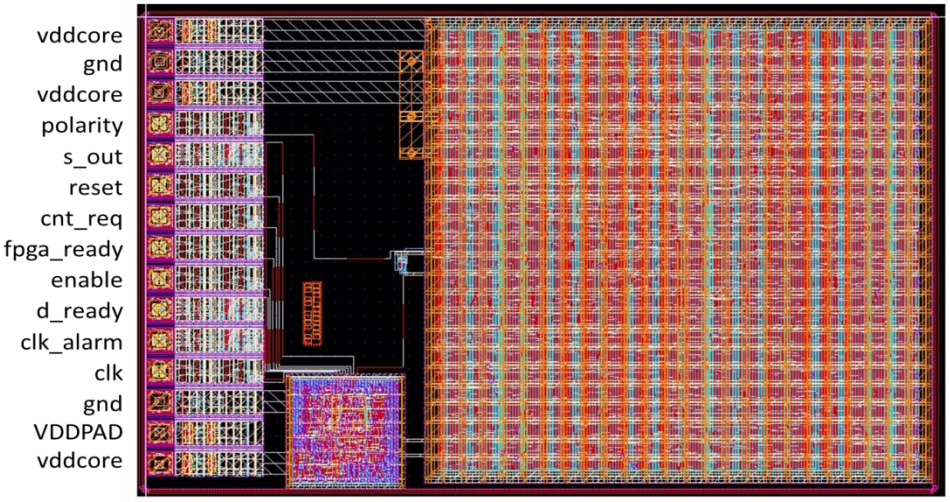
Performance Analysis (4)

- The number of triggered flip-flops in delay and capture module is linearly dependent on the input pulse width
- Since every pulse is stretched by 500 *ps*, it is possible to detect and measure effective pulse widths from 0.1 ns to 3.5 ns



Implementation Details

Parameter	Value
Technology	IHP 250 nm
Chip area	3.5 mm^2
No. of pads	15
Clock freq.	50 MHz
Core V_{DD}	2.5 V
I/O V_{DD}	3.3 V
Current	20.32 mA
Die thickness	300 µm



Thank you for your attention!

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