# 3rd ELICSIR Workshop

## 17. and 18. November, 2021

# *Fault-tolerant Electronics for Radiation Environments*

innovations for high performance microelectronics

UNIVERSIDAD DE GRANADA

# Programme

## Wednesday, November 17th, 2020

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| 10:30 | **MORAL – Export-free Rad-hard Microcontroller for Space Applications**<br>*Felipe Augusto Kuentzer (IHP, Germany)* |
| 11:00 | **Design to Survive**<br>*Sergio Montenegro (University of Würzburg, Germany)* |
| 11:30 | *Break* |
| 11:40 | **Self-adaptive Single-Event Upset Resilience in Reconfigurable Systems for Space Applications**<br>*Junchao Chen (IHP, Germany)* |
| 12:10 | **Fault-tolerant Systems Based on Coding Techniques**<br>*Tatjana Nikolic (University of Nis, Serbia)* |
| 12:40 | *End of Day 1* |

## Thursday, November 18th, 2020

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| 10:30 | **Characterization of Single Event Transient Effects in Electronic Integrated Circuits and Systems**<br>*Zoran Stamenkovic (IHP, Germany)* |
| 11:00 | **Fault Analysis in Early Design Steps for AI Applications**<br>*Mladen Berekovic (University of Lübeck, Germany)* |
| 11:30 | *Break* |
| 11:40 | **An STA CAD Tool for SET Generation and Propagation**<br>*Christos Sotiriou (University of Thessaly, Greece)* |
| 12:10 | **Machine Learning Techniques to Estimate the Functional Failure Rate of Complex Circuits**<br>*Thomas Lange (IROC Technologies, France)* |
| 12:40 | *End of Day 2* |

# *Invited Talks*

## Talk 1

**Felipe Augusto Kuentzer (IHP, Germany)**

**Title**: ***MORAL - Export-free Rad-hard Microcontroller for Space Applications***

**Abstract:** The space segment of modern applications, opens a wide spectrum of possibilities compared to the current traditional approach. Small satellites now perform new tasks, especially on the constellation and swarm formations, and push forward cluster satellites formation that will replace large satellites. This market segment is one of the major targets of the EU Horizon 2020 MORAL project. This presentation shows an overview of the MORAL project and the different aspects involved in its development.

**Biography:** Felipe A. Kuentzer received a bachelor degree in Computer Engineering from the University of Santa Cruz do Sul (UNISC) in 2009. In 2014 he received his M.Sc. degree in Computer Science from the Pontifical Catholic University of Rio Grande do Sul (PUCRS) and later in 2018 the Ph.D. degree in Computer Science also from PUCRS. Since 2018 he has been with the University of Potsdam, Germany, where he is a Postdoc, and also with the IHP Microelectronics, Frankfurt (Oder), Germany, as a Guest Scientist.

## Talk 2

**Sergio Montenegro (University of Würzburg, Germany)**

**Title**: ***Design to Survive***

**Abstract:** In Space no one can hear your scream. If something goes wrong first you have to survive then ask for help and hope a help will come on time. We use (sometimes) robust devices (Radiation tolerant) but most of our devices are normal COTS which will fail, and even the robust devices will fail some day. It is better to know it and to be ready to detect anomalies and then to find a way to continue living until the last light goes off, than to try to avoid anomalies. You can do the first but you cannot do the second. In this presentation I will show our strategies to survive until the last light goes off.

**Biography:** Sergio Montenegro was born in Guatemala. Since 2010, he has been Professor of Aerospace Information Technology at the University of Würzburg. He develops control systems for satellites, drones, aircraft, underwater vehicles, etc. He also works on reliable systems and survival machines. Previously he was with the Fraunhofer Gesellschaft and the German Aerospace Center (DLR - Space System).

## Talk 3

**Junchao Chen (IHP, Germany)**

**Title:** ***Self-adaptive Single-Event Upset Resilience in Reconfigurable Systems for Space Applications***

**Abstract:** Due to the downscaling of CMOS technologies, the design of Integrated Circuits (ICs) for space missions becomes more and more challenging. Radiation-induced Single Event Upsets (SEUs) caused by high-energy particles could cause circuit soft faults, and lead to data corruption and system failures. The intensity of cosmic radiation may differ over five orders of magnitude within a few hours or days during the Solar Particle Events (SPEs), thus increasing for several orders of magnitude the probability of SEUs in space-borne electronic systems. Generally, designers apply static mitigation techniques to achieve reliable designs based on the worst radiation conditions, but this causes resource overhead and is unnecessary most time. To overcome this issue, firstly, we proposed an embedded low-cost SRAM-based SEU monitor for in-flight detection, which could measure the real-time upset rate of SRAM. Secondly, in order to achieve efficient SEU mitigation and maintain the functionality of the system, it is necessary to enable the real-time flux variations prediction, i.e., to predict the upcoming SPEs. By analyzing radiation flux during historical solar events with supervised machine learning and proposed SEU monitor, an offline-training-online-adjustment module is obtained to predict SPEs and SEUs variations at least one hour in advance. Finally, the proposed design is integrated into the highly dependable and self-adaptive reconfigurable system, allowing to trigger the radiation mitigation mechanisms before the onset of high radiation levels.

**Biography:** Junchao Chen received the M.Sc. degree in electronic engineering from Politecnico di Torino, Italy, in 2017. Since February of 2018, he has been funded by the Maria Skłodowska-Curie RESCUE ETN project and employed as a member of Prof. Krstic research group in IHP Microelectronics, Frankfurt (Oder), Germany. His research has focused on exploring self-adaptive fault-tolerance mechanisms in multi-core processing architectures, which are backbones of the modern embedded systems. The goal is to enable and explore the dynamic trade-off between reliability, performance and power consumption in the relevant critical applications, such as space applications. He has proposed design of low-cost single-event upset monitor and a machine learning method for solar particle events event with several publications, as well as one patent of “electronic circuit with integrated SEU monitor”. Currently, he is working on the self-adaptive multi-core system design based on the RISC-V.

## Talk 4

**Tatjana Nikolic (Faculty of Electronic Engineering, University of Nis, Serbia)**

**Title:** ***Fault-tolerant Systems Based on Coding Techniques***

**Abstract:** Contemporary electronic systems are becoming more complex and increasingly sensitive to transient faults caused by cosmic rays and alpha particles. The engineering response to these challenges is to build systems that will acknowledge the existence of faults and incorporate

techniques to tolerate these faults, while still providing an acceptable level of service. This presentation considers fault-tolerance design techniques for improving reliability of both computation and communication architectures. The focus will be on the following two techniques: self-checking circuits and coding schemes for fault-tolerance. Self-checking circuits are an efficient but expensive mechanism that relies on hardware replication to enable instantaneous detection of transient faults in critical parts of complex systems. On the other hand, error-correcting codes require much less redundancy, while representing an elegant and technology-independent approach that can provide a common framework for jointly optimizing design for energy efficiency, speed, and reliability. The fault-tolerance capabilities of coding techniques will be demonstrated in the context of a communication architecture based on the CDMA bus. In the proposed system, a specific coding scheme is used both to allow simultaneous transmission of data over a common bus and to meet stringent requirements for fault-tolerant data transmission.

**Biography:** Tatjana Nikolic received her BS degree in communication engineering, and her MS and PhD degrees in electronic engineering from the Faculty of Electronic Engineering, University of Nis, Serbia, in 2000, 2005, and 2010, respectively. She is currently an associate professor with the Department of Electrical Engineering at the Faculty of Electronic Engineering, University of Nis, Serbia. Her research interests include fault-tolerant on-chip communication, low-power system-on-chip design, and reconfigurable hardware architectures for application-specific acceleration.

## Talk 5

**Zoran Stamenkovic (IHP, Germany)**

### Title: *Characterization of Single Event Transient Effects in Electronic Integrated Circuits and Systems*

**Abstract**: The presentation first introduces and describes radiation effects in electronic integrated circuits and systems. It focuses on single event transient (SET) pulse characterization and necessary hardware for this characterization. The proposed hardware has been used to evaluate SET effects in IHP's 250 nm bulk CMOS digital standard cells. It is composed of an inverter-based target circuit, a pulse stretcher and a processing unit for counting the SET pulses and measuring the SET pulse width. This small measurement system is based on the combination of best practices from various existing designs, and it has a simple architecture capable to provide the reliable SET characterization. It supports serial interfacing with the external data acquisition unit that transfers the acquired data to the personal computer. The circuit-level simulations have demonstrated detection and measurement of the SET pulse widths from 100 ps up to 3.5 ns, with a measurement resolution of approximately 100 ps.

**Biography:** Dr. Zoran Stamenkovic is a scientist at the IHP GmbH, Frankfurt (Oder), Germany. He acquired his PhD degree in electronic engineering from the University of Nis, Serbia in 1995. Dr. Stamenkovic has published more than 150 scientific book chapters, theses, journal papers and conference papers, and given more than 25 invited talks in the field of design and test of integrated

circuits and systems. He is the lead editor (and a co-author) of the book *Silicon Systems for Wireless LAN*. His research interests include hardware/software co-design, SOC design for wireless communications, fault-tolerant circuits and systems, and integrated circuit yield and reliability modelling. He serves as a program committee member of many scientific conferences (among them DDECS, IOLTS, EWDTS, DTIS, MIEL, and TELFOR). Dr. Stamenkovic was the general chair of DDECS15 and the program chair of DDECS18 and DDECS20. He is a regional editor of the Journal of Circuits, Systems, and Computers and a senior member of the IEEE.

## Talk 6

**Mladen Berekovic (University of Lübeck, Germany)**

**Title**: ***Fault Analysis in Early Design Steps for AI Applications***

**Abstract**: AI safety engineering is considered one of the important domains that analyze and evaluate faults in early design stages. In this talk the concept of fault analysis of AI applications is presented. The preliminaries and basic definition of the fault, error, and failure will be investigated Regarding AI applications. A case study by using a system model will be presented to show a practical approach of fault injection evaluation for AI.

**Biography:** Prof. Berekovic is director of the Institute for Computing Engineering at the University of Luebeck, Germany. Before that he was chair of the computer engineering group, and Intel chair for VLSI design both at TU Braunschweig, Germany. He graduated with a PhD from University of Hannover, Germany in circuit design for signal processing systems. After his PhD he was working on processor design in IBM, and leading research teams in reconfigurable computing and mobile system design at IMEC, Belgium. His research interests include circuit and system design for safe, reliable and secure autonomous systems.

## Talk 7

**Christos Sotiriou (University of Thessaly, Greece)**

**Title:** ***An STA CAD Tool for SET Generation and Propagation***

**Abstract**: We present a Static Timing Analysis (STA) CAD tool for SET (Single Event Transient) Generation and Propagation, capable of replacing transistor-level, i.e. SPICE, simulations and completely compatible with state-of-the-art industrial EDA tools and flows. STA-based SET Generation upper bounds SPICE simulation results, and is capable of generating SET pulse profiles at any circuit node, based on current injection model(s). STA-based SET Propagation accurately analyses the pulse effect and propagation through circuit gates and wires. The pulse direction through gates and the widening or shortening effect through wires is accurately analysed, using fast STA algorithms. Logic Masking, Electrical Masking and regularly sized IPs and Verilog netlists are natively supported.

**Biography**: Christos P. Sotiriou received his BEng in Computer Science and Electronics, and PhD degree in Computer Science from the University of Edinburgh, Scotland, in 2001. He is an Associate Professor at the Department of Electrical and Computer Engineering of the University of Thessaly. His research interests include design methodologies for synchronous or asynchronous digital circuits and systems, Electronic Design Automation (EDA) Algorithms, Tools and Flows for digital circuit implementation, physical design, lower-power design, reliability and Power, Performance and Area (PPA) optimisation. Prof. Sotiriou has received three Qualcomm Faculty Awards, in 2019 and 2020 and 2021, and has collaborated with several large corporations on EDA tools and flows development, circuit implementation and physical design.

## Talk 8

**Thomas Lange (IROC Technologies, France)**

### Title: *Machine Learning Techniques to Estimate the Functional Failure Rate of Complex Circuits*

**Abstract:** Due to technology scaling, lower supply voltages and higher operating frequencies, modern circuits become more and more vulnerable to reliability and functional safety threats. Additionally, today's reliability standards and customers' expectations set tough targets for the quality of electronic devices and systems. Especially, transient faults, such as Single-Event Upsets and Single-Event Transients in the individual sequential and combinational cells, are the leading contributor to the overall failure rate for many applications and determining the Soft-Error Rate of the circuit is an important task. However, due to the increasing complexity of today's circuits, a detailed failure analysis requires a significant investment in terms of human efforts, processing resources and tool licenses. New methodologies need to be considered, in order to lower the cost of failure analysis efforts. Therefore, in this talk a methodology is presented which applies machine learning techniques to accelerate functional fault simulations and assists to obtain accurate fine-grained Functional Failure Rates for the full list of circuit instances.

**Biography:** Thomas Lange is a Research and Development Engineer at iRoC Technologies, France. He holds a M.Sc. degree in Computer Engineering from Berlin University of Technology and received his Ph.D. degree in Computer and Control Engineering from Politecnico di Torino, Italy. In his research he is investigating the effects of transient faults for high reliability applications in harsh environments. His main interest includes the development of new models and assessment techniques for transient faults, as well as new mitigation and error management techniques with the focus on hardware capabilities.