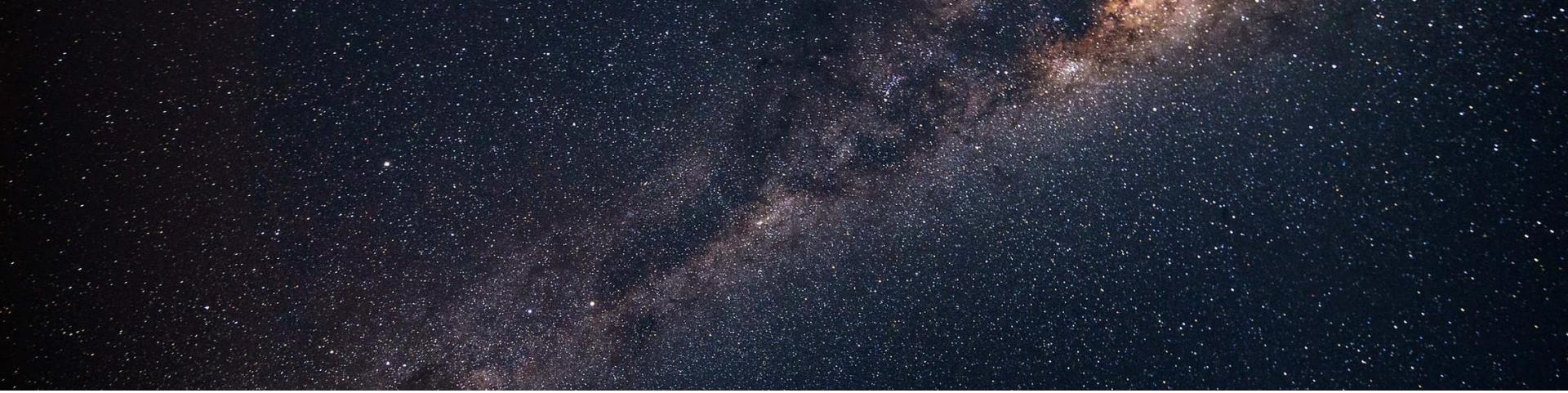


MORAL - Export-free Rad-hard Microcontroller for Space Applications

H2020 Programme Space Theme

Felipe A. Kuentzer

November 17th, 2021

ELICSIR Workshop

Agenda

- Background
- MORAL Project Introduction
- MORAL Microcontroller
  - PEAKTOP
  - MORAL Chip
- Radiation Hardening Techniques
  - Fault Tolerant Design Flow
- Project Developments Overview

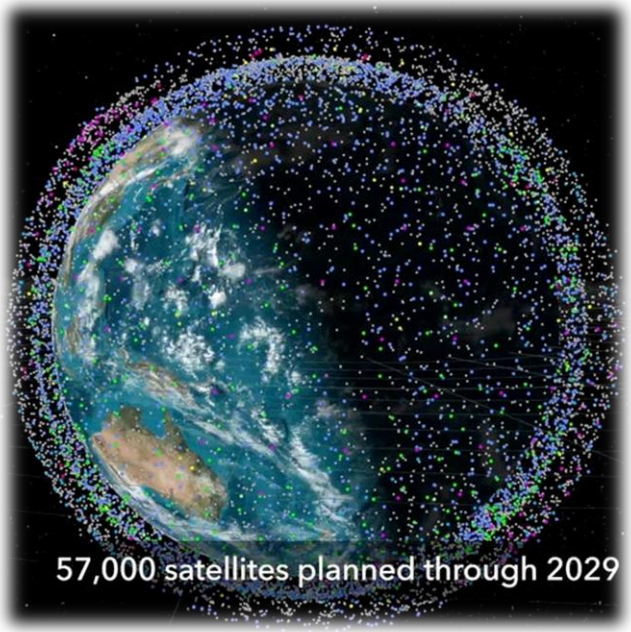
Background

Small satellites – 2030 and beyond

- Low-cost small satellites (from 10 kg to 500 kg)
  - Potential for scientific research and practical applications

- Small satellite modern applications
  - Satellite swarms or constellations replacing large satellites
  - Augmented satellite based navigation systems
  - Satellites in commercial aviation
  - Commercial satellite imagery based services
  - Robotic servicing technologies for space applications

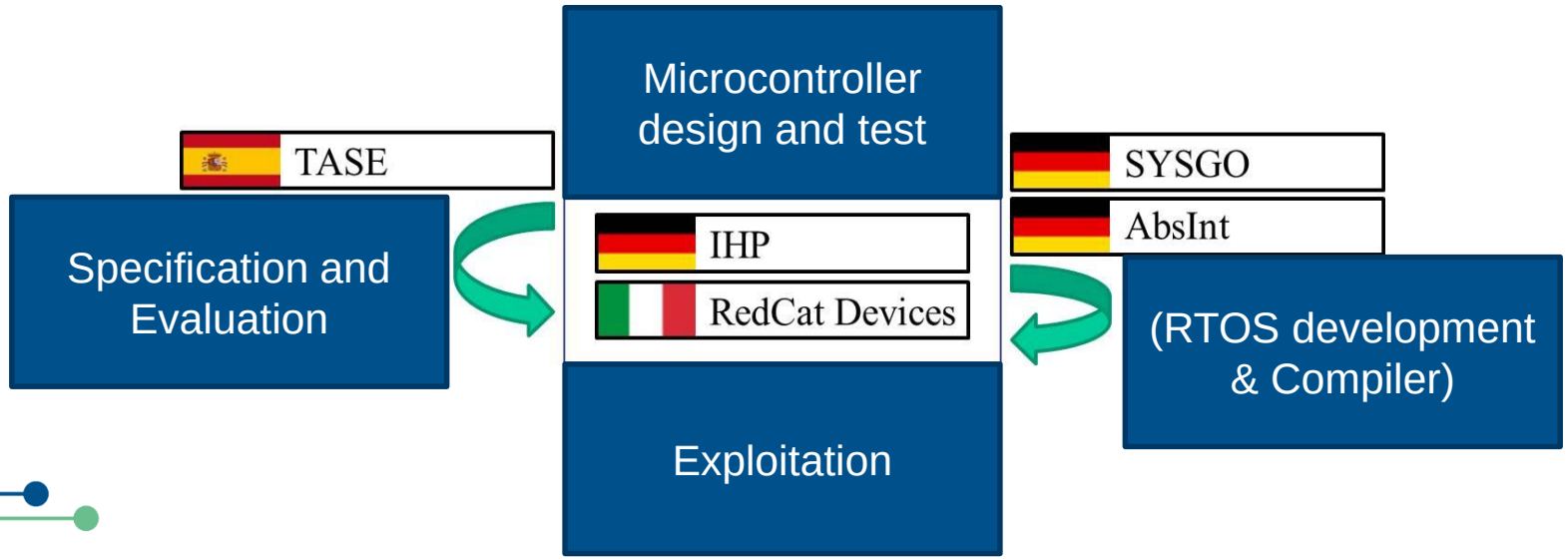
- Mainly powered by traditional electronics
  - Increased capabilities, but reduced reliability



Introduction

MORAL Project – H2020 Space Theme Programme

- Duration from 01. January 2020 to 30. April 2023 (40 months)
  - Funded by the EC - GA No. 870365
- Two main objectives
  - Develop a completely European, ITAR-free microcontroller for space applications
  - Exploitation plan for entering the market
- 5 partners



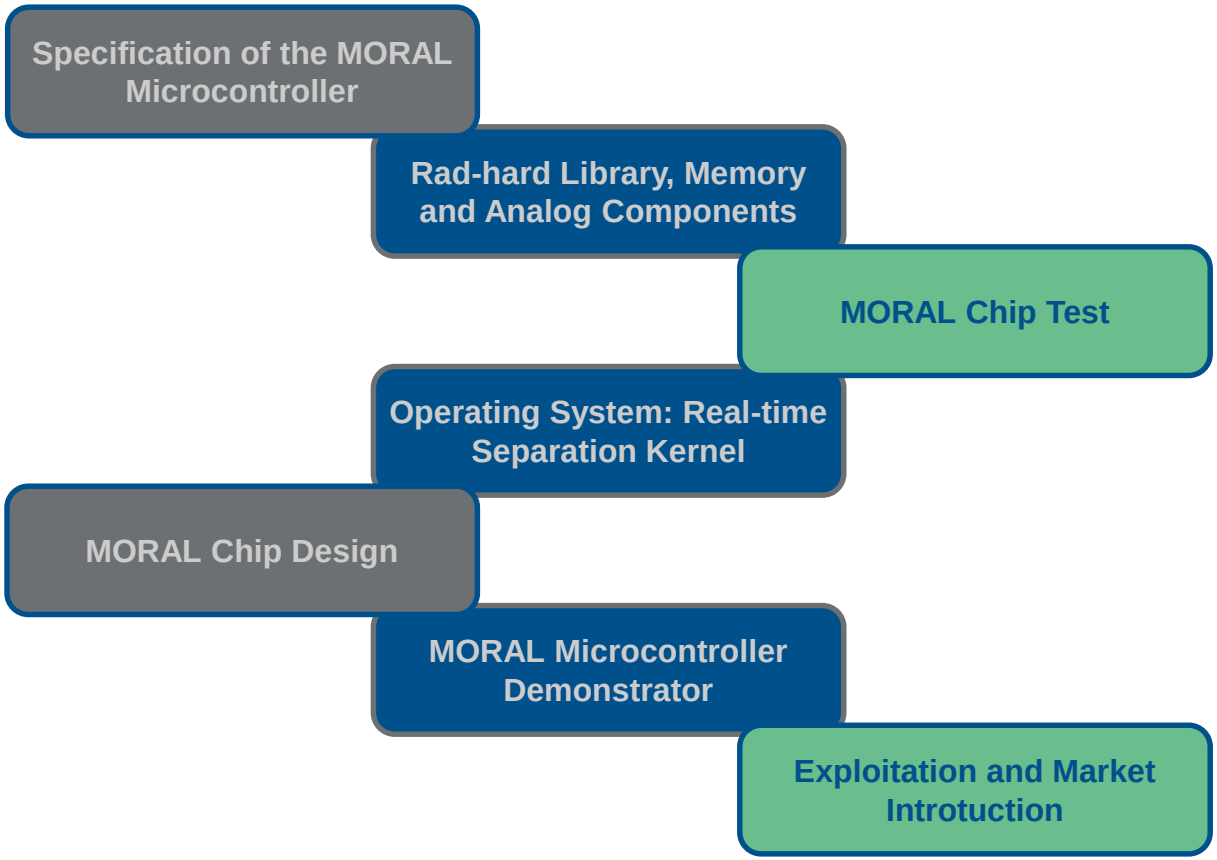
Introduction

MORAL in a nutshell

- Microcontroller based on the novel PEAKTOP architecture, including a novel Instruction Set Architecture (ISA)
- Formally-verified C compiler, RTOS, and toolchain
- Demonstrator board
- Irradiation tests
- Aggressive exploitation plan for bringing the product into market

Introduction

MORAL work overview



MORAL Microcontroller - PEAKTOP

Why a new processor core architecture?

- Processors currently used by the European Space Agency (ESA)
  - 32-bit LEON
  - 32-bit Arm Cortex
- LEON processors are based on the old SPARC architecture
  - Not scalable (e.g., to 64-bit)
  - Register windows that increase chip size or impose small code density
- ARM processor IP
  - Not freely available
  - Basic architectural reliability features
    - TMR (Triple-Modular Redundancy)
    - ECC (Error Correction Codes) for the memory blocks

MORAL Microcontroller - PEAKTOP

Why a new processor core architecture?

- RISC-V?
  - There was no reference implementation which could guarantees full verification

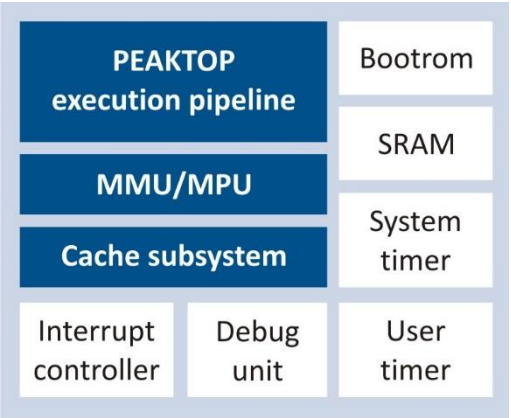
- PEAKTOP provides effectively the mixed criticality support
  - Multiple functions with different criticalities and assurance levels to co-exist in the microcontroller architecture
  - General Purpose Register (GPR) banks can be dynamically grouped
    - Dual-, Triple- or Quadruple-Modular Redundant (DMR/TMR/QMR) module to increase the fault tolerance

	Radiation hardness	Mixed criticality	Price	ITAR-free	Wide acceptance
ARM	+	-	-	-	+
LEON	+	-	+	+/-	+
RISC-V	-	-	+	+	+
PEAKTOP	+	+	+	+	-

Basic criteria for space microcontrollers

PEAKTOP Architecture

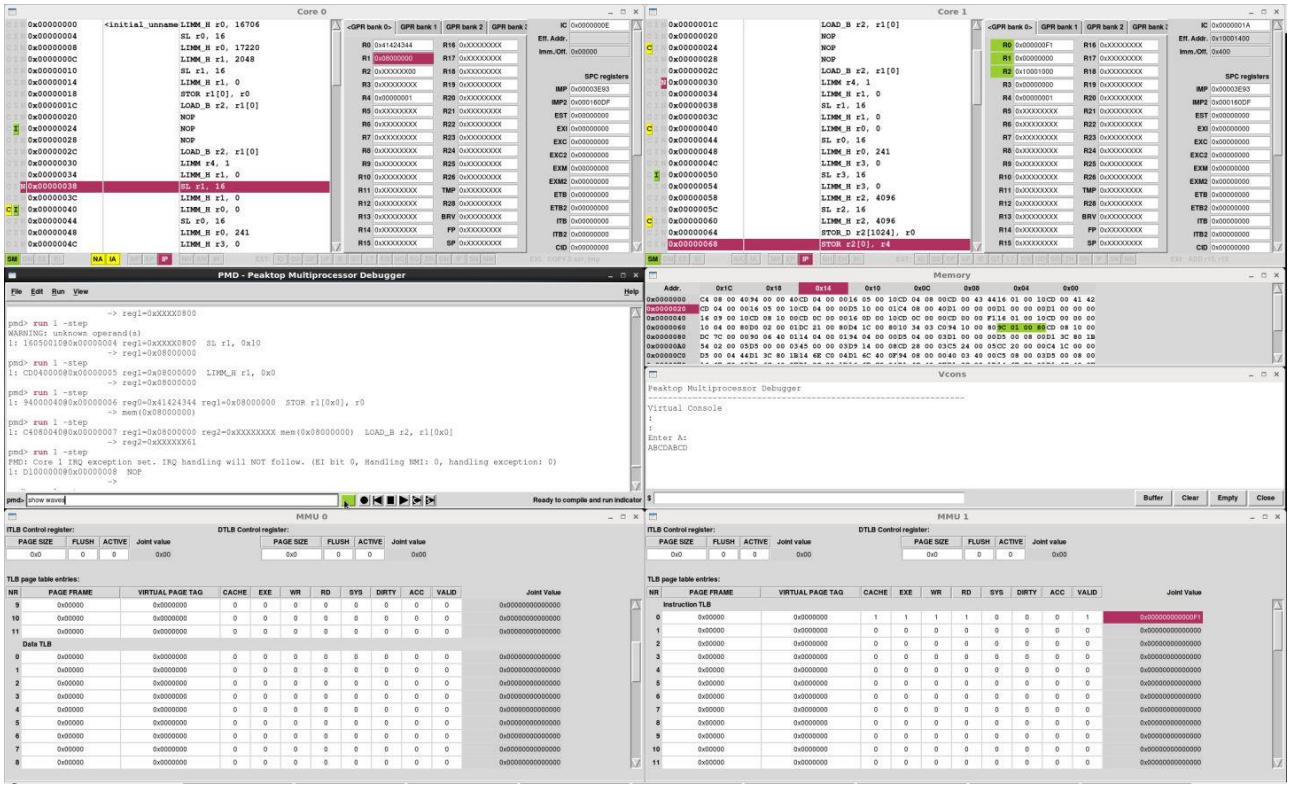
- IHP's own processor
  - Developed, implemented and tested in IHP 130nm technology



- Core architecture characteristics
  - RISC architecture
  - Up to 64 GPR
  - IEEE 754 compliant Floating Point Unit (FPU)
  - Optional Digital Signal Processing (DSP) extension
  - New ISA is fully **orthogonal**, **regular**, and **circular**
  - Multiprocessing support (cache coherence, synchronization support, atomic transfers)
  - Configurable addressing space: up to 64-bit; virtual address space is up to 128-bits
  - 32-bit wide instructions up to 3 operands
  - 2-level Memory Protection Unit (MPU), or (optionally) 2-level Memory Management Unit (MMU)
  - Optional L1 (separate data/instruction) cache, and L2 cache

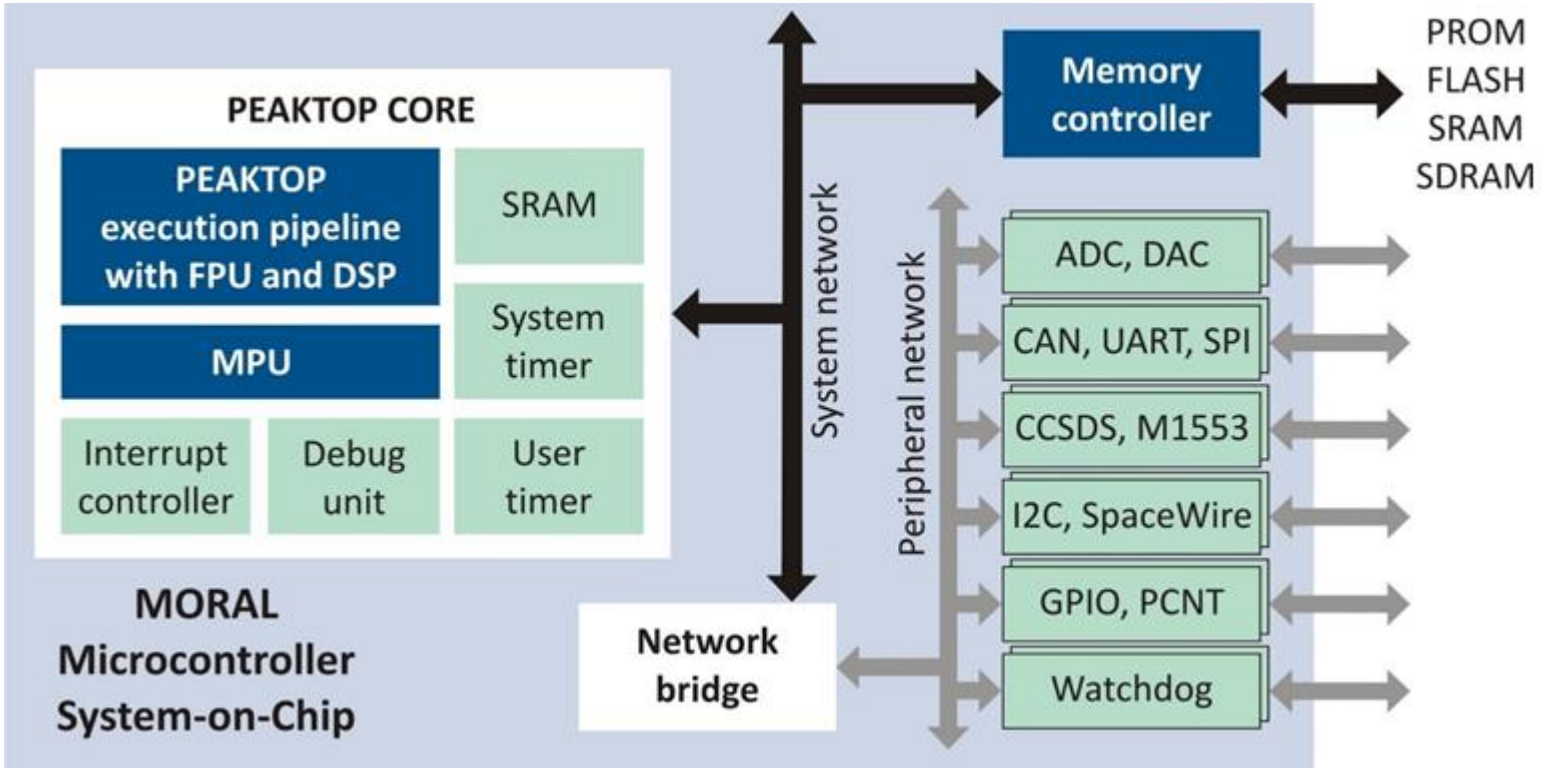
PEAKTOP Toolchain

- Open source toolchain
  - Multiprocessor Debugger
  - Instruction Set Simulator
  - Complete ISA and tools documentation



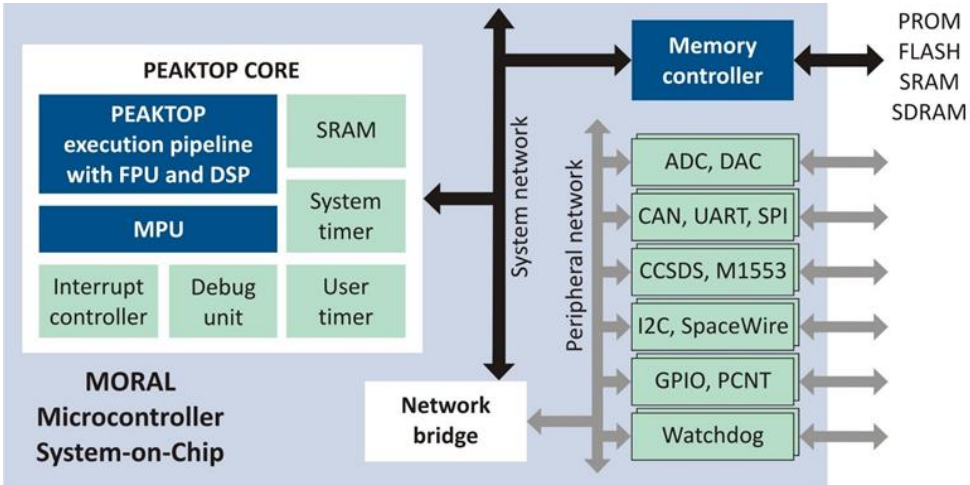
https://www.moral-project.eu/publication_open_source.html

MORAL Microcontroller



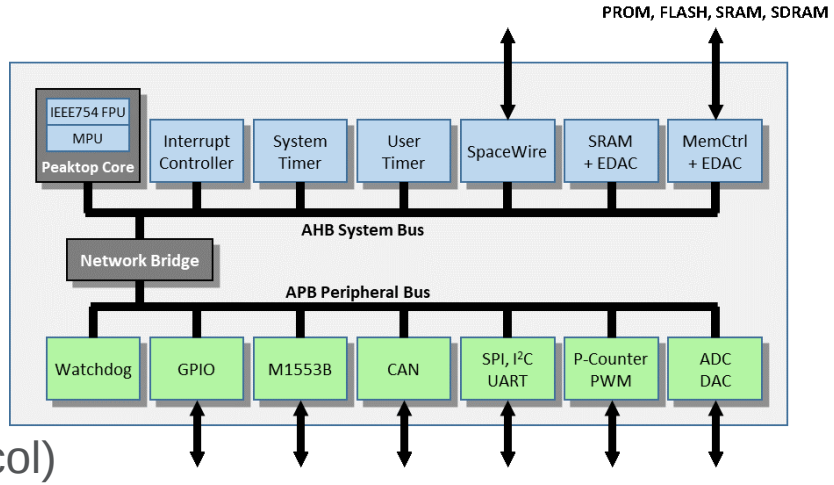
MORAL Microcontroller

- 256/512 Kbyte SRAM
  - Error Detection and Correction (EDAC) protection unit
- 1 x Interrupt Controller
  - 32 interrupt lines
- 6 x Timers
  - 2x system + 4x user timers
- 64 x GPIO ports
  - Shared with internal peripherals I/Os



MORAL Microcontroller

- Peripherals
  - 1 x 8-channel 12-bit ADC module
  - 2 x 12-bit DAC modules
  - 2 x CAN 2.0 modules
  - 4 x UART interfaces
  - 2 x SPI interfaces
  - 2 x SpaceWire interfaces (incl. RMAP protocol)
  - 1 x MIL-STD 1553C bus interface (incl. redundant bus)
  - 2 x I2C interfaces
  - 1 x 8-channel PWM generator
  - 4 x Pulse counters
  - 1 x Watchdog timer



- Rad-Hard Specification
  - Total ionizing dose (TID) **100 krad** (Si)
  - Single event upset (SEU) for the processor's digital core **>30 MeVcm²/mg**
  - Single event latch-up (SEL) >60 **MeVcm²/mg**

Radiation Hardening Techniques

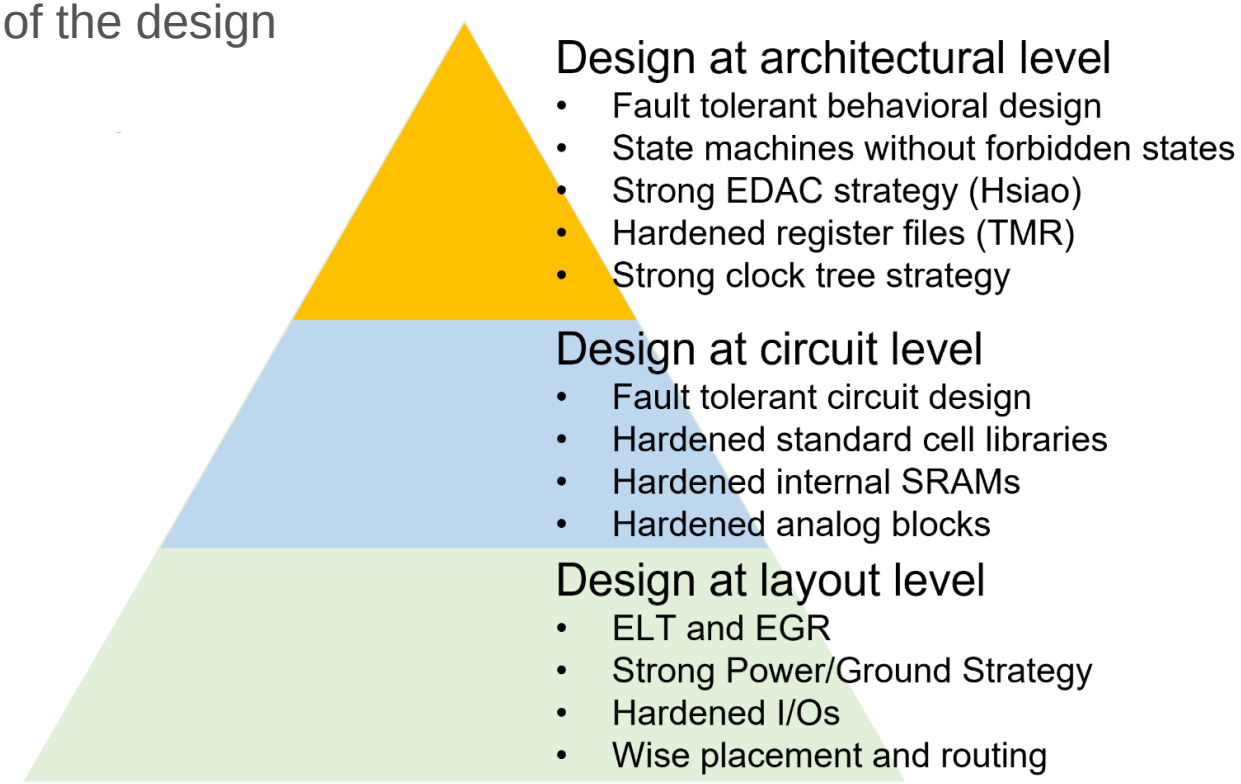
- Hardening silicon devices towards radiation
  - Radiation Hardening by Process (RHBP)
  - Radiation Hardening by Design (RHBD)
- RHBP falls under large silicon foundries efforts
  - Cost of developing new RHBP technology nodes became prohibitively expensive
  - RHBD is considerably less expensive
- In both RHBP and RHBD approaches radiation cannot be avoided
  - Solution is to mitigate the effects
- MORAL rad-hard methodology focus only on RHBD
  - IHP 130nm technology process

Radiation Hardening Techniques

Fault Tolerant Digital Flow

- Establishing a RHBD Flow for a digital ASIC means working at all levels
  - From the layout of the single logic port up to the RTL code

- Balance between RHBD techniques and area/power consumption is the most critical part of the design

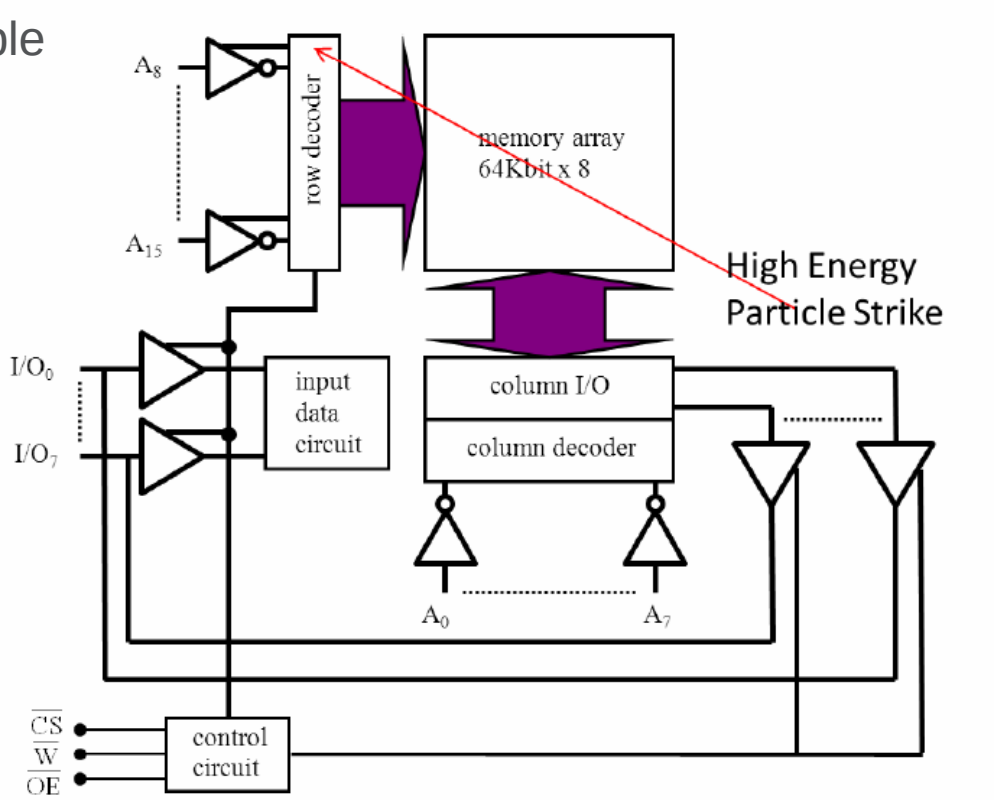


Radiation Hardening Techniques

RHBD-AL: Radiation Hardening by Design at Architecture Level

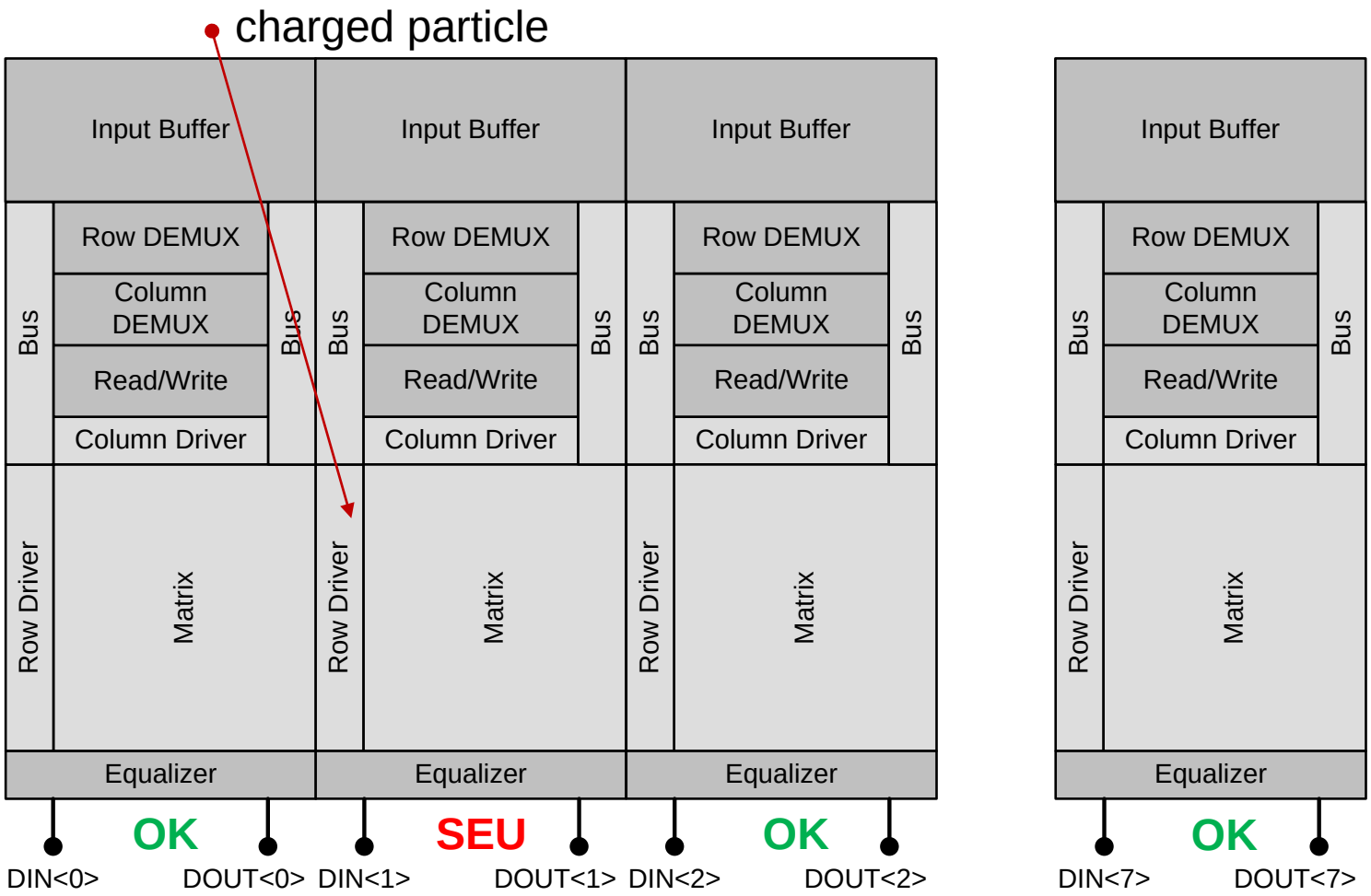
- Chip is floor-planned and considered in its entireness
  - Macro-blocks are built (and eventually replicated)

- Memory example



Radiation Hardening Techniques

- RHBD-AL methodologies suggest replicating row and column decoders

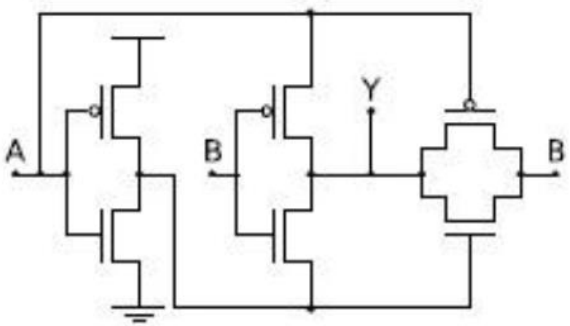


Radiation Hardening Techniques

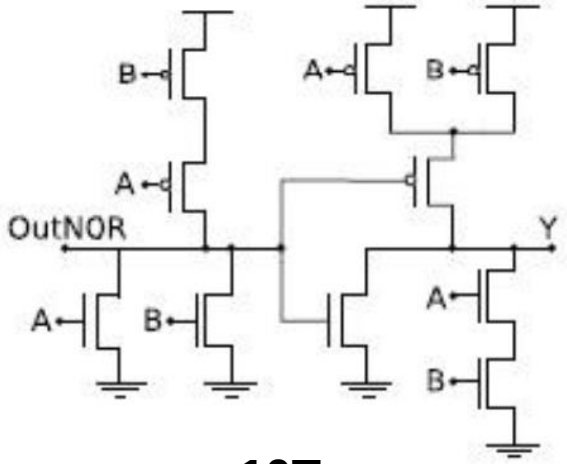
RHBD-CL: Radiation Hardening by Design at Circuit Level

- Single block or circuit is considered
  - Design of logic gates in digital libraries
- Usually logic gates are devoted to a minimum area occupation
  - It is assumed they can be extensively used in an entire chip
  - From rad hard point of view they are not optimized

- XOR gate example
  - Six transistors (6T) vs ten transistors (10T)



6T



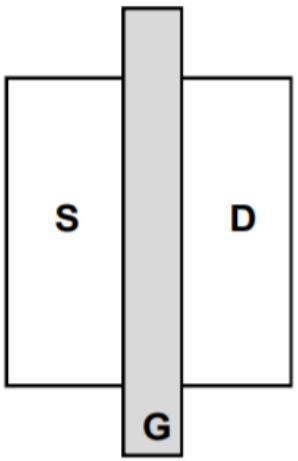
10T

Radiation Hardening Techniques

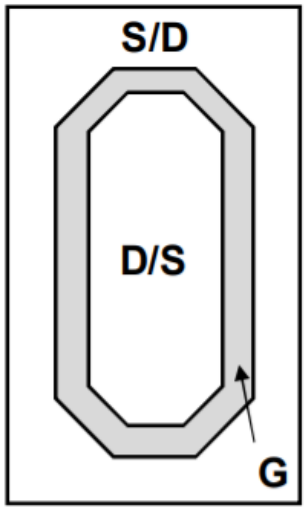
RHBD-LL: Radiation Hardening by Design at Layout Level

- Single transistor shape is considered
  - Shape to avoid degradation on channel borders

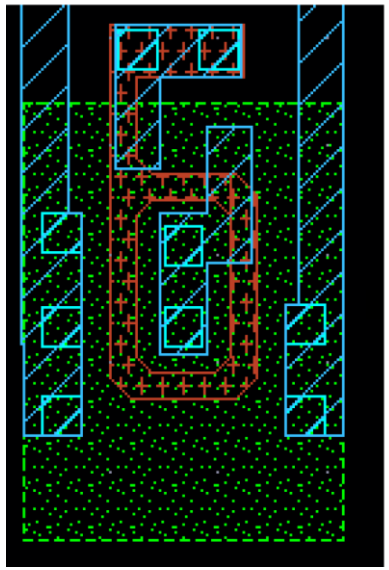
- Edgeless Transistor (ELT) represent a typical RHBD-LL solution
  - Annular Transistor or Ring Transistor



Standard two-edge



Annular

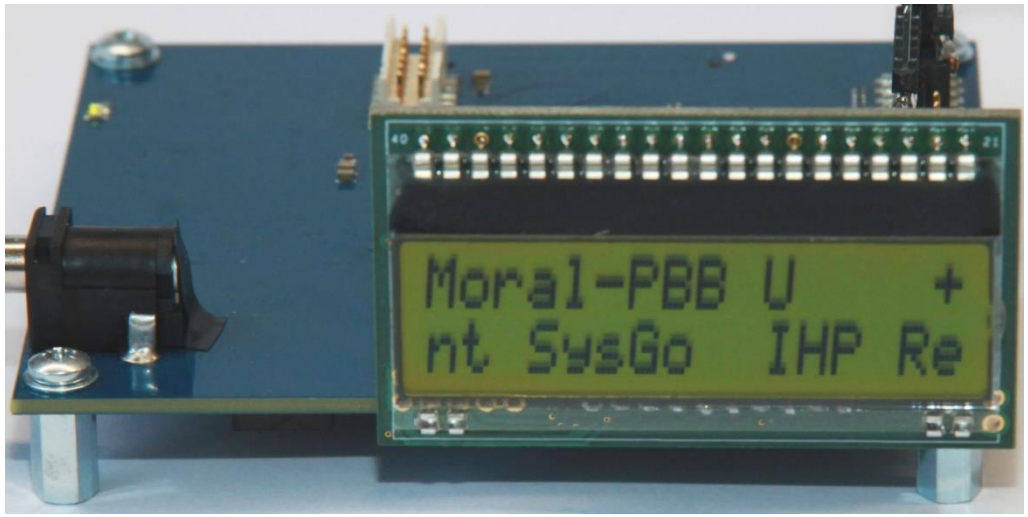


ELT nmos IHP130nm

Project Developments Overview

What was accomplished in the first 20 months of the project?

- Microcontroller design and verification
  - Digital Design and Verification of Chip Components
  - Verification of the integrated Digital Design by VHDL / Verilog Simulation
  - Hardware Verification in an FPGA Implementation

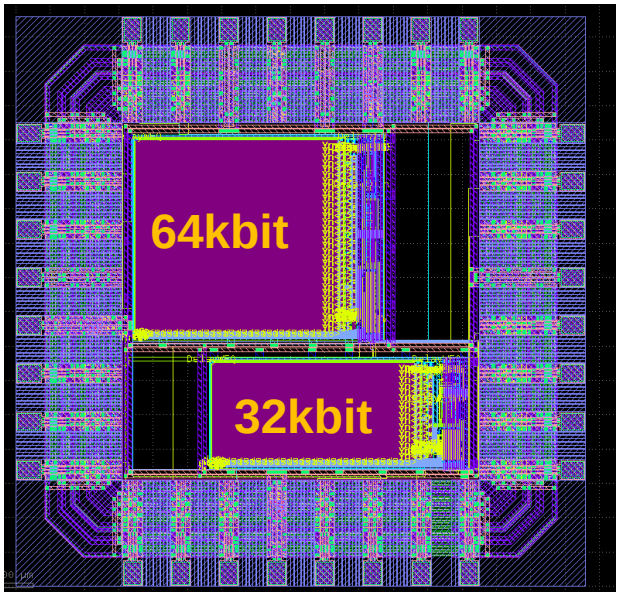


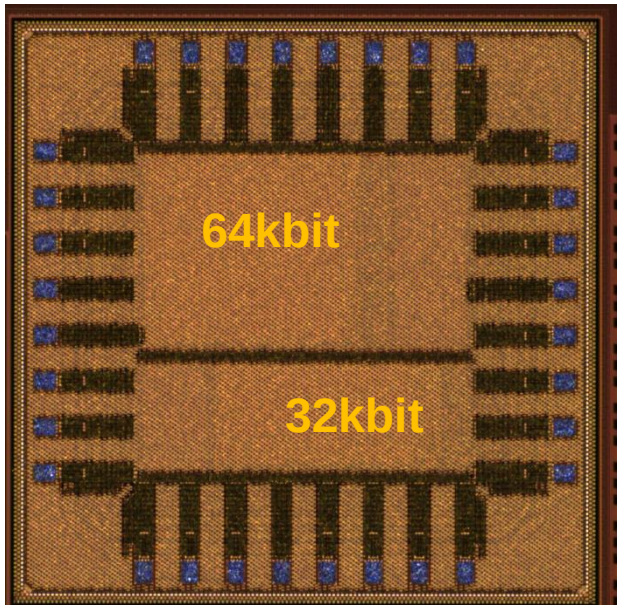
Experimental FPGA board

Project Developments Overview

- Four test chips produced in the first 20 months of the project

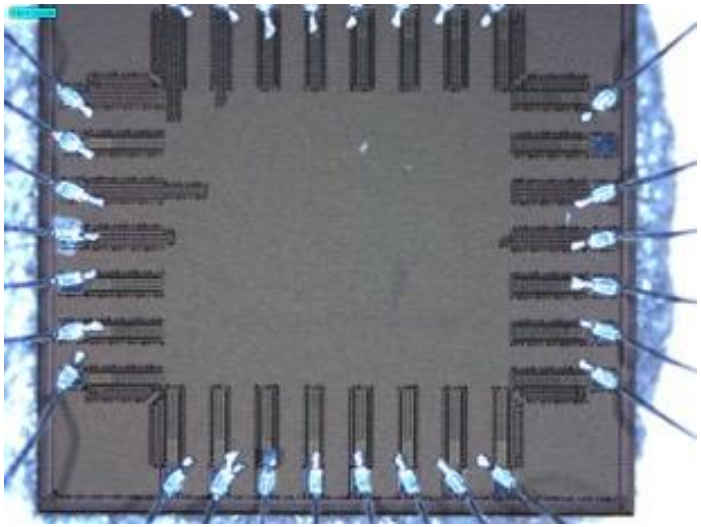
- **Test Chip 1 (MORAL_TC01)** - Single bit SRAM blocks of 32kbit and 64kbit
  - SRAM modules were tested on wafer at IHP





Project Developments Overview

- **Test Chip 2 (MORAL_TC02)** - 10-bit DAC for evaluation
  - Evaluate the layout approach
  - Designed, integrated into a test chip, and electrically characterized in lab with satisfactory results



Project Developments Overview

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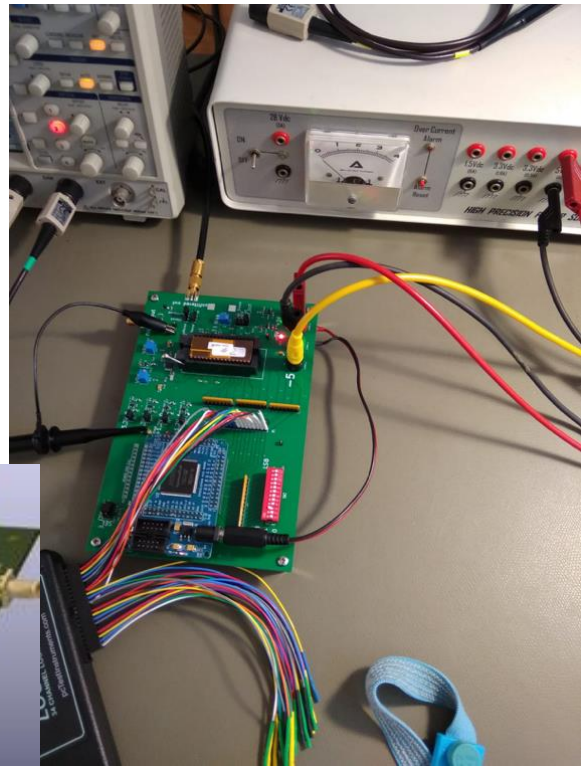
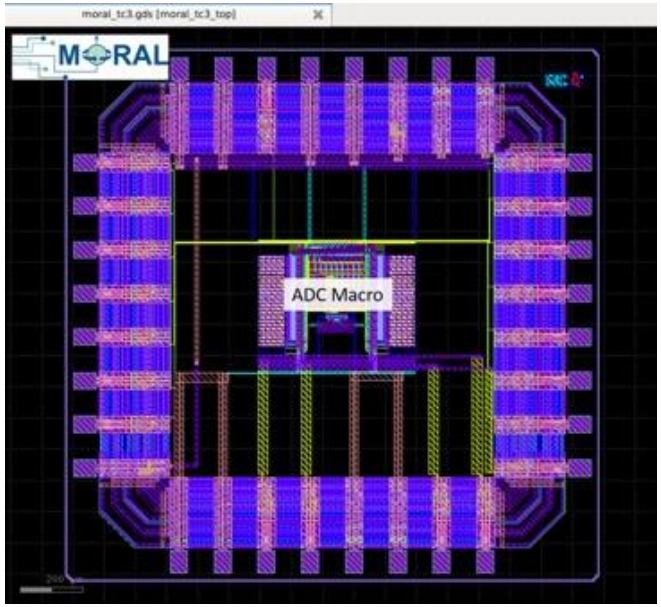
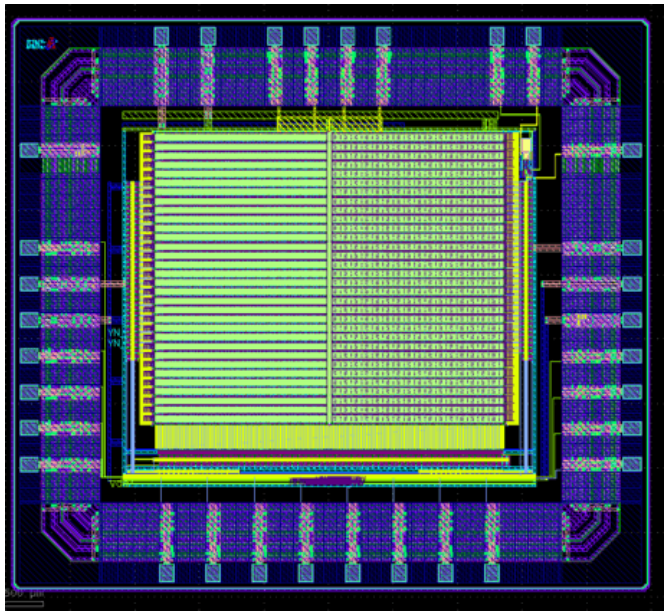


Project Developments Overview

- **Test Chip 3 (MORAL_TC03)** - 12-bit ADC
  - Currently being electrically characterized in lab

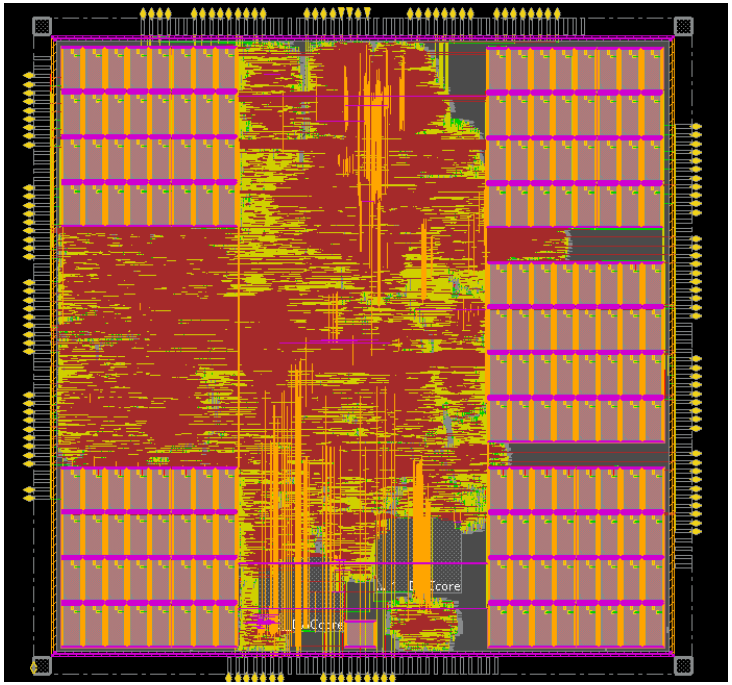


- **Test Chip 4 (MORAL_TC04)** - 12-bit DAC
  - Taped-in in July



Project Developments Overview

- The C compiler (CompCert) porting for the MORAL architecture was completed
  - CompCert generated code currently being tested in FPGA
- Preliminary RTSK is running in the FPGA platform
- Work on final chip layout is undergoing

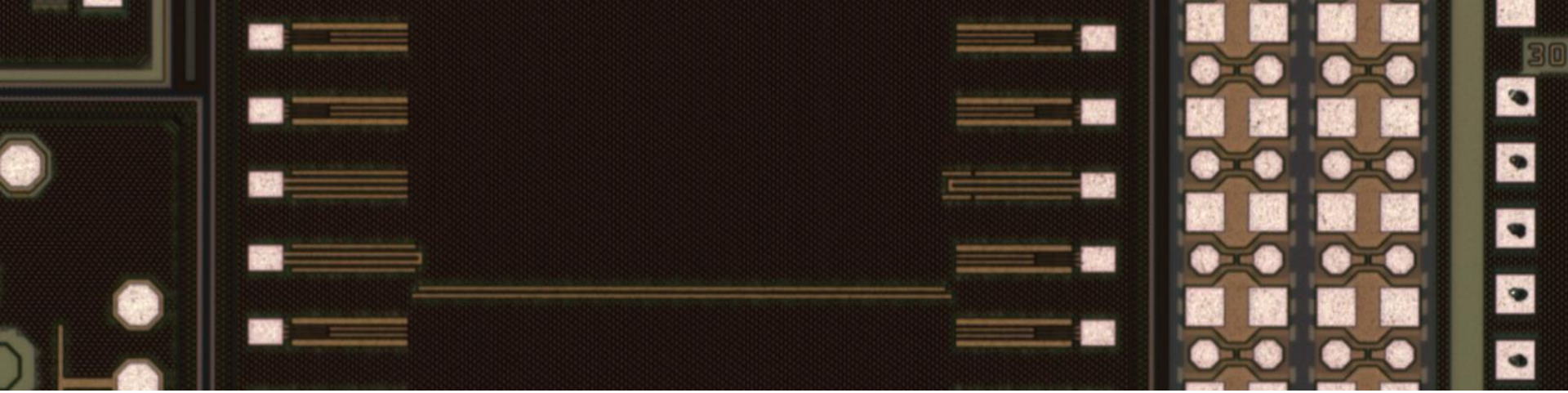


Preliminary MORAL Chip Layout

MORAL Website

- Access for more information and news about MORAL
- Links for the project Social Media
- PEAKTOP toolchain download

www.moral-project.eu



Thank you for your attention!

MORAL

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