Ionizing Radiation and Electromagnetic Interference on Integrated Circuits:
from the need of combined test to current solutions

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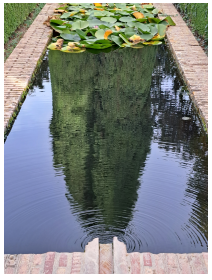
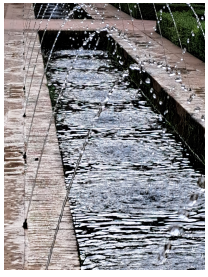




Session 3
Meeting room: Carmen de la Victoria
10:25 - 10:55

Motivation, Main Concerns

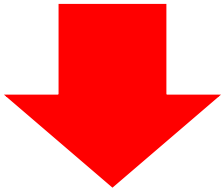
Aerospace Industry

Designers face a continuous pressure to use **new technologies** and **architectures** to improve **performance**, reduce **area**, **power** and **cost** of electronic systems devoted to **critical applications** (aerospace, defense, automotive, …).

Motivation, Main Concerns

Aerospace Industry

These new architectures require more and more the use of **fast** and **reliable ICs** (such as **NoC MPSoC**, **FPGAs** and **memories**) in **mission-critical applications**



which makes **EMI & ionizing radiation control** even **more challenging**

Current State-of-the-Art

From the best of our knowledge ...

Only a few works addressing the problem: trying to understand and quantify the combined effects of ionizing (**total-ionizing dose: TID**) and non-ionizing (**EMI**) radiations on ICs
(*IEEE TRANS. ON PLASMA SCIENCE, VOL. 40, NO. 6, JUNE 2012*)

Lack of research focusing on the combined effects of ionizing (**soft errors in memory elements**) and non-ionizing (**EMI**) radiations on ICs

Absence of a **standard** to rule combined tests
(*currently, only a Draft Recommendation from ITU:*
"Overview of particle radiation effects on telecommunications systems", Geneva, Oct. 2016)

Our studies have shown a **considerable reliability degradation** for systems operating in harsh environments (such as space, where satellite electronics is exposed to the combined effects of ioninzing rad: TID/soft errors and EMI)
(*Analysis of SRAM-Based FPGA SEU Sensitivity to Combined EMI and TID-Imprinted Effects, IEEE TRANS. ON NUCLEAR SCIENCE, VOL. 63, JUNE 2016*)

Where is the problem?

It is a common practice that …

engineers qualify electronic systems to EMI, TID or SEU, or eventually to all of them, but often NOT taking into account the combined effects one phenomenon may take over the other.

e.g., assume a given part of an embedded system for satellite application is certified by a set of EMI tests according to specific stds

Where is the problem?

After a given period of t… ing i… …

Who can ensure that this part will still per… operly according to the same set of EMI stds, after a given l… TID radiation has been cumulated over time on the system, if … was certified independently for EMI and radiation?

Moreover, who can ensure that the system will be approved for the same set of EMI stds, if operating in a harsh environment with dense flux of high-energy particles (SEEs)?

Our Contribution

Aerospace Industry

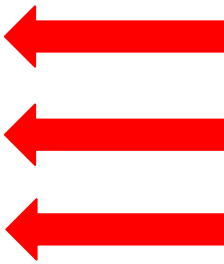
Develped technology to qualify ICs for the Brazilian Space Agency having in mind combined effects of TID, SEU and EMI

Study: addressing FPGAs of different types and technology nodes

Our Contribution

The analyzed FPGAs ...

Xilinx:	**Spartan3XC3S500E**	
	Virtex4XC4VFX12-10SF363	**(SRAM)**
Microsemi:	**ProAsic3E1500**	**(Flash)**
IECAS:	**ERC3000-G**	**(SRAM)**



Our Contribution

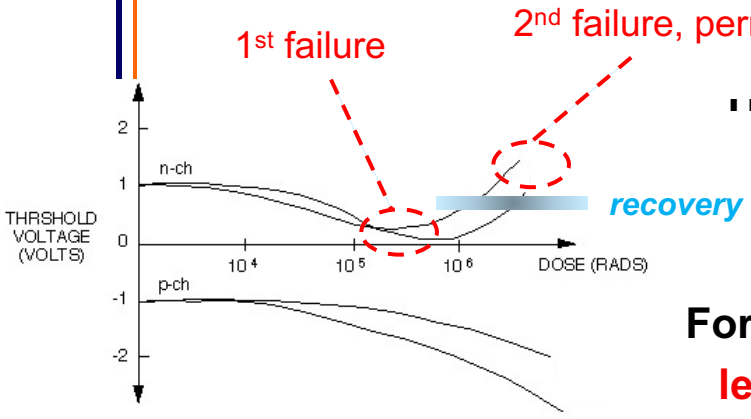
We ...

analyzed the impact of combined tests for EMI + radiation (TID/SEU) on the reliability of electronic components

proposed a new methodology that takes this combination into account in order to qualify state-of-the-art COTS ICs

Understanding the Effects of Radiation (TID) on Electronics

For critical applications (military, aerospace or biomedical) reliability assurance to total ionizing dose (TID) radiation is always at a premium being a key-issue for the success of such products in the market.



TID effects on CMOS ICs are caused primarily by positive charge trapped in insulating layers

⬇

For CMOS ICs, the main TID effect is the increase of leakage currents and change in V_{th} of the devices

⬇

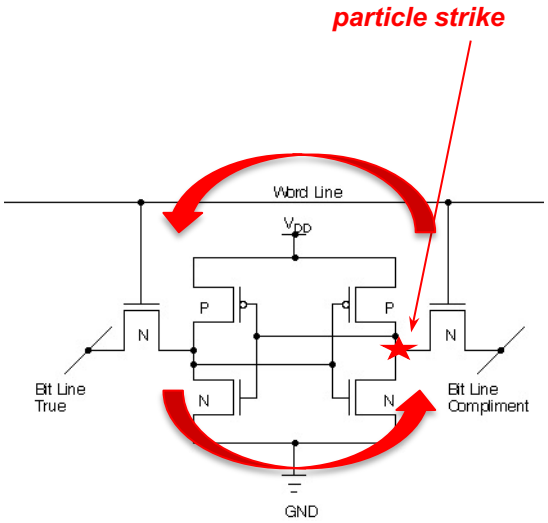
For high doses, a permanent functional failure of the circuit is observed.

Understanding the Effects of Radiation (SEE) on Electronics

Radiation (SEU) effects on CMOS ICs are mainly caused by high-energy particles striking reverse biased drain depletion region of off-transistors

For CMOS ICs, the main SEU effect is the loss of information stored in memory elements (FFs, RAMs)

Transient functional failure of the circuit is observed



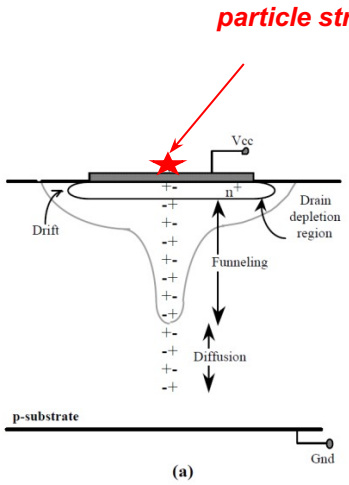


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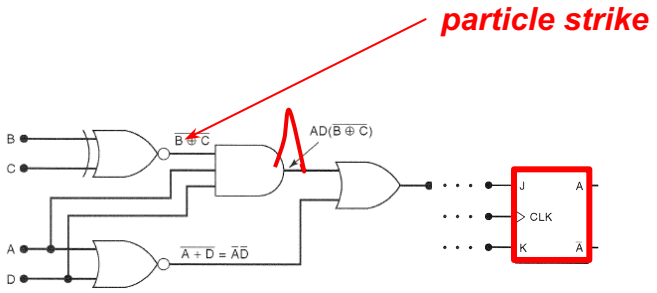
Fig. 1. Illustration of the charge collection mechanism that cause single-event upset: **(a)** particle strike and charge generation; **(b)** current pulse shape generated in the n+p junction during the collection of the charge.

Understanding the Effects of Radiation (SEE) on Electronics

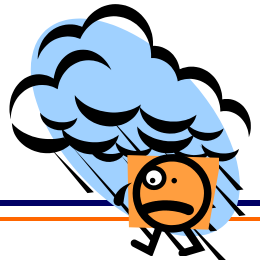
Radiation (SET) effects on CMOS ICs are mainly caused by high-energy particles striking logic along with critical paths

For CMOS ICs, the main SET effect is the loss of information stored in memory elements (FFs, RAMs)

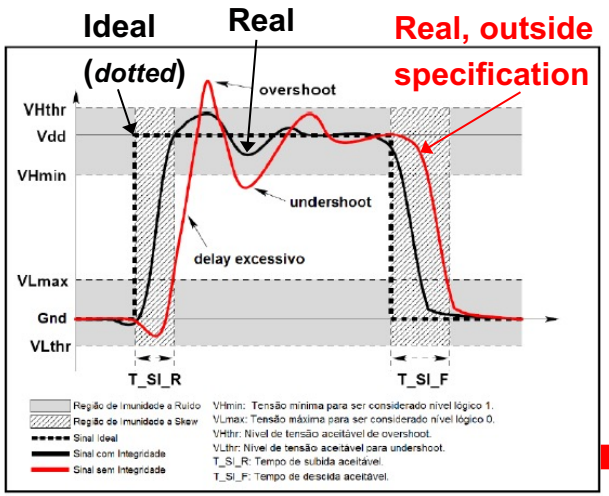
Transient functional failure of the circuit is observed



Understanding the Effects of EMI on Electronics



The increasing hostility of the electromagnetic environment caused by the widespread adoption of electronics, (mainly wireless technologies), represents a huge challenge for the reliability of RT embedded systems.



Electromagnetic Interference (EMI)

⬇

Power Supply Disturbances (PSD)

⬇

Transient Faults

Signals outside noise margins can be erroneously interpreted and stored by memory elements at the end of critical paths

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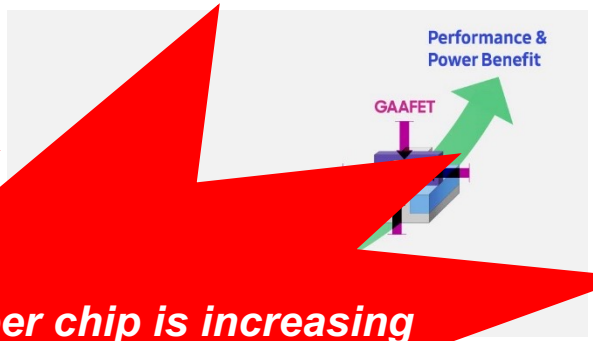
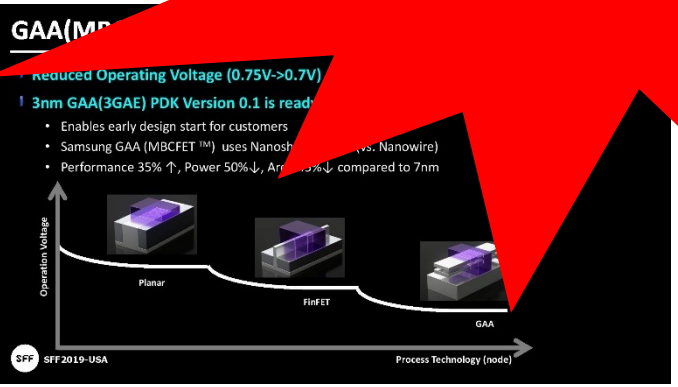
Technology trends impact on ICs

Technology scaling down …

Gate All Around, Multi-Bridg



Soft Error Rate (SER) per chip is increasing



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Performance (frequency)

1) Ionizing Radiation:

~~TID:~~ or ~~ ~~ ?

SEEs: (SEU/SET)

2) Aging:

3) EMC:

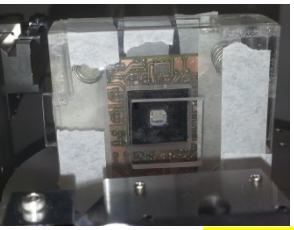
~~E~~E:

EMI:

Hot Topics for the incoming years !!!

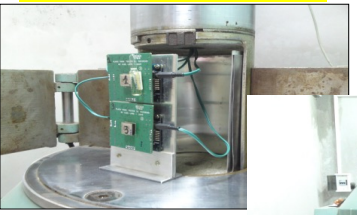
Combined Test Planning Methodology

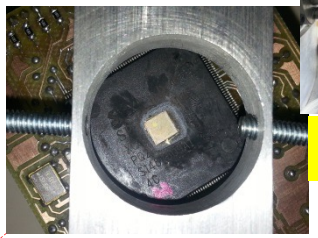
Combined tests of TID + SEU + EMI



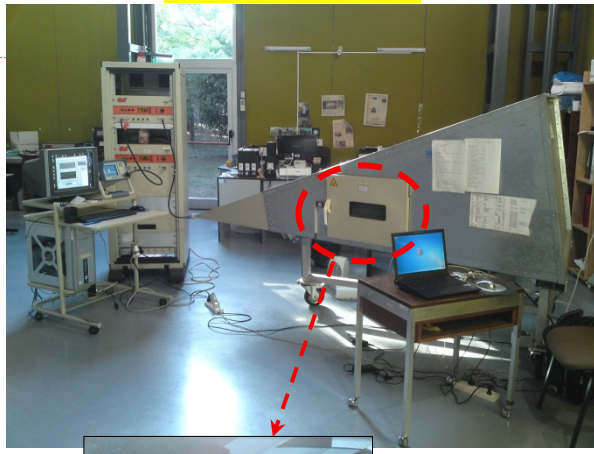
X-Ray

Co^{60} (Gamma Cell)

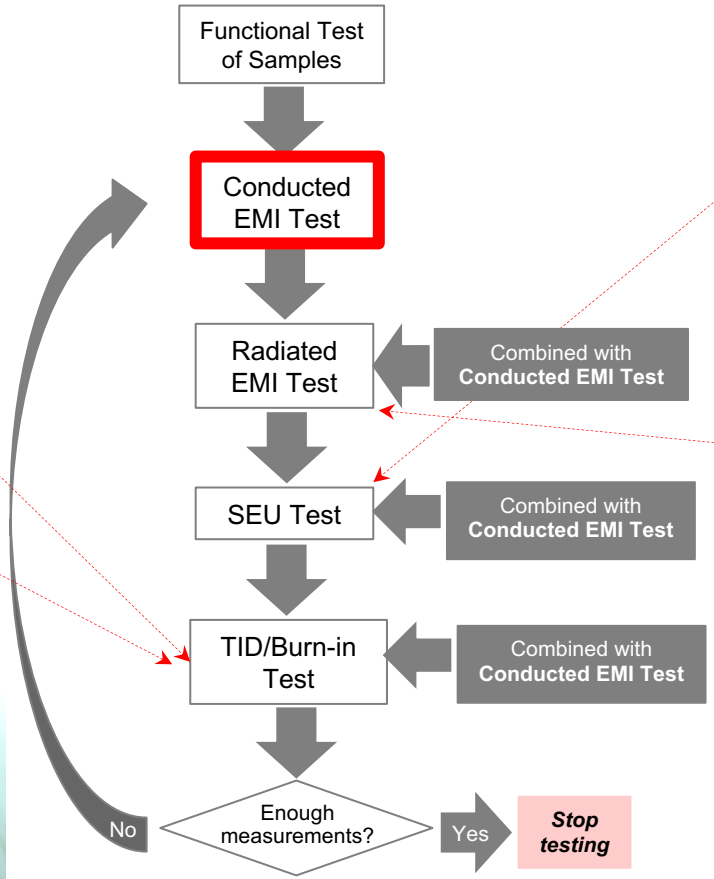




SEU



Radiated EMI Test (G-TEM Cell Test Method)



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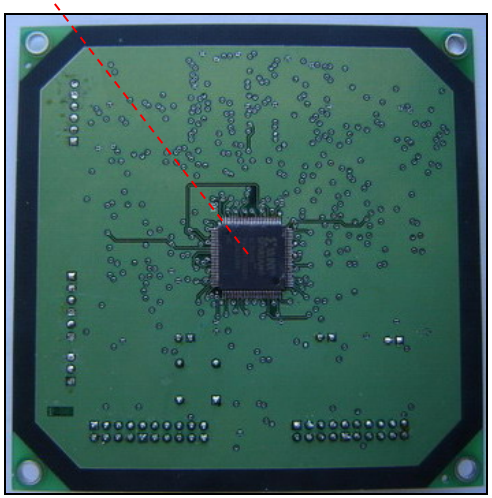
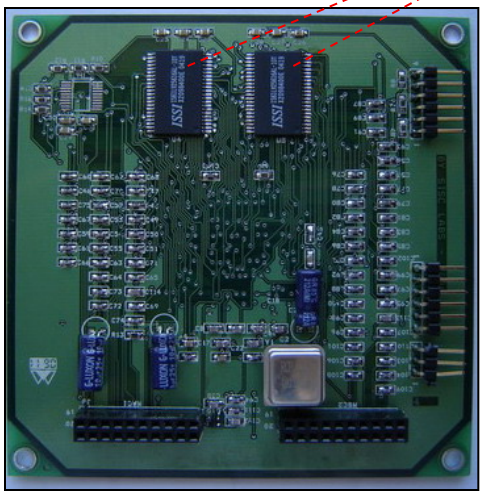
Test Boards (HW parts)

FPGA (System-on-Chip)

16MB SRAM (RTOS + user application)

System under Test





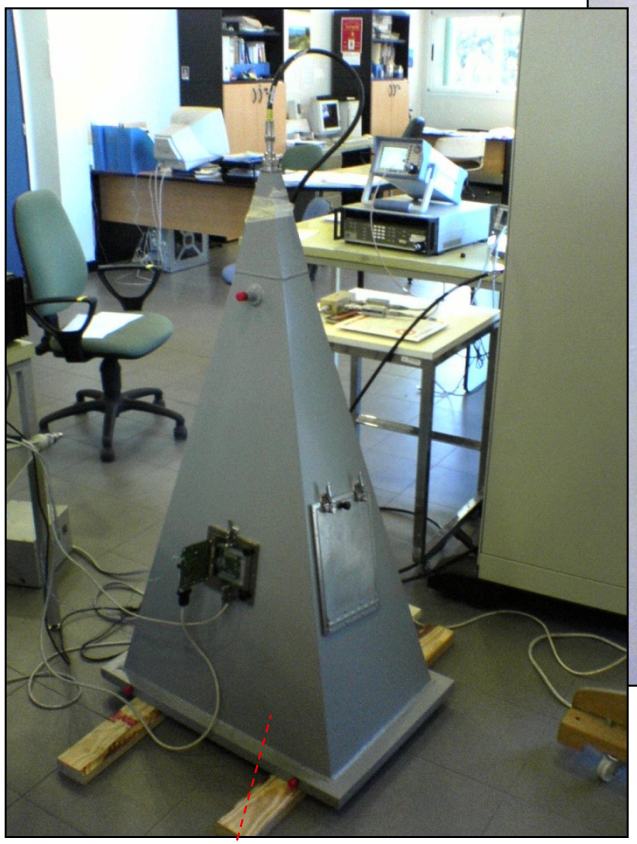
Top view

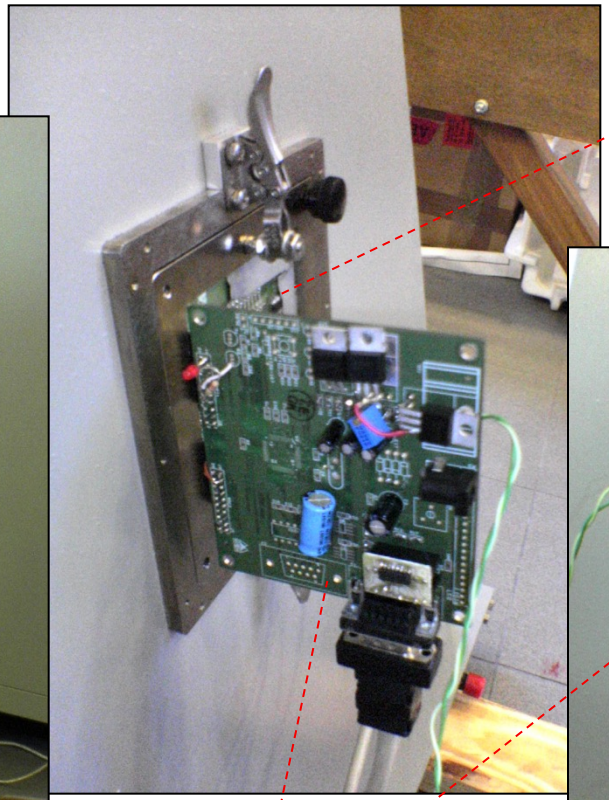
Bottom view

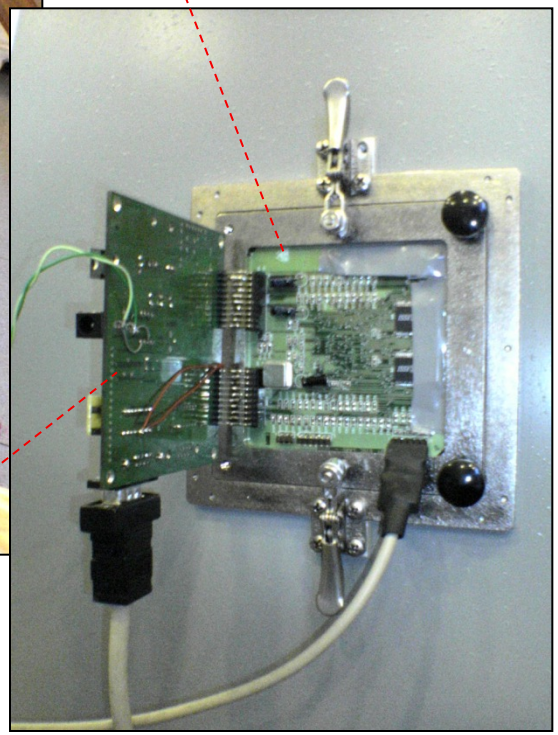
IEC 62.132-2 std compliant board.

Four-layers: Gnd (top) - signal - signal - Vdd (botton).

Test Boards (HW parts)







System under Test

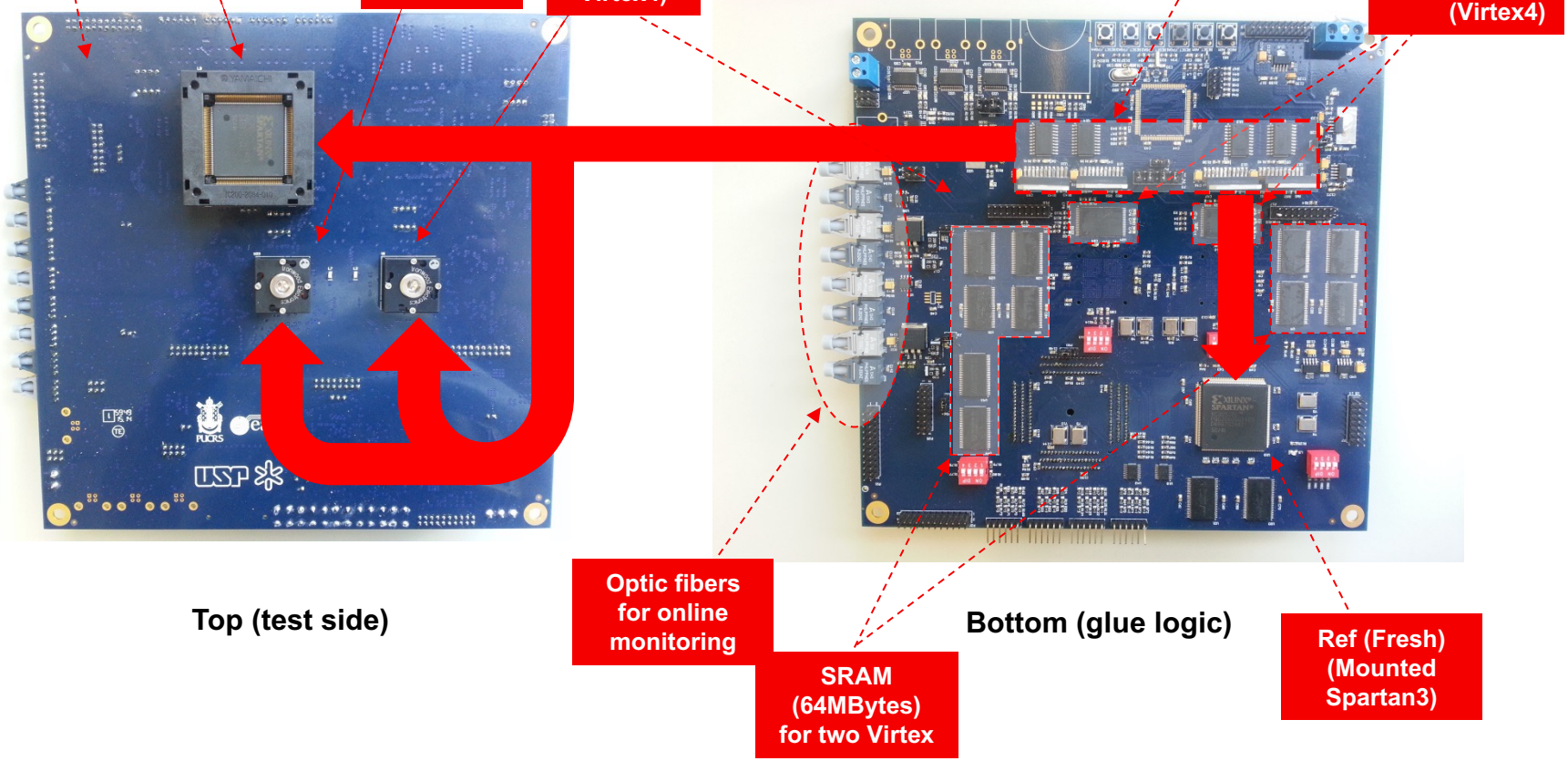
TEM Cell

Interface Board

Gnd Plane

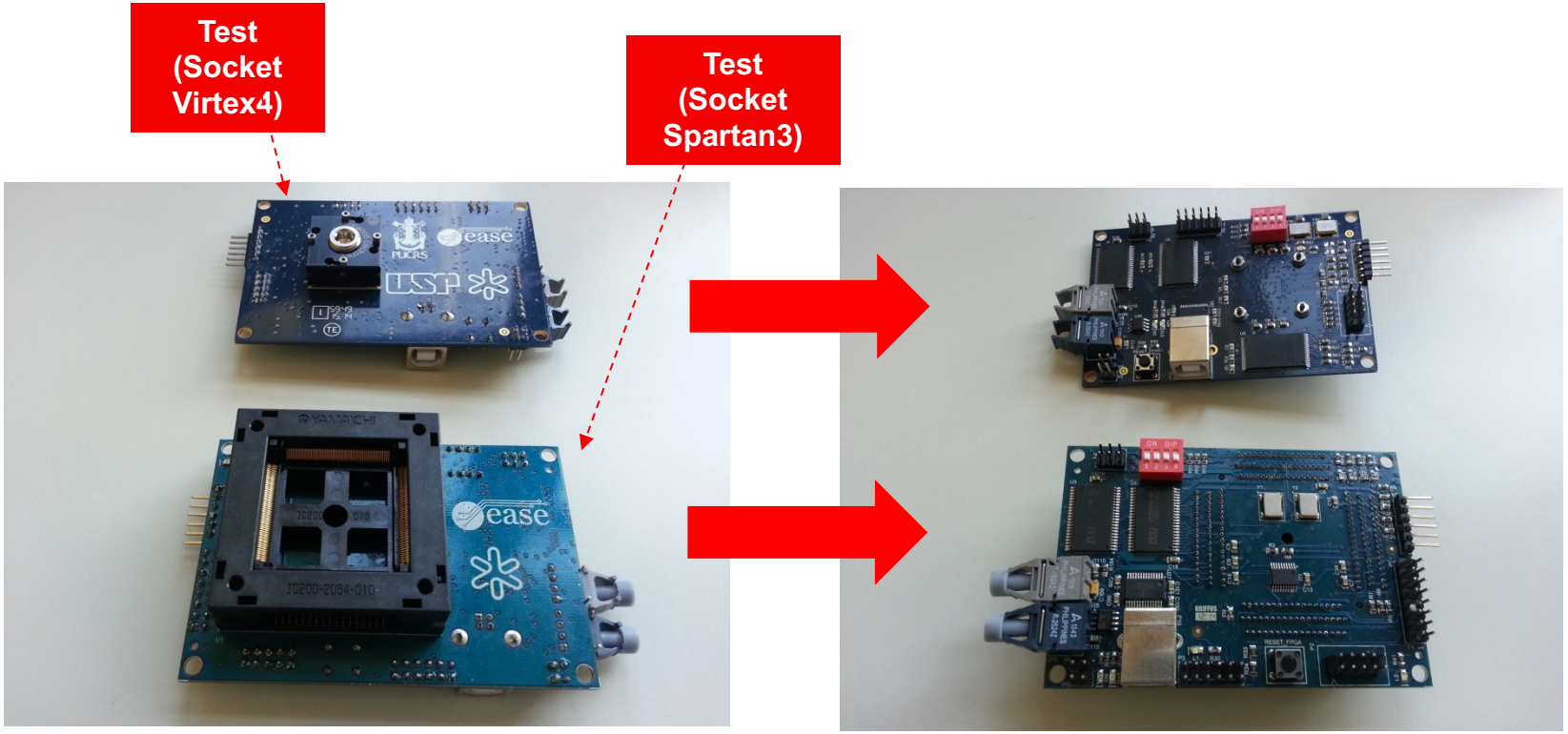
4th Generation

Test Boards (HW parts)



12-layer Motherboard for Combined EMI x Radiation tests

Test Boards (HW parts)



Top (test side)

Bottom (glue logic)

6-layer Daughterboards for Combined EMI x Radiation tests

Experiment (1)

Combined Tests:

Conducted EMI + TID + SEU

Photo with Microsemi ProAsic3E A3PE1500

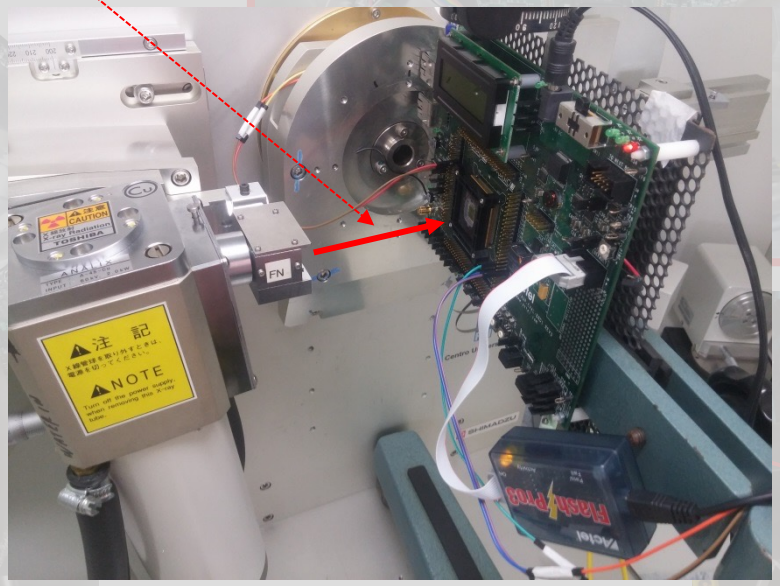
Experiment (1)

Goal (Xilinx Spartan3 XC3S500E):

SEU sensitivity w.r.t. Conducted Noise on V_{DD} Bus, TID and Imprint Effect

TID
(X-Ray Diffractometer)

Beam direction



SEU
(Heavy Ions Accelerator)

Local Test Host Computer

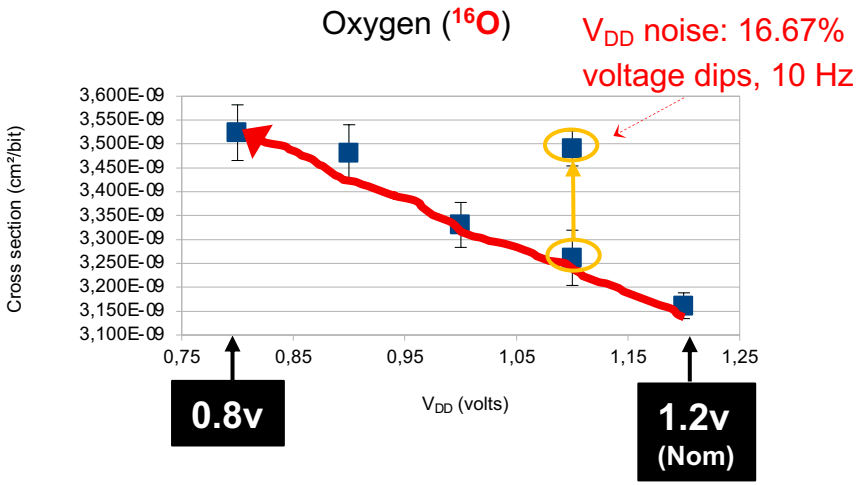
IEC 61.0004-29-Compliant
EMI Noise Generator

Experiment (1)

(Configuration Bitstream) Cross Section as function of Power Supply (V_{DD}) Disturbance (**Fresh FPGA**)

SEU sensitivity (σ): +10% w.r.t. nominal V_{DD}

SEU sensitivity (σ): +11% w.r.t. nominal V_{DD}



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Experiment (1)

Imprint Effect:

When a memory element remains for a long period storing **the same logical value** (“0” or “1”) while being irradiated for high dose rates, **it tends to maintain this value during the rest of its lifetime (**similar to the **“stuck-at fault” Model** widely used by industry**)**.

RAM → ROM

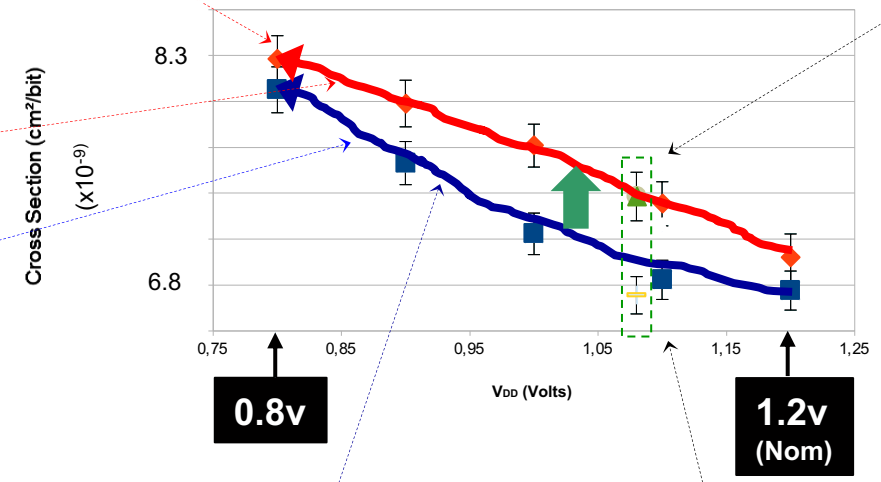
We have deposited **750 krad** and **950 krad** on two **Xilinx/Spartan3** FPGAs storing the pattern “all 0’s” in the BRAMs (“hard” pattern) (same fabrication lot)

Experiment (1)

(BRAM) Cross Section as function of Power Supply (V_{DD}) Disturbance
(**Irradiated FPGA with 750 krad**)

750 krad, pattern "all 1's" ("soft")

BRAM Cross Section as function of V_{DD} reduction/noise
Considering "Imprint Effect" [750 krad], ^{16}O (50 MeV)



σ: +27.6%

σ: +29.5%

V_{DD} noise: 16.67%voltage dips, 10 Hz, pattern "all 1's" ("soft").
σ Degradation w.r.t. the nominal V_{DD}: 8.33%

σ degradation induced by TID imprint effect: +13%

750 krad, pattern "all 0's" ("hard")

V_{DD} noise: 16.67%voltage dips, 10 Hz, pattern "all 0's" ("hard").
σ Degradation w.r.t. the nominal V_{DD}: 0%

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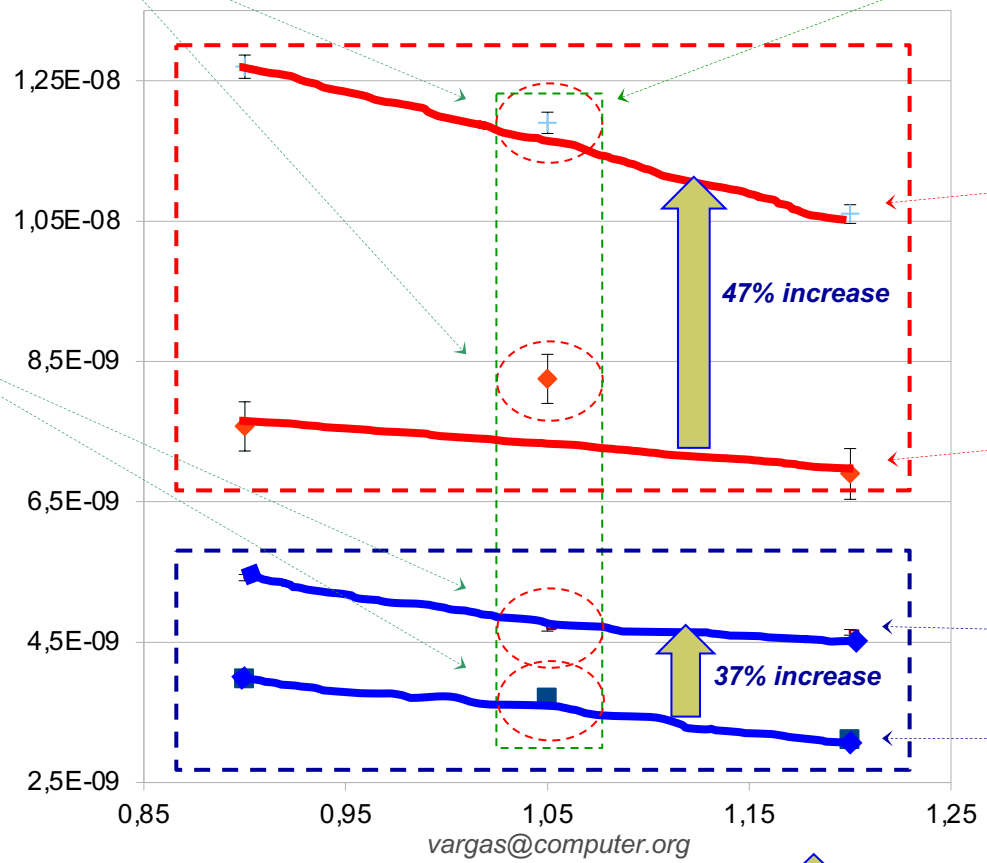
Experiment (1)

(BRAM vs. Config) Cross Section as function of Power Supply (V_{DD}) Disturbance
(**Irradiated FPGA with 950 krad, ^{28}Si**)

SEU sensitivity degradation w.r.t. the nominal V_{DD}: 16%

SEU sensitivity degradation w.r.t. the nominal V_{DD}: 10.4%

V_{DD} noise: 25%voltage dips, 5kHz



BRAM, 950 krad Pattern "All "1's" ("soft")

BRAM, Fresh Pattern "All "0's" ("hard")

Config, 950 krad

Config, Fresh

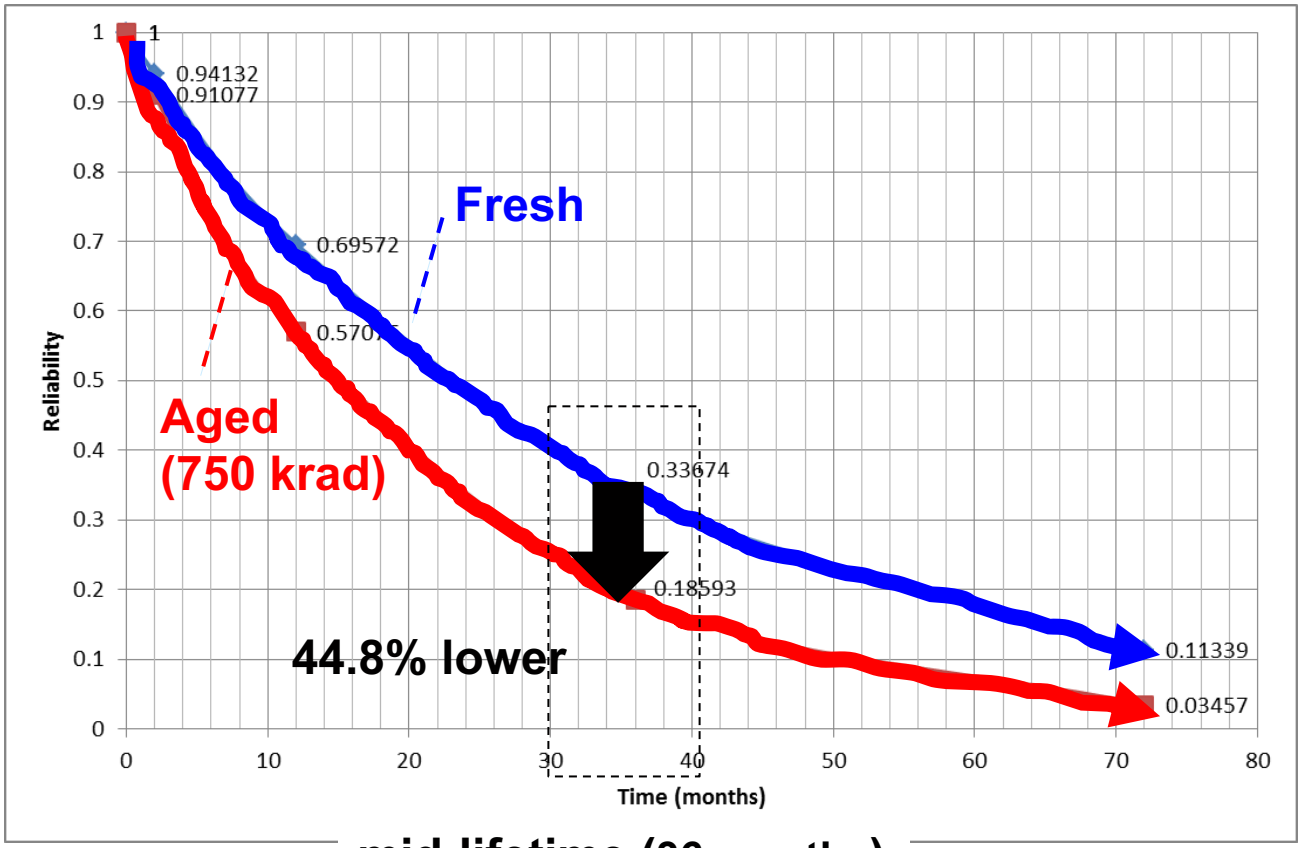
BRAM ~ x4.3 more sensitive to SEU than Config mainly due to the imprint effect

SEU sensitivity increase due to 950 krad TID

Experiment (1)

BRAM Reliability per Bit

Power Supply (V_{DD}): 0.85 volts
SEU Results for Fast Neutrons (^{241}AmBe), [2 – 11] MeV
(**Fresh x Irradiated FPGA with 750 krad, ^{28}Si**)



Mainly induced by the "soft" pattern (all 1's)

mid-lifetime (36 months)

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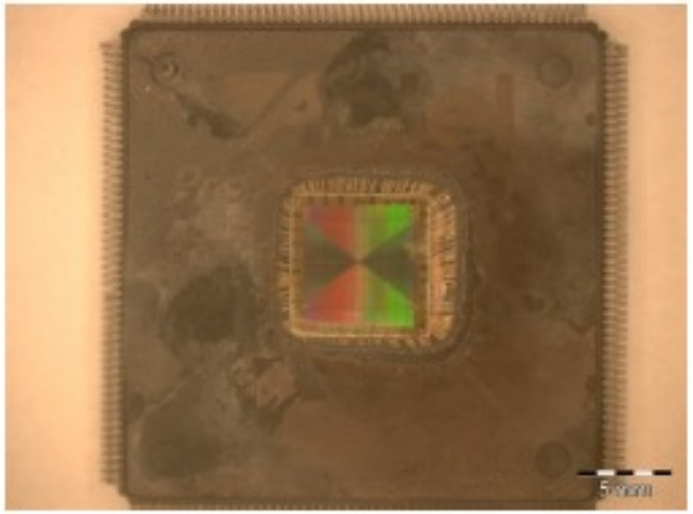
Combined Tests:

Conducted EMI + SEU

Experiment (2)

(a)



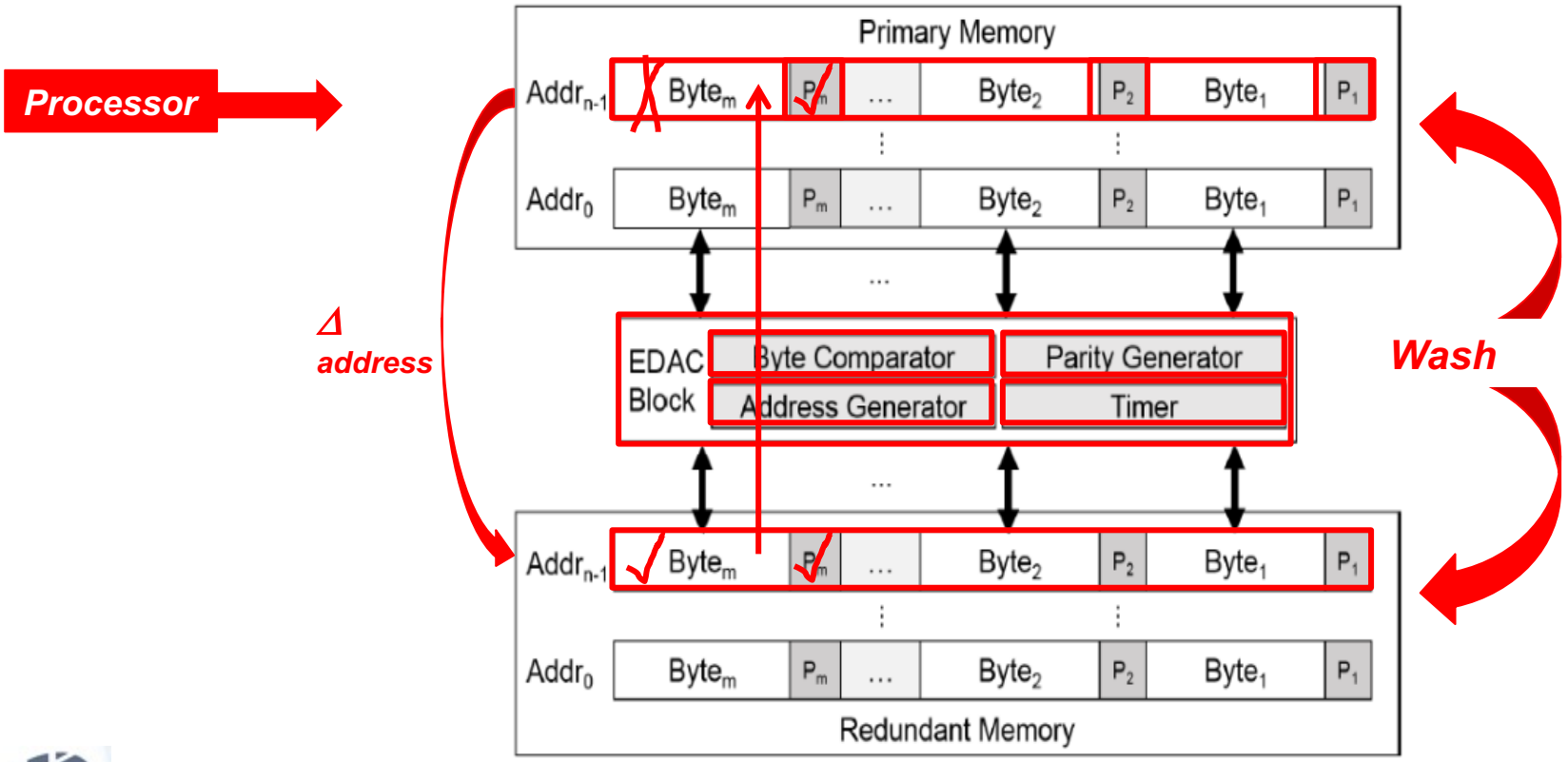
(b)

Microsemi ProAsic3E A3PE1500 FPGA:
(a) Packaged device;
(b) Unpacked, ready for radiation (SEU and TID) tests.

(commonly used for automotive and aerospace apps)

Experiment (2)

Parity per Byte & Duplication (PBD) EDAC Technique



General block diagram of the proposed EDAC approach.

Experiment (2)

SEU Test:

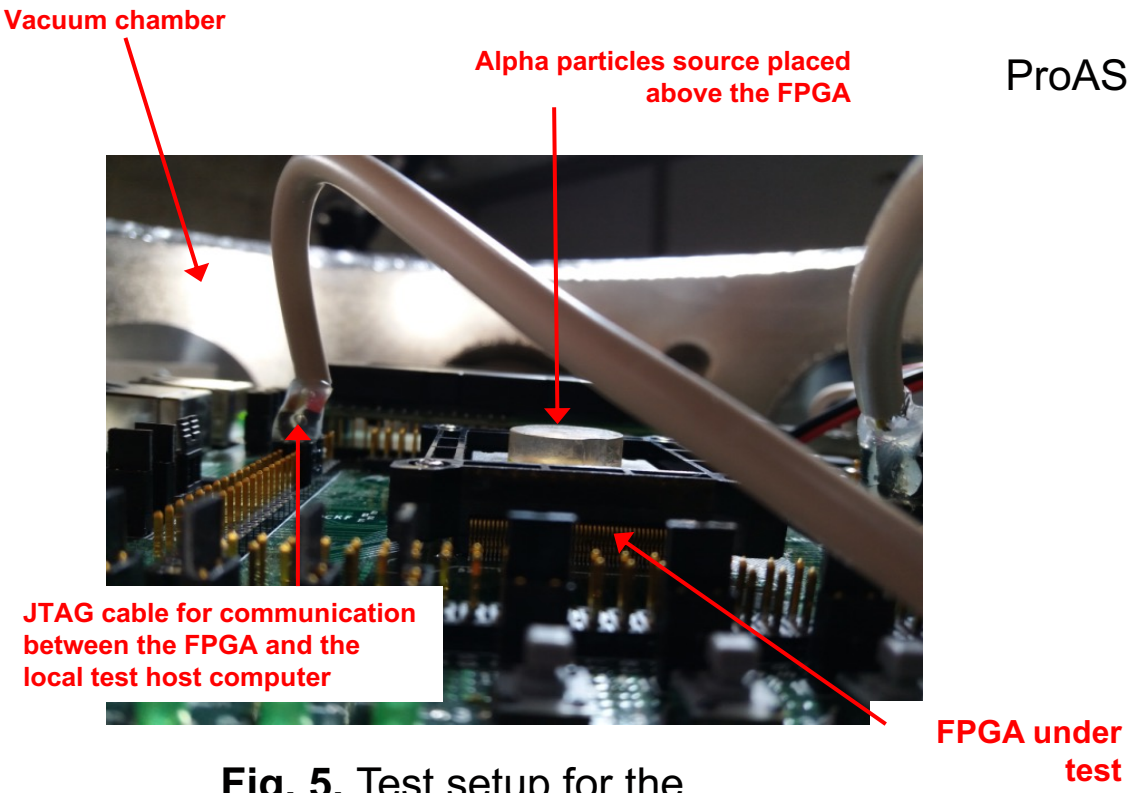


Fig. 5. Test setup for the ^{241}Am source

ProASIC3E FPGA exposed to 5.4 MeV alpha particles emitted by a ^{241}Am source

Alpha-particle flux:.
Appr. 1,300 part/cm^2.s
(13.7 particles/second /millisteradian)

Experiment (2)

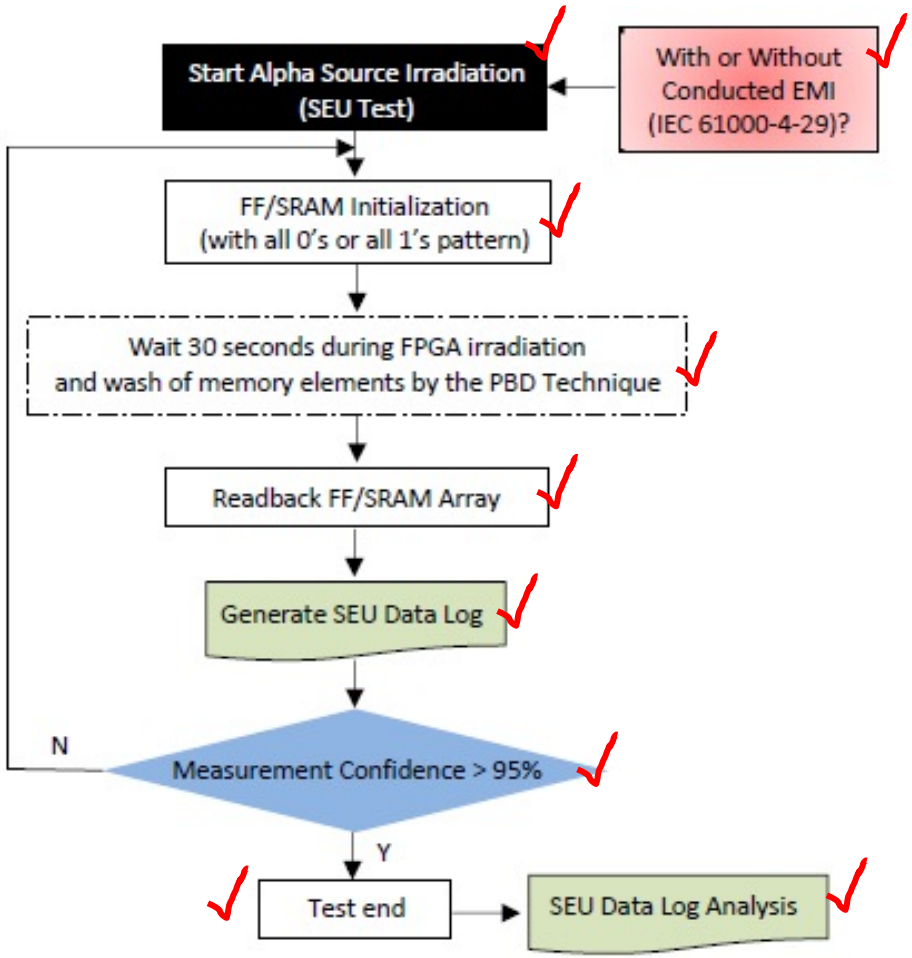
Combined Test for SEU/Conducted EMI

PROASIC3E OCCUPIED RESOURCES

FPGA Hardware Summary	Core Logic (VersaTiles)	FFs	SRAM Cells
Used hardware configuration	37,903	18,432	276,480
Max. hardware available	38,400	38,400	276,480

100%

48%

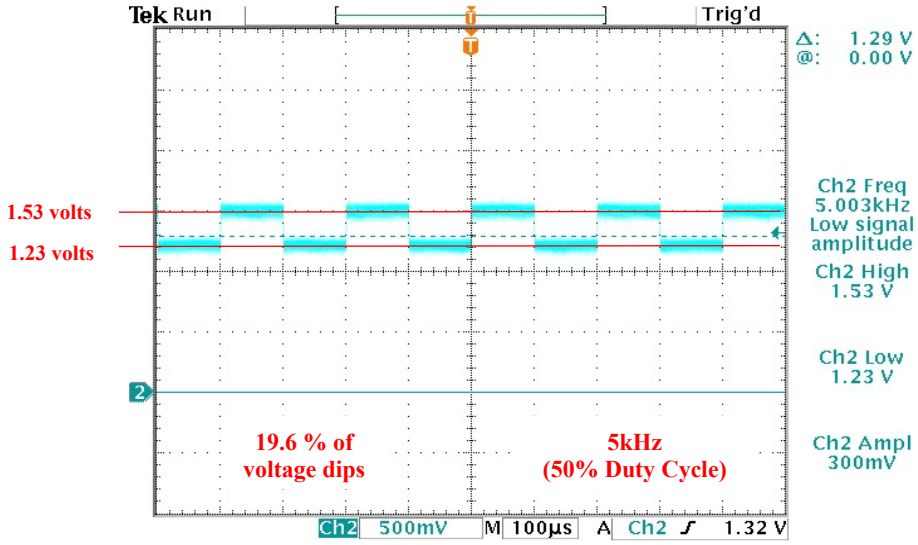


Test Flow

Experiment (2)

EMI Test:

Fault injection campaigns were generated according to the IEC 61000-4-29 Std



Voltage dips applied to the FPGA core V_{DD} pins (Nominal core V_{DD}: 1.5 volts)

IC peripheries remained fixed at their nominal voltage levels (3.3, 2.5 and 1.8 volts)

Fig. 6. Noise injected on FPGA V_{DD} pins.

Experiment (2)

Obtained Results

TABLE II.
CAPABILITY OF THE PBD TECHNIQUE TO MITIGATE SOFT ERRORS INDUCED BY ALPHA PARTICLES, WITH AND WITHOUT CONDUCTED EMI NOISE ON THE CORE INPUT POWER PORT OF THE FPGA. RESULTS FOR THE SRAM ARRAY.

PBD TECHNIQUE EFFECTIVENESS TO ALPHA PARTICLES, WITH AND WITHOUT CONDUCTED EMI NOISE ON INPUT POWER PORT			
Average number of…	Without Noise	With Noise	Soft Error Increase*
observed bit-flips	395.00	1,049.00	2.7
bit-flips per memory bits	0.0027	0.0071	2.6
bit-flips per second	0.4760	1.0708	2.3
bit-flips per memory bits per second	0.0028	0.0073	2.6
addresses corrected**	393.33	1,044.37	2.7
addresses not corrected	0.17	0.63	3.7
masked addresses***	0	0	0
EDAC Effectiveness (%)	99.96	99.94	

*"Soft Error Increase" rate computed as: With Noise/Without Noise.
**the number of addresses corrected is smaller than the number of observed bit-flips because there was at least one address with more than one bit flip.
***masked addresses are addresses not detected and not corrected, thus escaping detection by the proposed technique.

Experiment (2)

Obtained Results

Compared to only ionizing radiation, when the IC was additionally exposed to conducted EMI,
FF & SRAM arrays became
~ 2.7 times more sensitive to soft errors

Thank you for your attention …

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