Memristive In-Memory-Computing: Radiation hard Memory for Computing in Space (MIMEC)

ELICSR Training School – Granada, Spain

Emilio Perez-Bosch Quesada, Tommaso Rizzi, Eduardo Perez, Christian Wenger

26.10.2022

IHP – Leibniz-Institut für innovative Mikroelektronik

Leibniz Association

Outline

1. Introduction: memristors, RRAM and applications
2. MIMEC – goals and development
3. Radiation hardness – device level
4. System level simulation - ECC
5. Outlook

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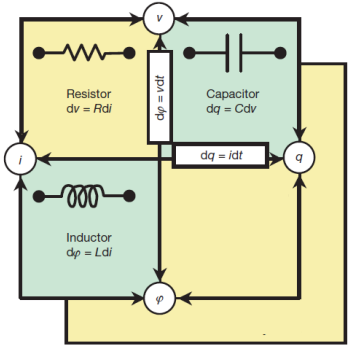


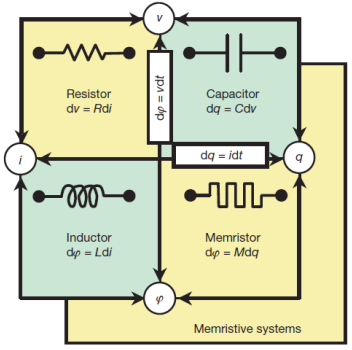
Introduction: memristors, RRAM and applications

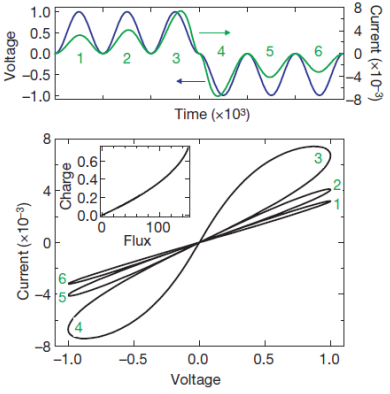
IEEE TRANSACTIONS ON CIRCUIT THEORY, VOL. CT-18, NO. 5, SEPTEMBER 1971 507

Memristor—The Missing Circuit Element

LEON O. CHUA, SENIOR MEMBER, IEEE

University of California, Berkeley





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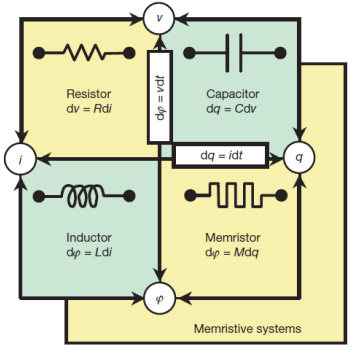

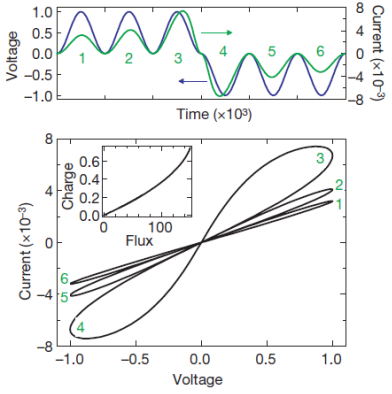

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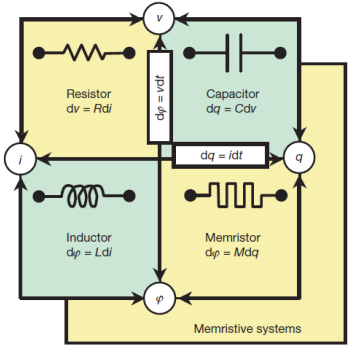

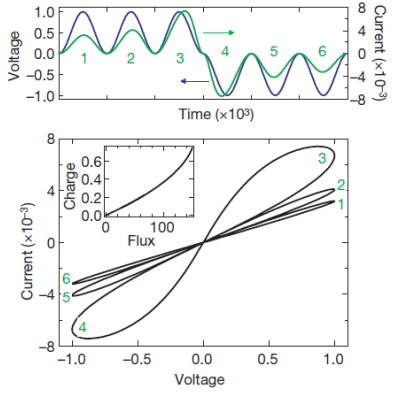

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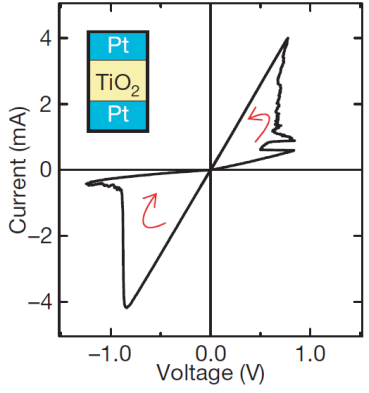
nature Vol 453 | 1 May 2008 | doi:10.1038/nature06932

LETTERS

The missing memristor found

Dmitri B. Strukov[1], Gregory S. Snider[1], Duncan R. Stewart[1] & R. Stanley Williams[1]

HP Labs



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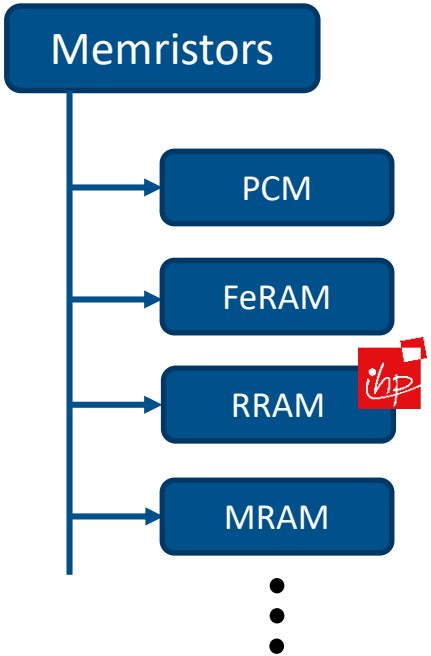

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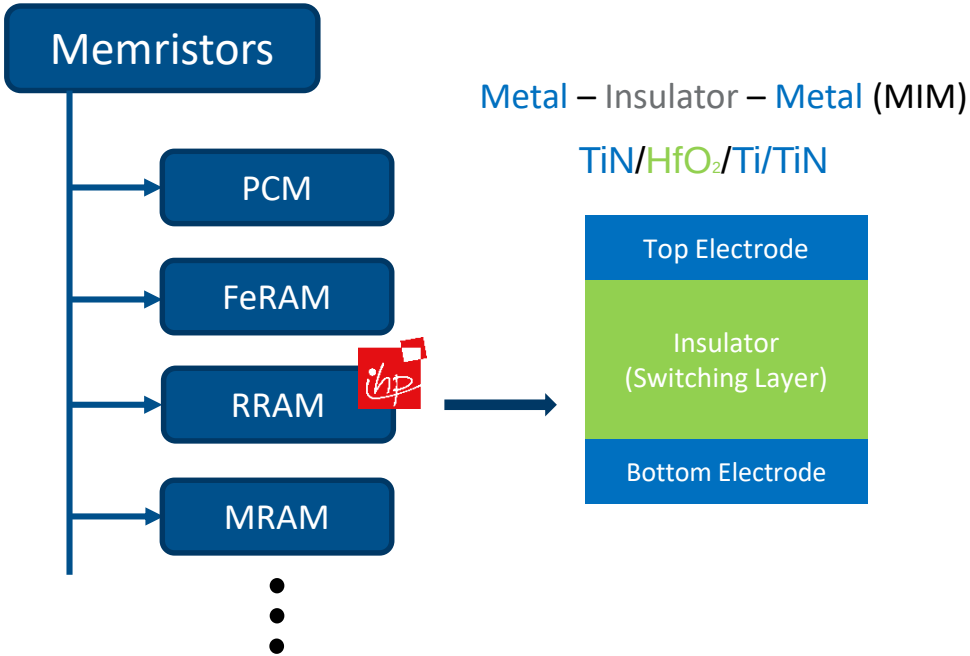

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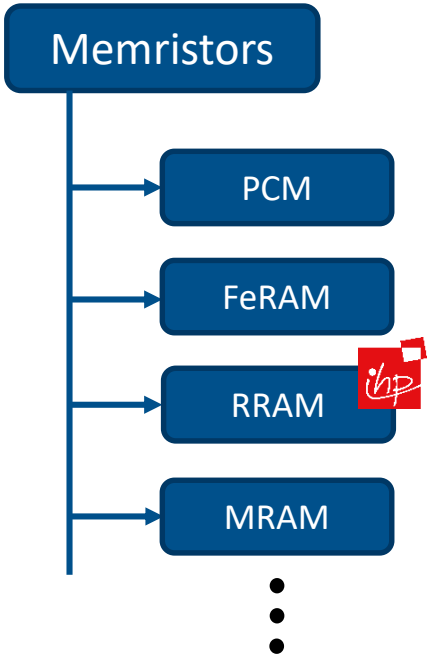
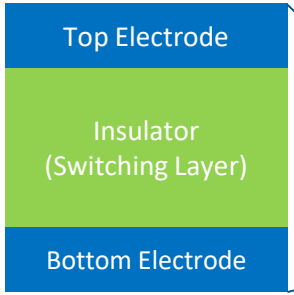
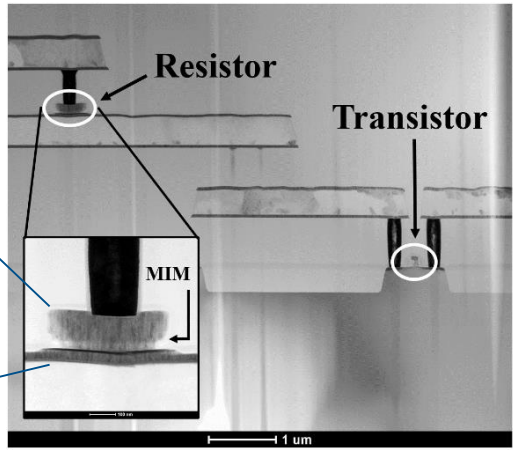


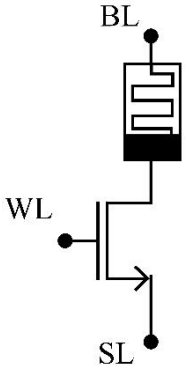
Metal – Insulator – Metal (MIM)

TiN/HfO_2/Ti/TiN



Pérez-Bosch Quesada, E., et al. Electronics (2021)





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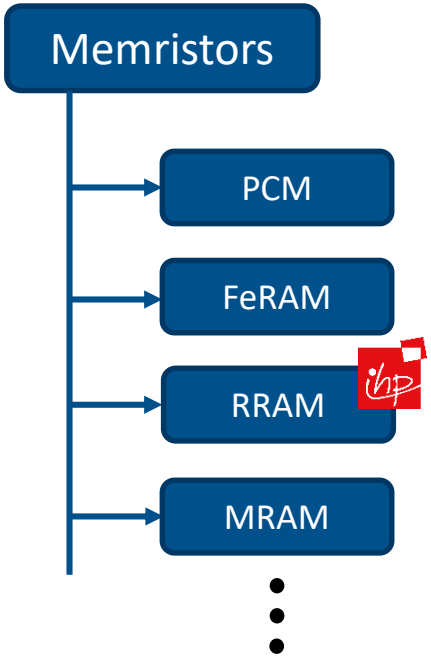

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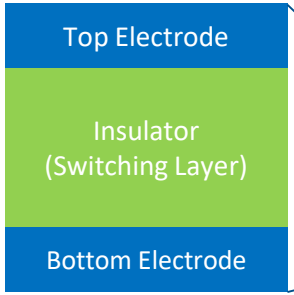

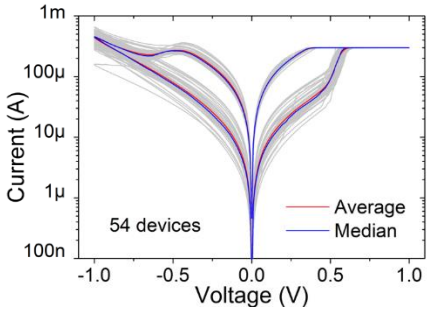

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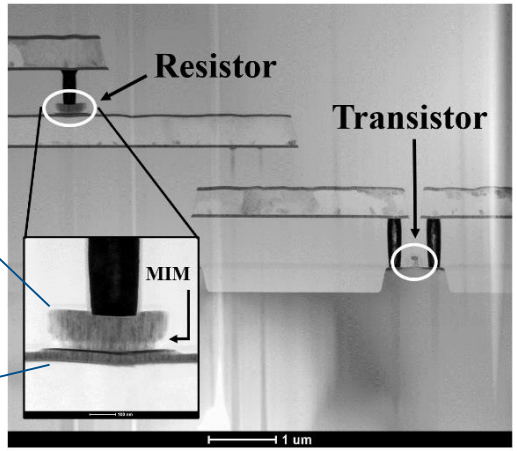
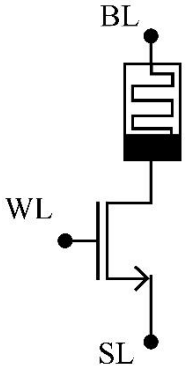
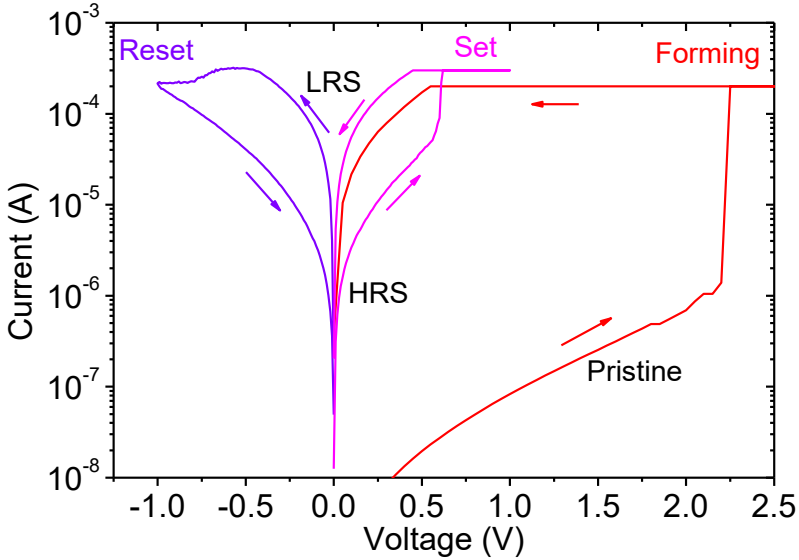




Pinched hysteresis loop

Introduction: memristors, RRAM and applications



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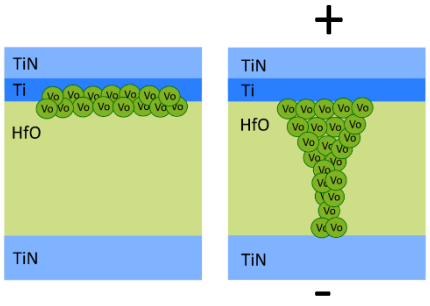
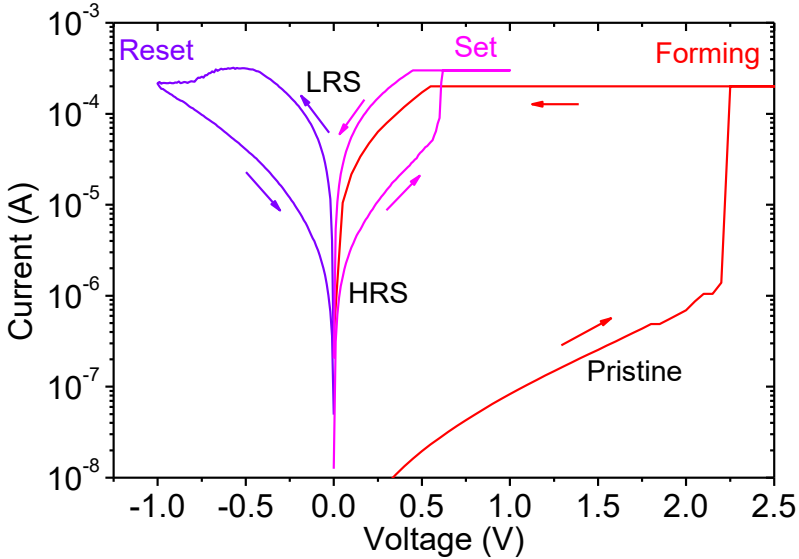


Forming

Pristine → LRS



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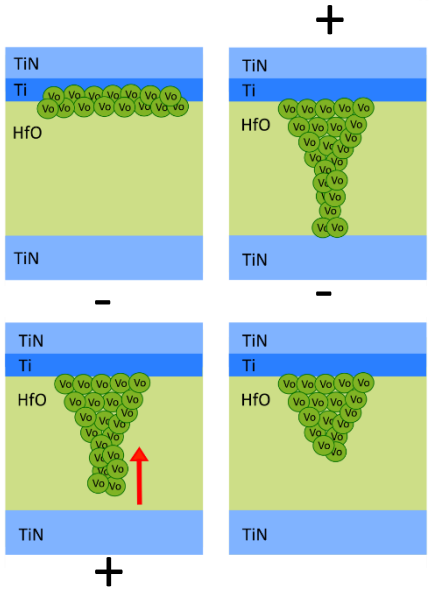
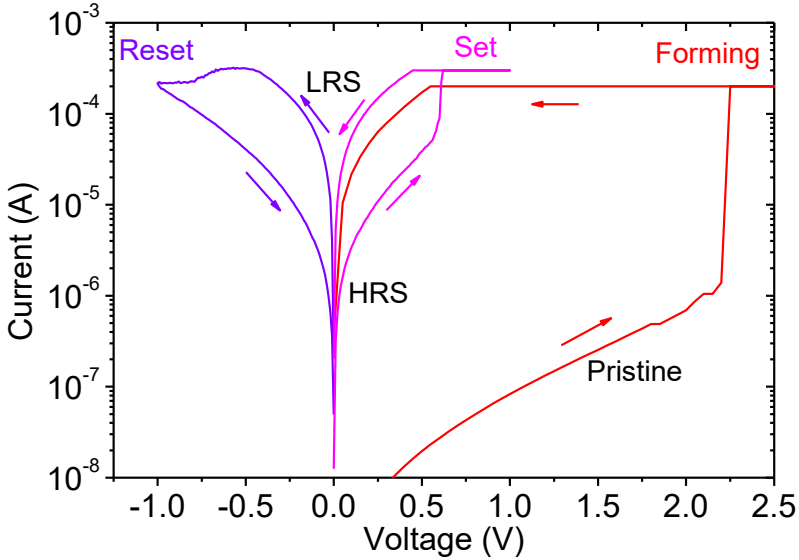


Forming

Pristine → LRS

Reset

LRS → HRS



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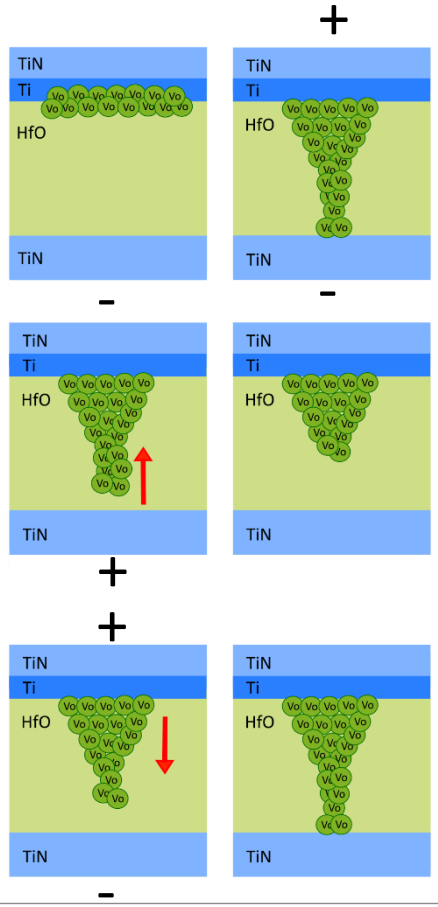

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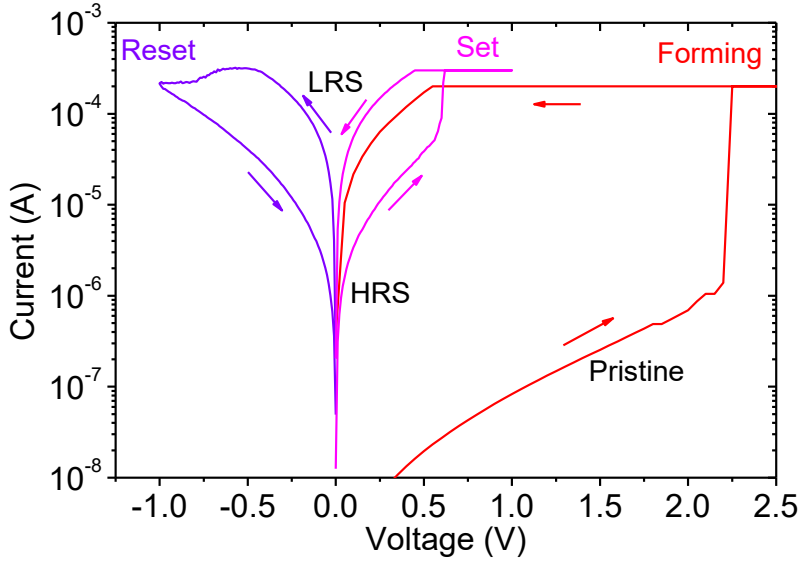
Reset

LRS → HRS

Set

HRS → LRS



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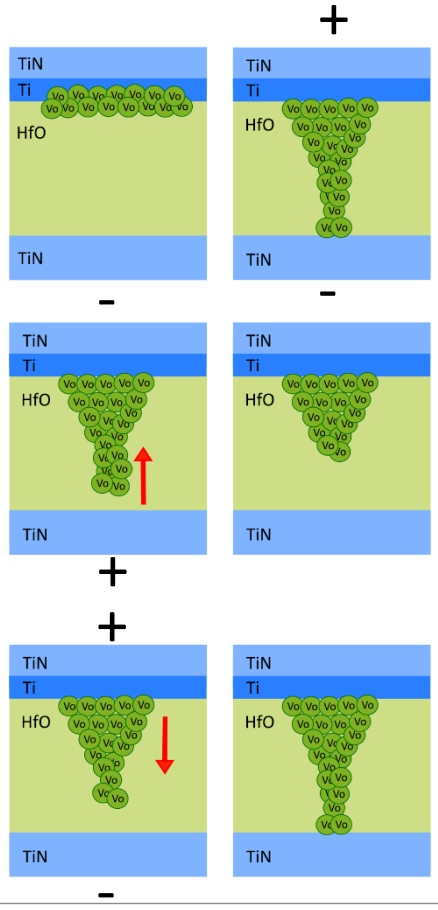

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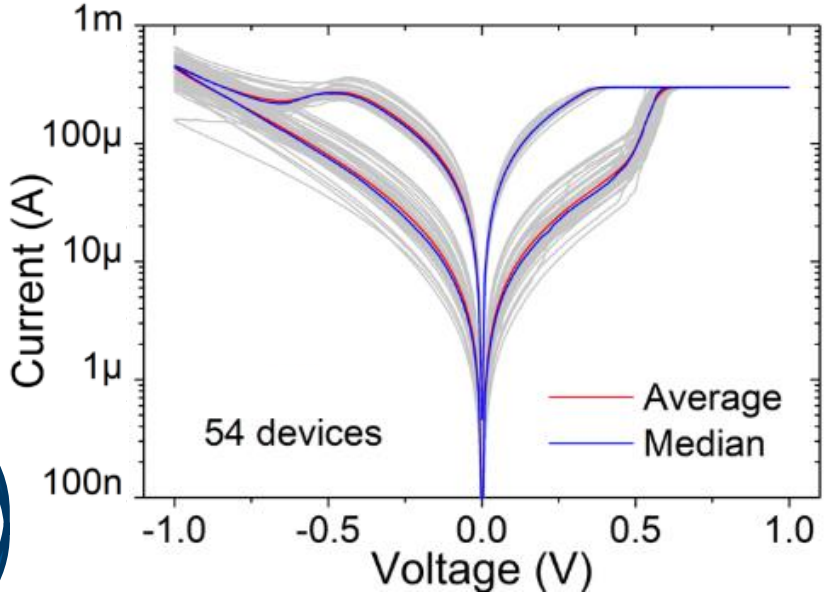

Introduction: memristors, RRAM and applications

Why 1-Ttransitor-1-Resistor structure?

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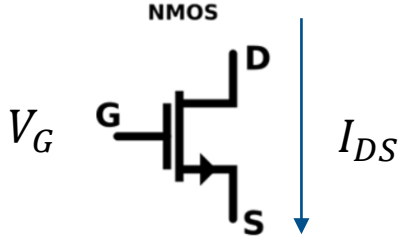

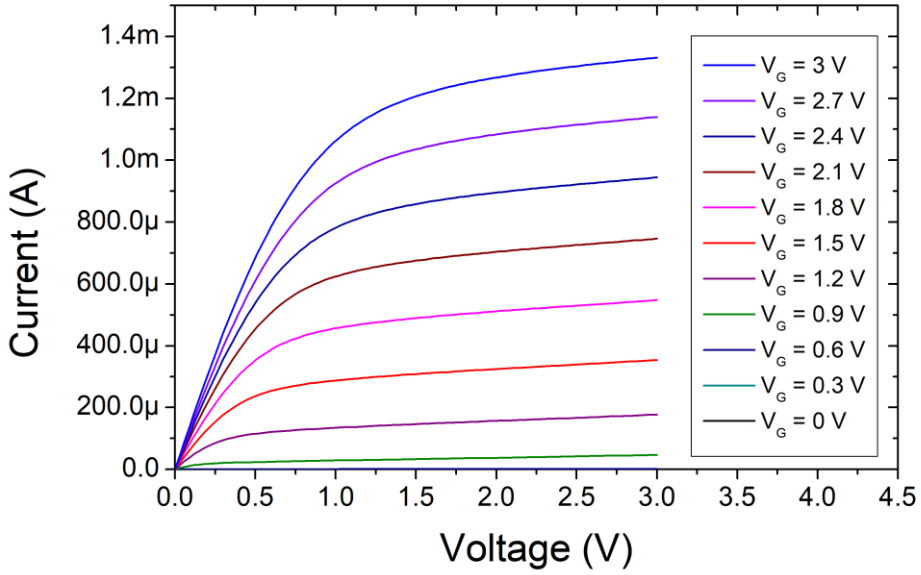

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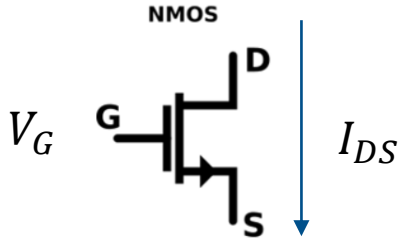
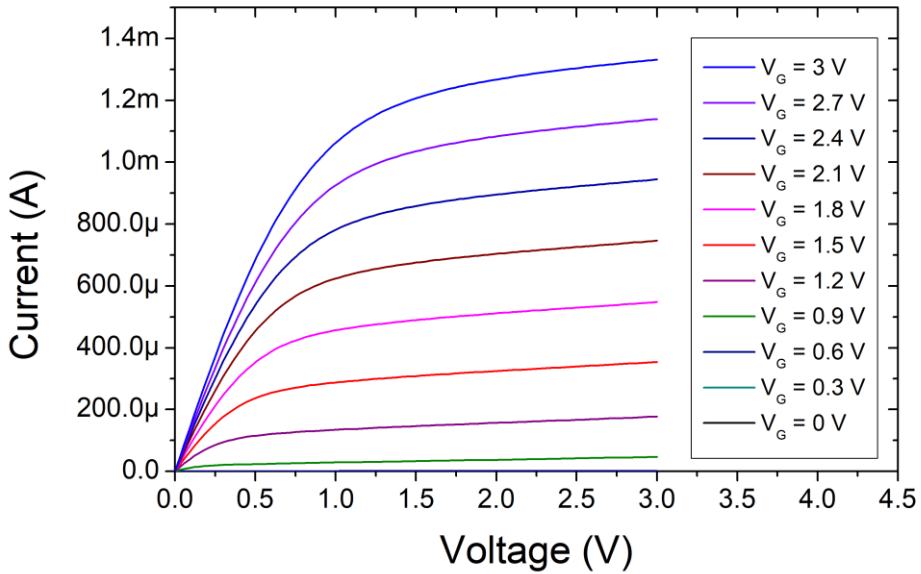
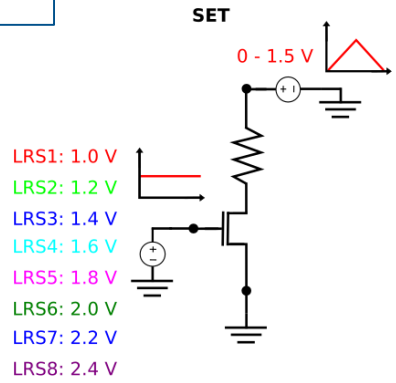


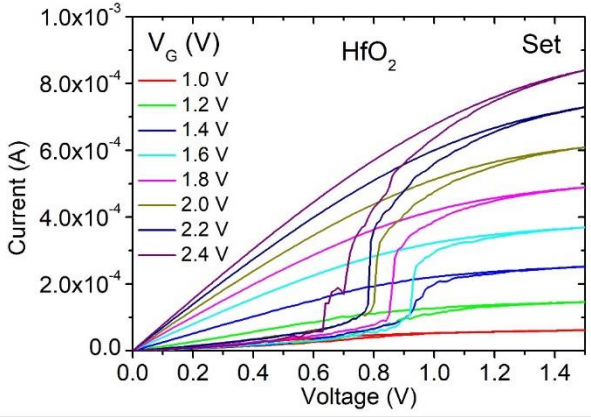
- Protects against current overshoots
- Selector device in arrays
- MULTILEVEL CELL



Introduction: memristors, RRAM and applications

Multilevel approach





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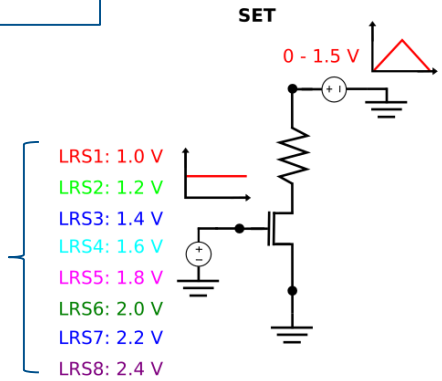
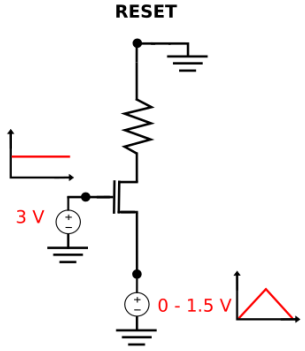
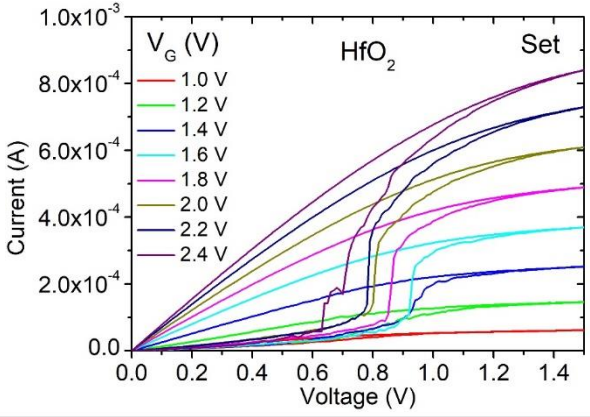
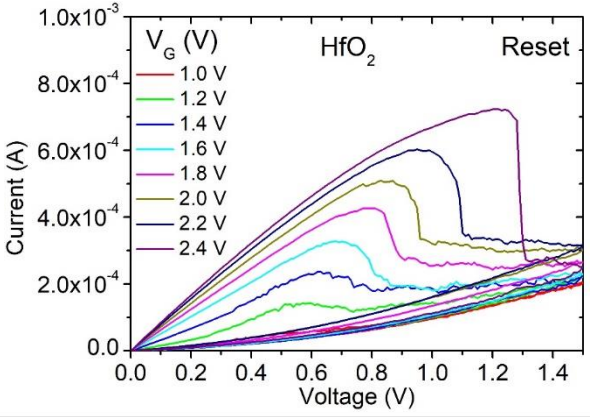
Multilevel approach

Up to 9 levels
> 3 bits









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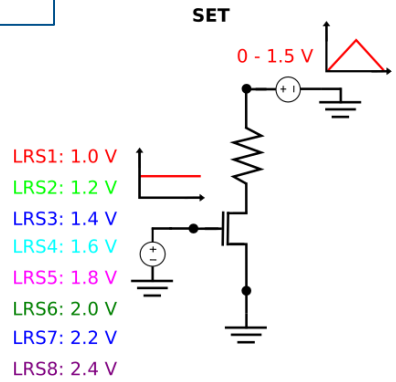

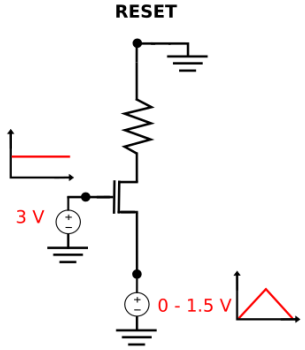

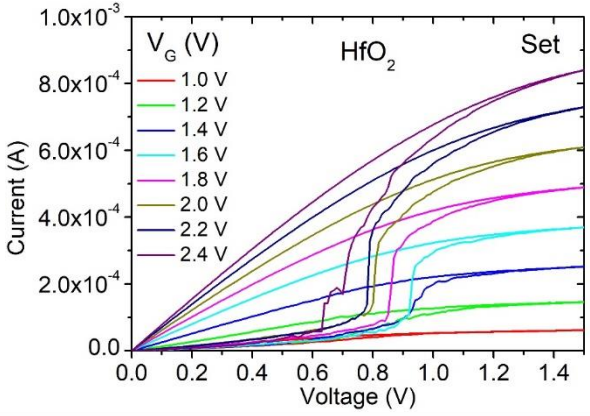

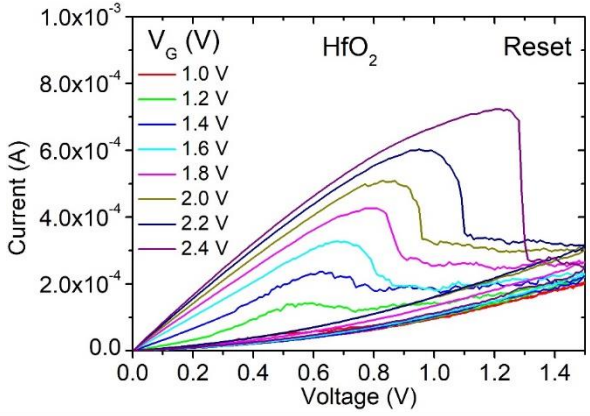

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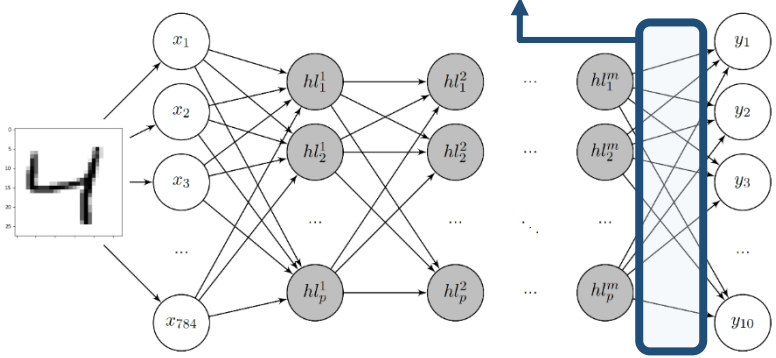
Vector-Matrix Multiplication (VMM) is the most common operation in ANNs

$$y_k = f(\hat{y}_k + b_k) \rightarrow \hat{y}_k = \sum_{i=1}^{n} x_i * w_{i\,k}$$

algorithmic



Multiply and accumulate (MAC) operations may require **several processing cycles** to be computed in traditional CPUs

In memristor crossbars, MAC operations are performed simultaneously **utilizing Kirchhoff's current law and Ohm's law.**

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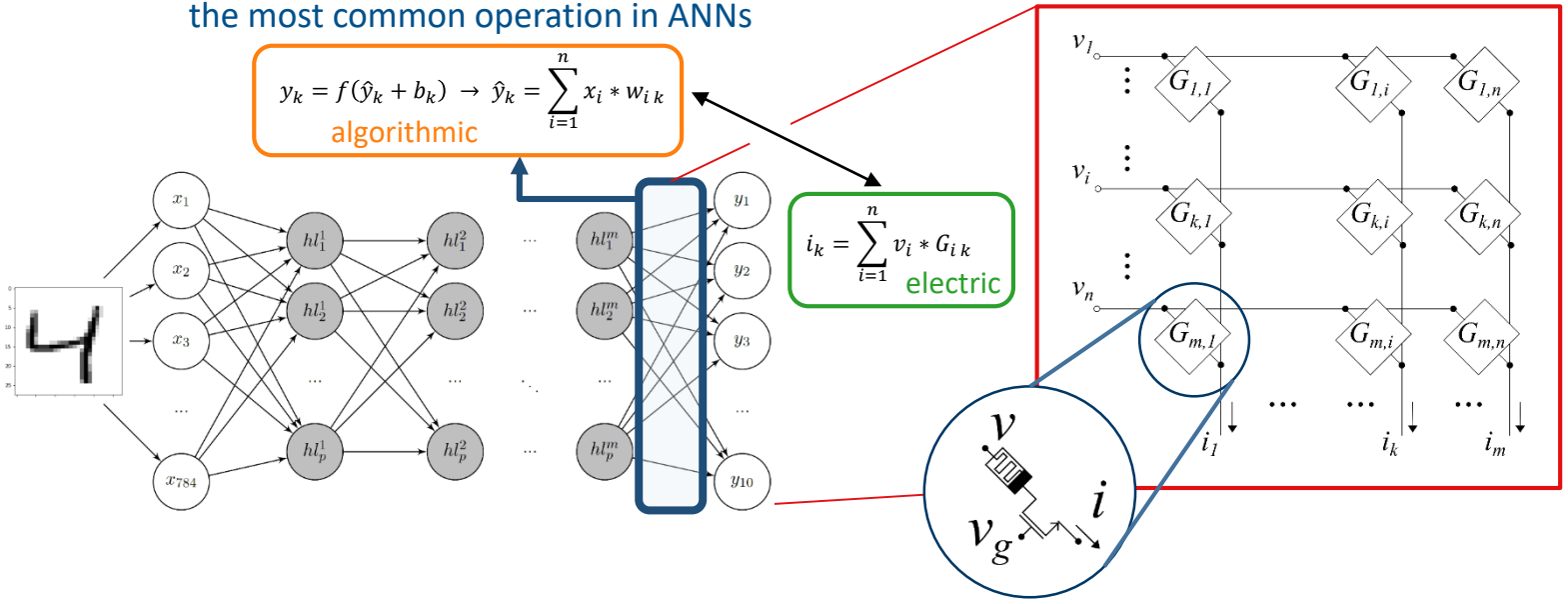
$$i_k = \sum_{i=1}^{n} v_i * G_{i\,k}$$

electric



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3. Radiation hardness – device level
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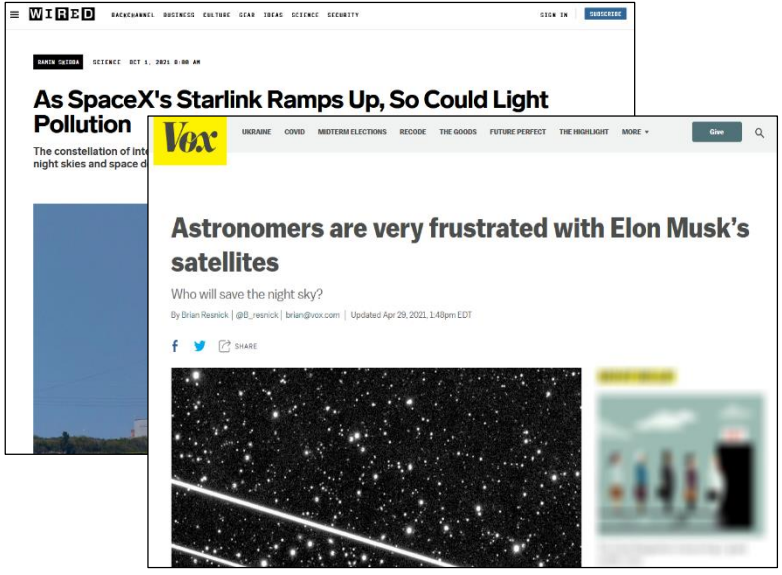
MIMEC – goals and development

Improve **Internet access** to rural and developing areas of the world.

- **Noble Cause** with high technical and optimization problems to solve
  - **Noble Cause** with controversial and vivid discussion around it



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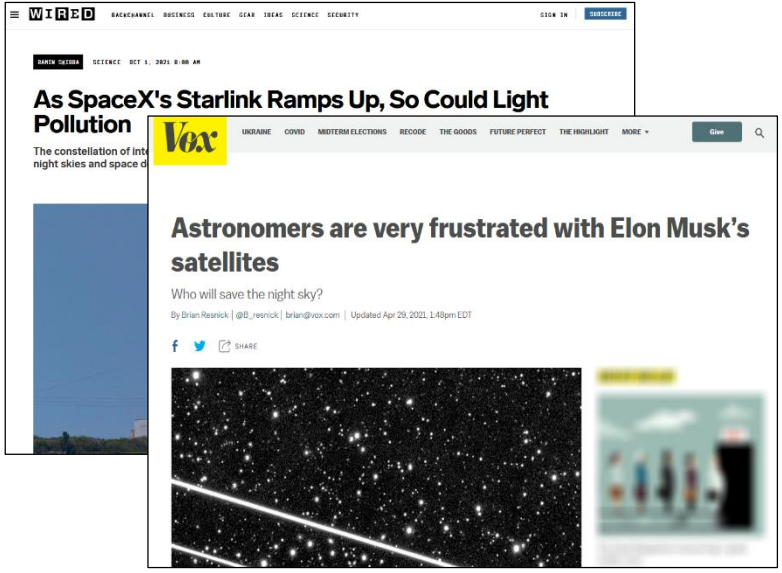

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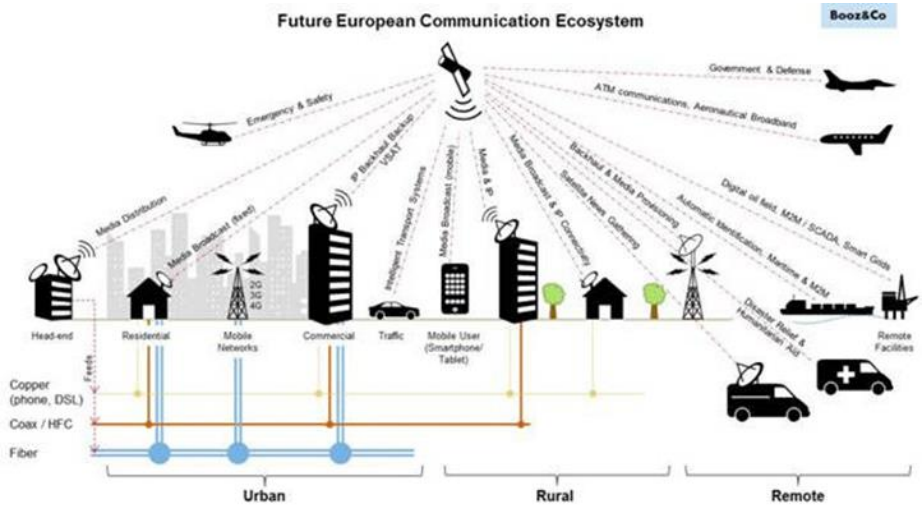


Internet of Space (**IoS**) applications:

- Computation into space
- Radiation hardened (**Rad-Hard**) electronics

https://www.networld2020.eu/satcom-wg/

MIMEC – goals and development

Conceive, realize, prototype and evaluate a RRAM-based computing architectures for IoS applications

Radiation Hardened (**Rad-hard**) **1T-1R cells**

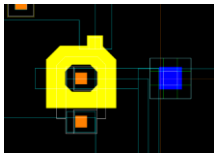
In-memory computing (**IMC**) architecture for **detection** and **correction of errors**

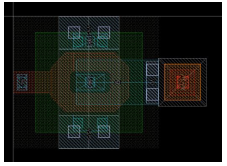
MemrisTec

Funded by DFG Deutsche Forschungsgemeinschaft German Research Foundation

Project Timeline

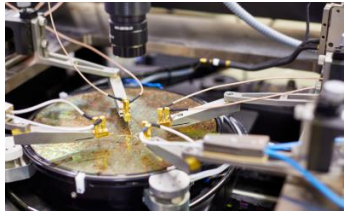
Rad-hard 1T-1R cells





Characterizations

Electrical



Radiation

RAD NEXT

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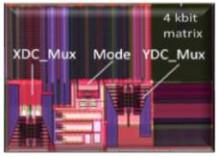
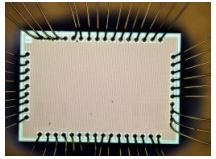
IMC Architecture for ECC





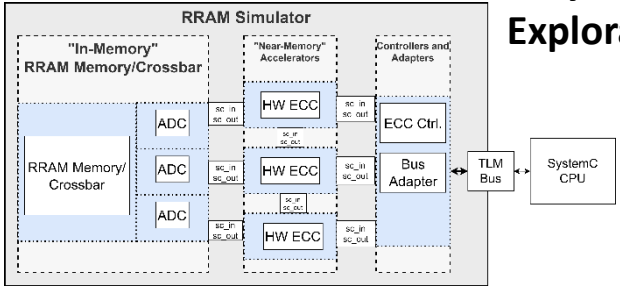
4kbits
1T-1R arrays

Requirements

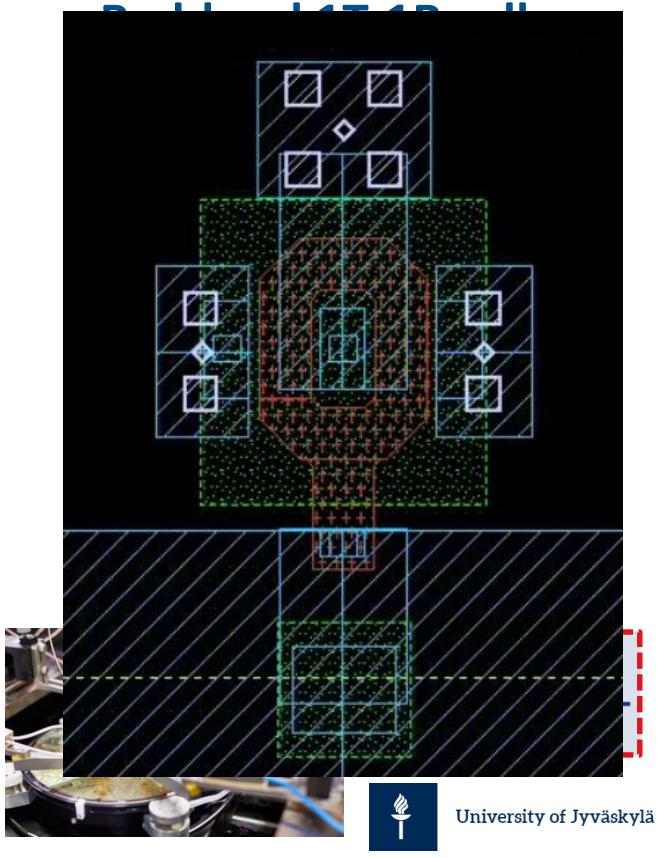
Radiation Error Model

Device Models

System Exploration



Project Timeline



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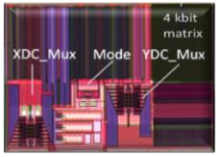
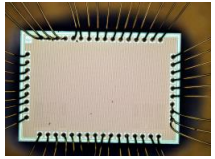
IMC Architecture for ECC





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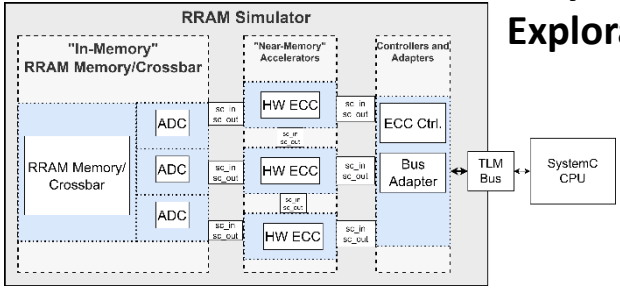
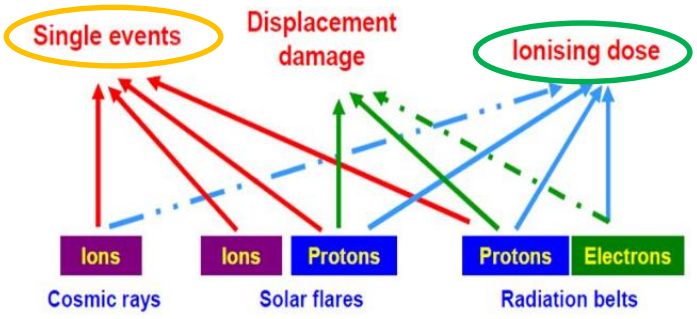


Outline

1. Introduction: memristors, RRAM and applications
2. MIMEC – goals and development
3. Radiation hardness – device level
4. System level simulation - ECC
5. Outlook

Hardness requirements for satellites

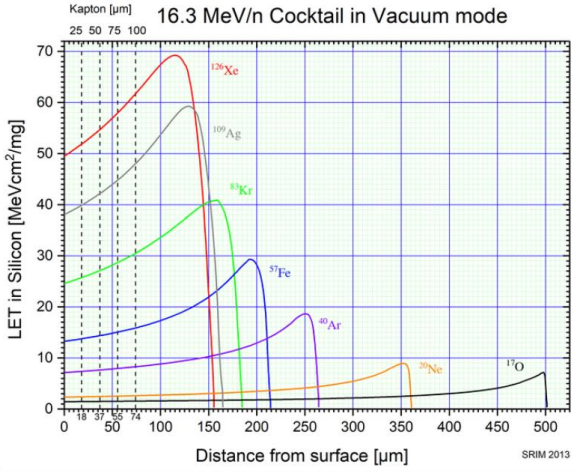
Single Event Effects threshold:
35 MeVcm²/mg



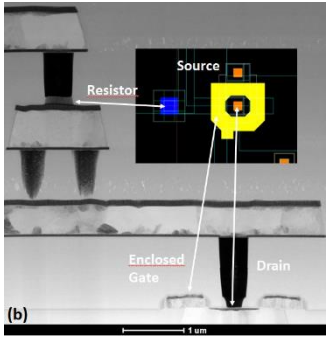
Total Ionizing Dose threshold:
50 krad

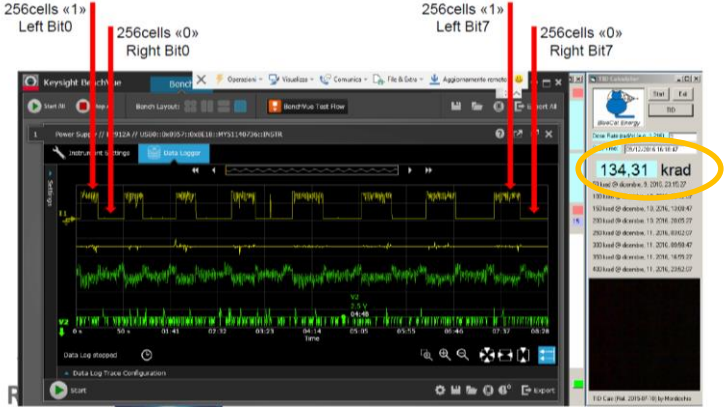
To be demonstrated for 1ELT-1R cells in MIMEC, using heavy ion cocktails at RADEF via RADNEXT

Successfully demonstrated for 1ELT-1R cells in former H2020 project R²RAM



Rad-hard 1T-1R architecture



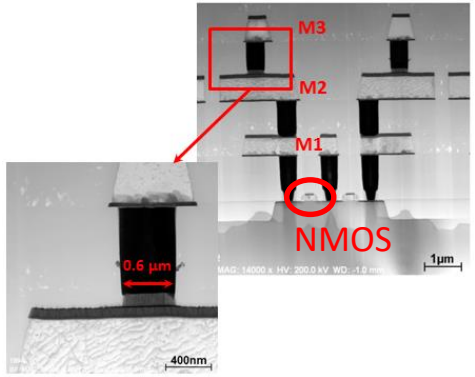


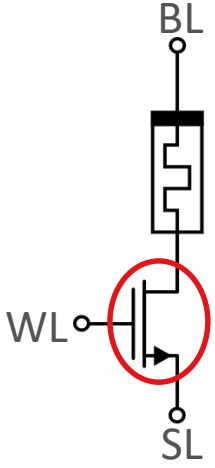
Rad-Hard 1T1R design

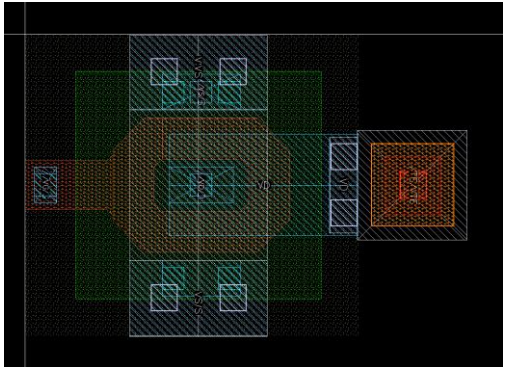
- Standard 1T1R configuration
  - MIM-Stack in BEOL → intrinsic resilient to radiation
  - Selection Transistor in substrate → prone to radiation

☑ Design of Rad-hard structure:
  - MIM-Stack in BEOL → intrinsic resilient to radiation
  - ELT-NMOS (130 nm) → TID robust

☑ Optimize transistor dimensions
  - Comparison with former measurements:
    - Change of programming voltages
    - Influence on multi-level operation
    - Influence of layout arrangements



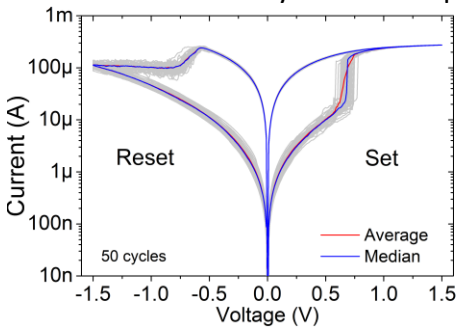




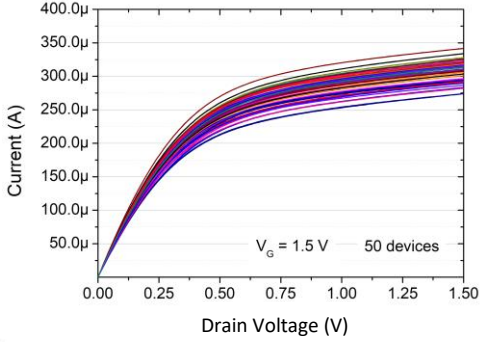
Rad-Hard 1T1R characterization

Electrical Characterization:

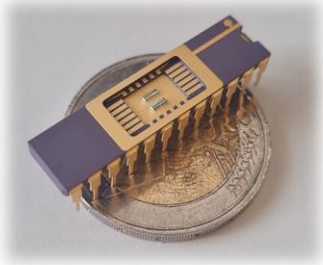
1T1R - Pinched Hysteresis Loop



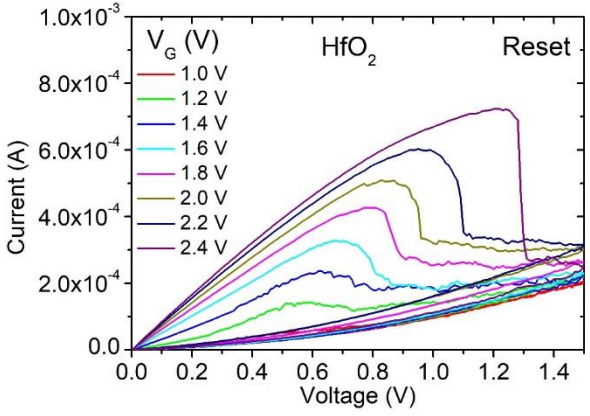
Rad-Hard NMOS

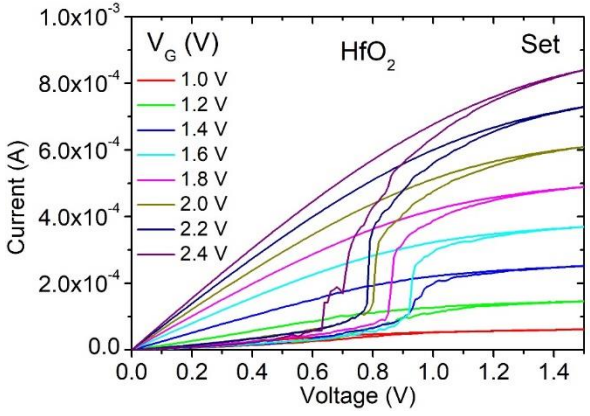


Package with opening for radiation test

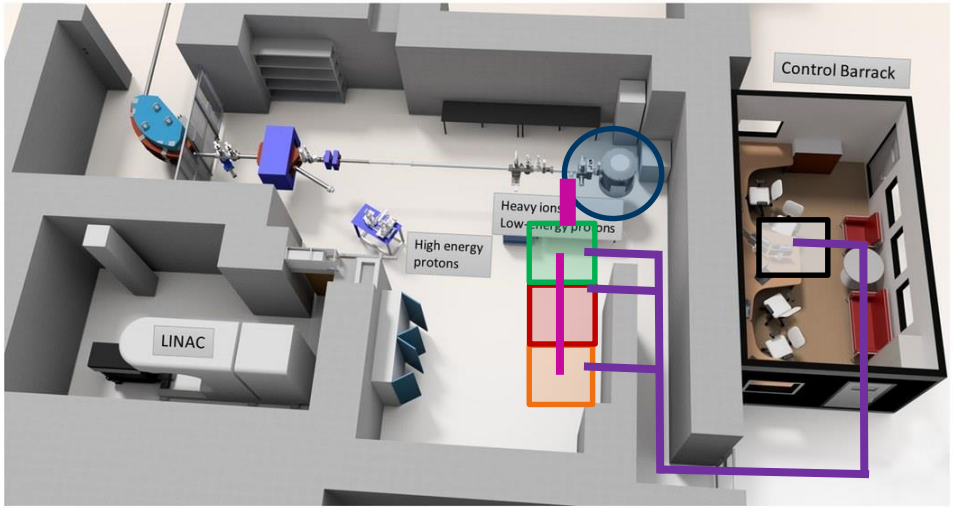


Multilevel Switching:

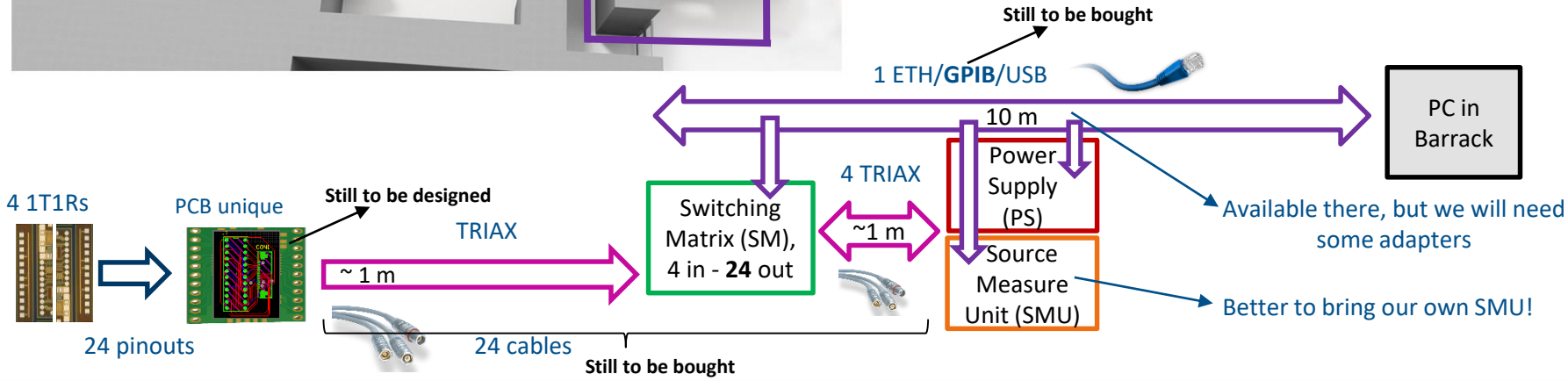




Setup



- 1 unique PCB on LAM
- PCB not affected by heavy ions [Marko, Florian, Heikki]
- Components at 2cm from irradiation are safe [Heikki]
- SMU and PS can also be inside CAVE



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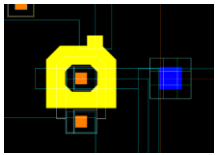
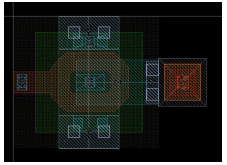
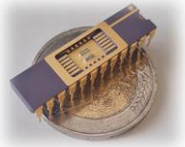
Rad-hard 1T-1R cells

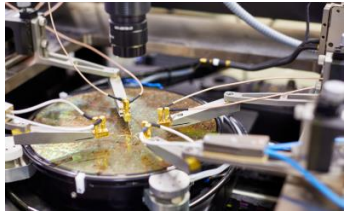






Characterizations

Electrical



Radiation

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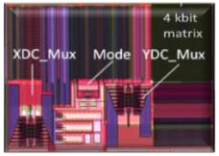
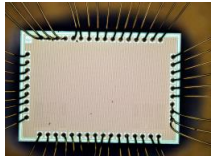
IMC Architecture for ECC





4kbits
1T-1R arrays

Requirements

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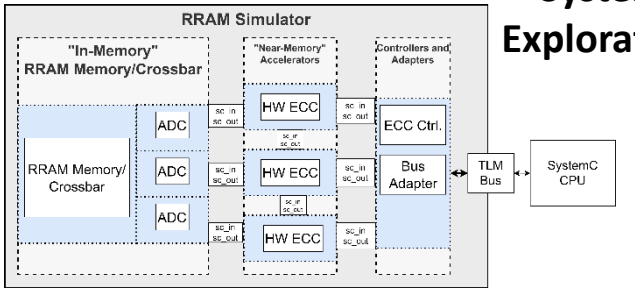
System Exploration

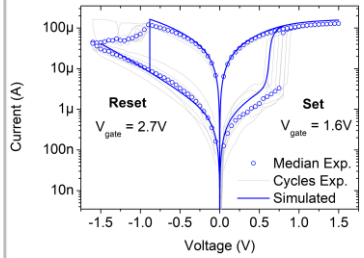


Improve Device Modeling

The memristive model must be **fast** and **"accurate enough"** in circuit/system simulations.

❑ Physical-based compact models

- Reproduce **switching mechanism**
- Difficult to capture the variability
- **Slow** (for system level)



☑ Stanford-PKU models

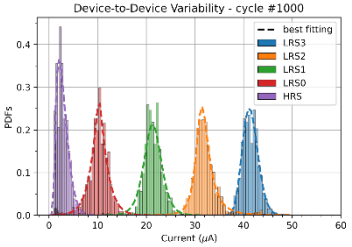
- Convergence Issues
- MLC variability

☑ **New Model**

TECHNISCHE UNIVERSITÄT DRESDEN

❑ Statistical behavioral models

- Reproduce **stochastic nature**
- **Fast**
- Difficult to capture the device's evolution



☑ Develop Framework

☑ Extract models for 4kbits arrays

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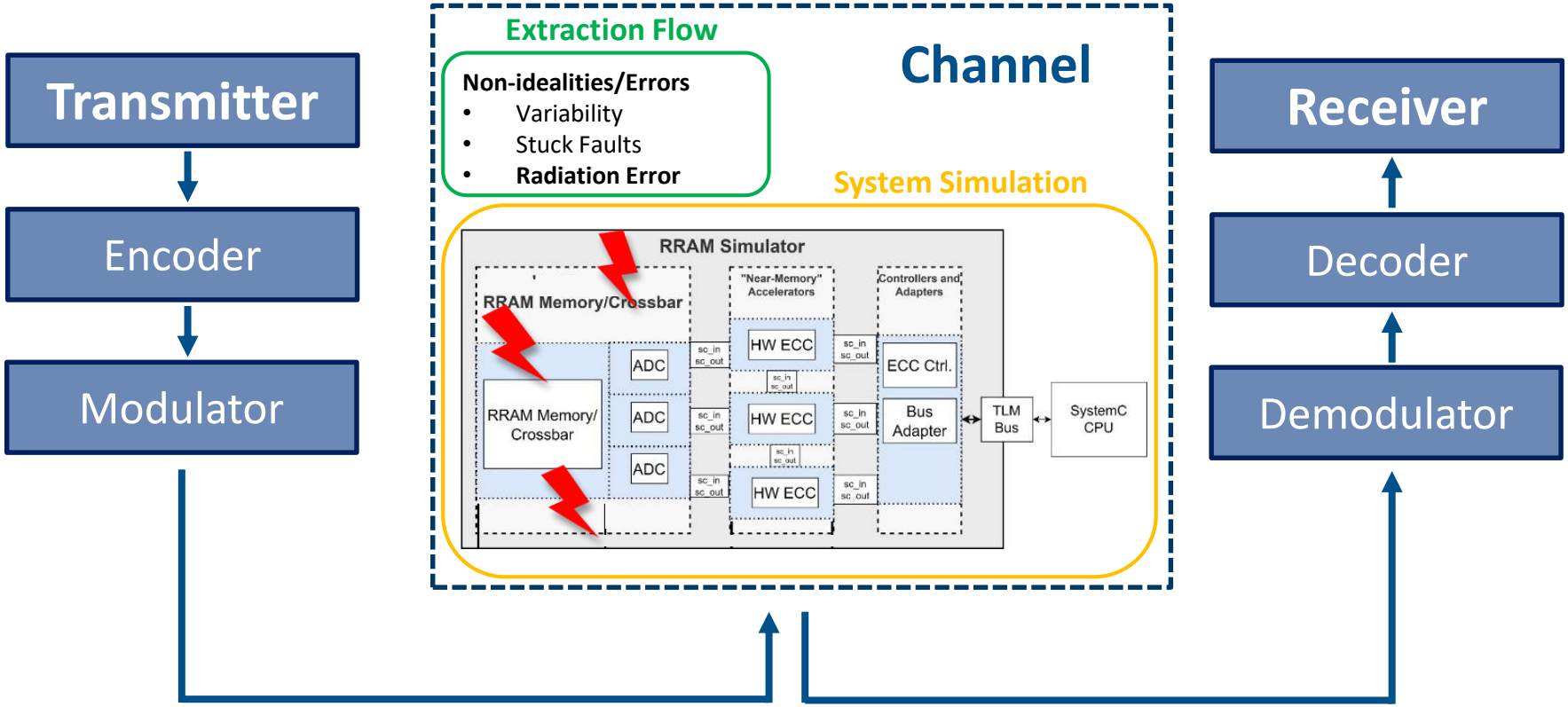
System Exploration



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Outlook

- RRAM technology inherently exhibit high radiation tolerance
- Multilevel capabilities open many design possibilities for IoS applications
  - 1ELT-1R structure demonstrated good tolerance during TID tests
  - SEE tolerance of 1ELT-1R structures will be tested in the near future
- Model development is on going
- RRAM simulator framework to optimize ECC
- RRAM-based computation systems to be deployed in radiation harsh environments

Publications

Reiser, D. *et al.* (2022). A Framework for Ultra Low-Power Hardware Accelerators Using NNs for Embedded Time Series Classification. J. Low Power Electron. Appl. 2022, 12, 2. https://doi.org/10.3390/jlpea12010002

Fritscher, M. *et al.* (2022). Mitigating the Effects of RRAM Process Variation on the Accuracy of Artificial Neural Networks. SAMOS 2021. Lecture Notes in Computer Science, vol 13227. Springer, Cham. https://doi.org/10.1007/978-3-031-04580-6_27

Rizzi T. *et al.* (2021). Comparative Analysis and Optimization of the SystemC-AMS Analog Simulation Efficiency of Resistive Crossbar Arrays. *2021 XXXVI Conference on Design of Circuits and Integrated Systems (DCIS)*, 2021, pp. 1-6, https://doi.org/10.1109/DCIS53048.2021.9666193

Pechmann, S. *et al.* (2021). A Versatile, Voltage-Pulse Based Read and Programming Circuit for Multi-Level RRAM Cells. *Electronics* **2021**, *10*, 530. https://doi.org/10.3390/electronics10050530

Pechmann, S. *et al.* (2021). A Low-Power RRAM Memory Block for Embedded, Multi-Level Weight and Bias Storage in Artificial Neural Networks. *Micromachines* **2021**, *12*, 1277. https://doi.org/10.3390/mi12111277

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Thank you for your attention!

Emilio Perez-Bosch Quesada

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