Characterization of Single Event Transient Effects in Standard Combinational Cells

Marko Andjelkovic

innovations for high performance microelectronics

24-26.10.2022, Granada, Spain

3rd ELICSIR Training School

elicsir project

Leibniz Association

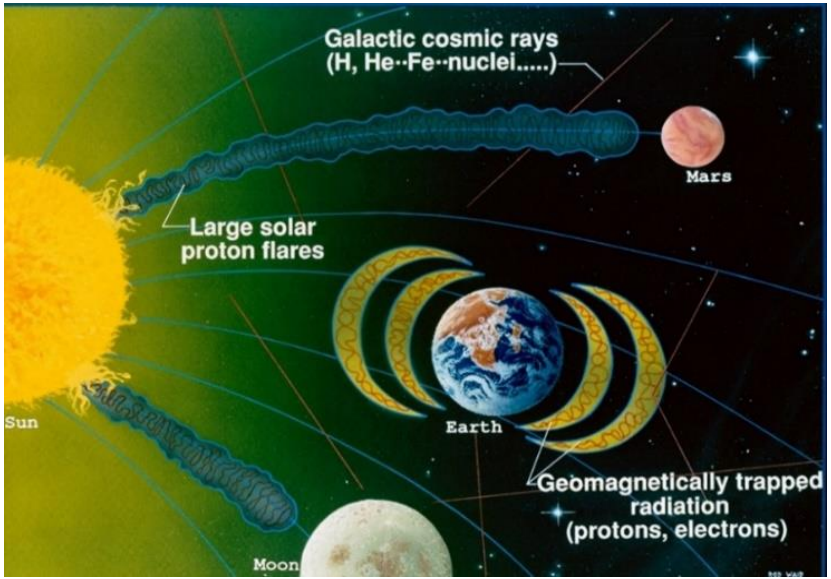
Outline

Outline

1. Motivation

- **Space radiation**
  - Galactic cosmic rays, Solar Particle Events and particles trapped in Earth's magnetic field
  - Radiation intensity may vary by several orders of magnitude over hours or days

- **Electronics employed in space should be tolerant to radiation-induced effects**
  - Cumulative Effects (CEs)
    - *Total Ionizing Dose (TID)*
    - *Displacement Damage (DD)*
  - Single Event Effects (SEEs)
    - *Soft SEEs - data loss and temporary failures*
    - *Hard SEEs - permanent failures*

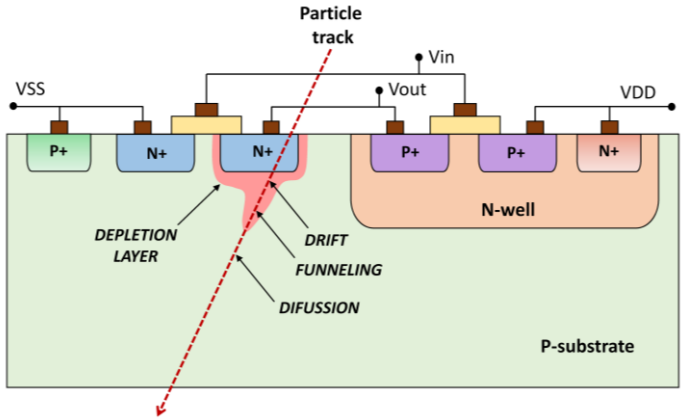


[Illustration from https://www.nasa.gov]

1. Motivation

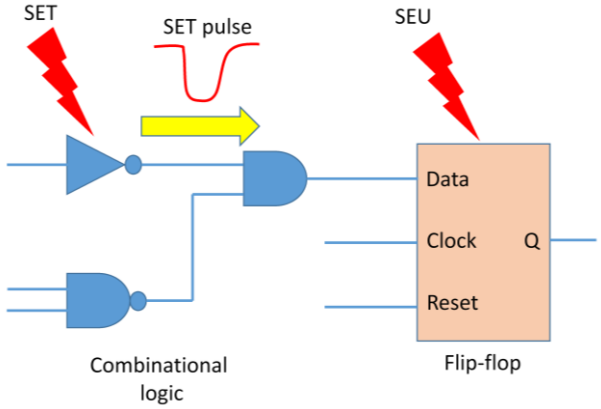
Soft SEEs (soft errors)

- Major reliability threat for CMOS integrated circuits (ICs) operated in space
- Caused by a single energetic particle (heavy ion, proton, neutron, electron)
- Manifested as unwanted bit-flips in data storage elements (flip-flops, latches, SRAM cells)



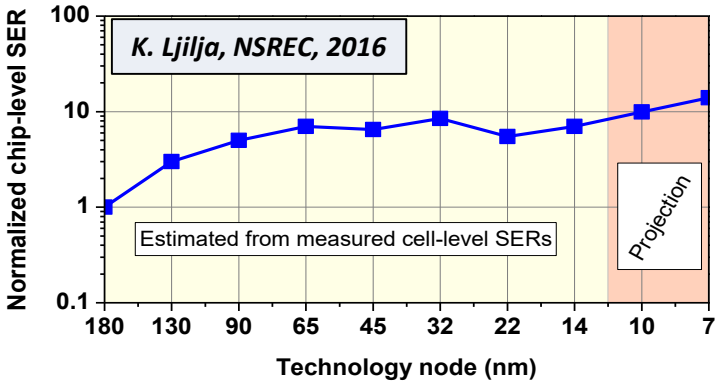
Two scenarios for soft error occurrence

1) Particle strike in a storage element, resulting in a bit flip (Single Event Upset – SEU)
2) Particle strike in a combinational gate, resulting in a voltage pulse (Single Event Transient – SET), which then propagates to a storage element

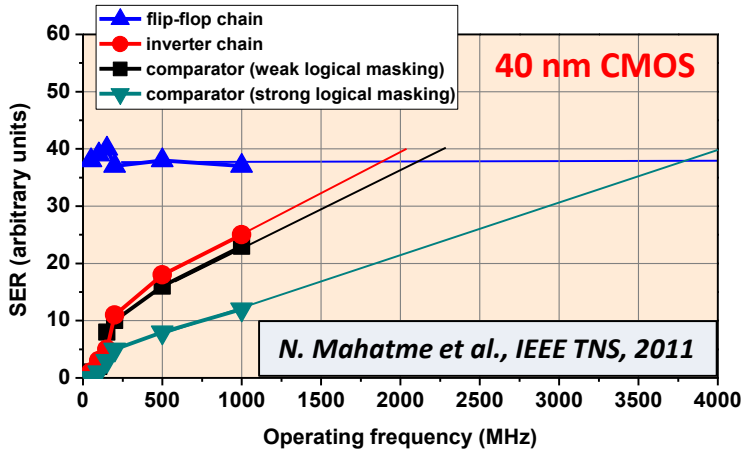


1. Motivation

- **Technology scaling effects**
  - Increase of total Soft Error Rate (SER) due to increase of IC complexity
  - Soft errors have become relevant even for terrestrial safety-critical applications



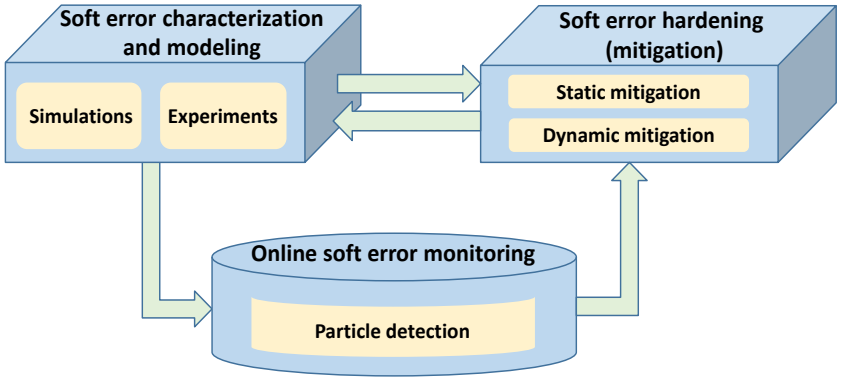
- **Contribution of SETs to the total SER of an IC increases with technology scaling**
  - Increase in operating frequency leads to an increase of SET latching probability
  - Decrease in supply voltage leads to an increase of SET generation probability
  - Decrease in logic path length leads to a decrease of logical and electrical masking probabilities



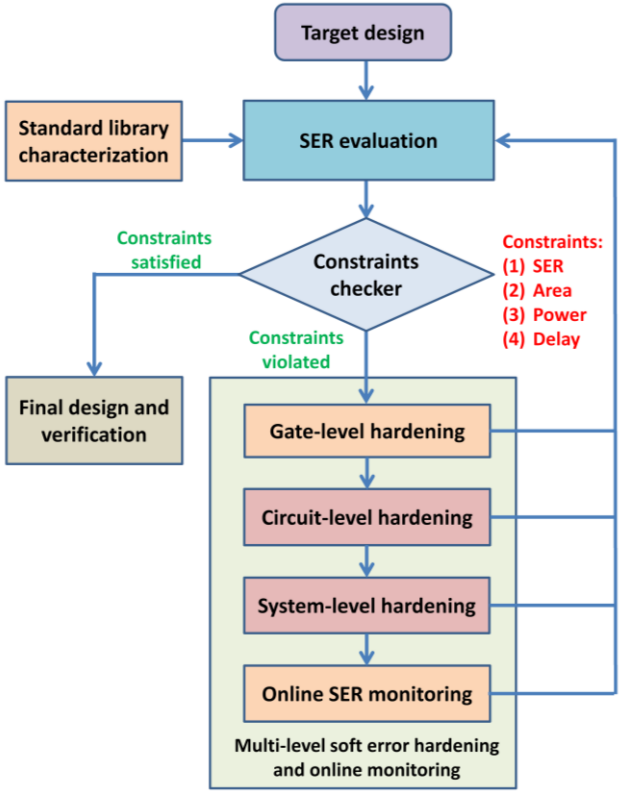
1. Motivation

Soft-error-aware IC design

- Characterization and modeling of soft error effects at device, circuit and system levels
- Multi-level static and dynamic mitigation of soft error effects (radiation hardening by design)
- Online monitoring of soft errors (energetic particles) as a support for dynamic fault tolerance



Multi-level design flow

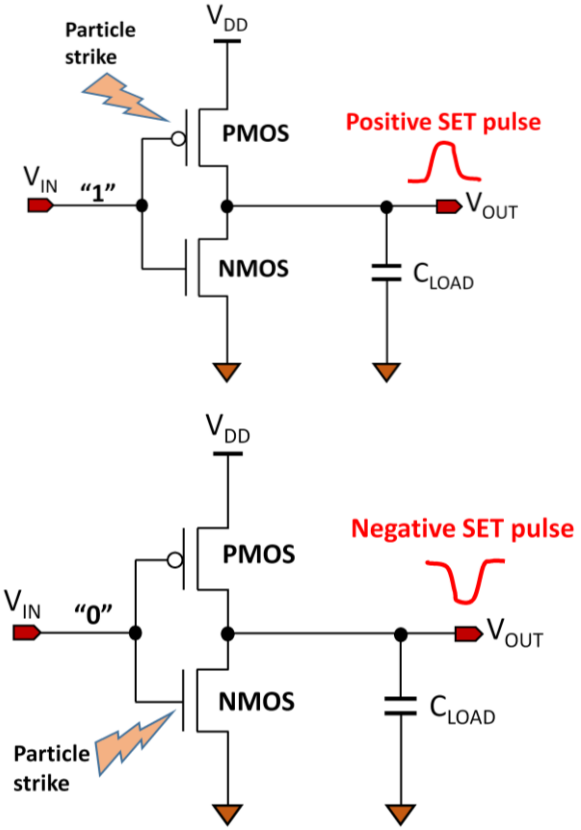


Outline

2. Fundamentals of SET Effects

SET generation

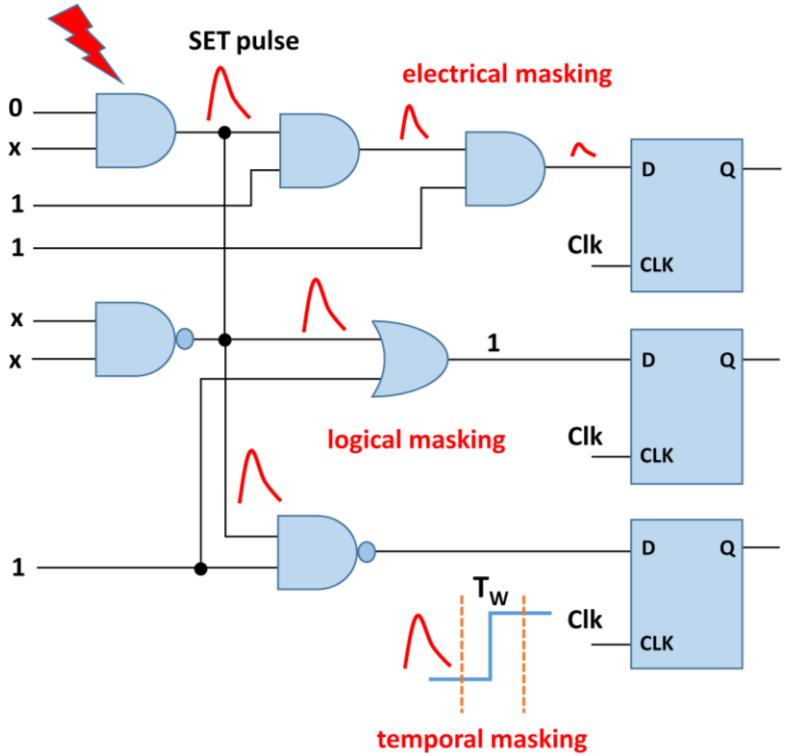
- Particle-induced current pulse results in a positive or a negative voltage pulse at the output of a gate
- Off-state transistors are most sensitive to particle strikes, due to existence of reverse-biased p-n junctions
- On-state transistors act as restoring elements, i.e., provide restoring current to counteract the particle-induced current
- One particle can hit multiple transistors, causing multiple SETs
- Typical SET pulse width - from tens to hundreds of picoseconds



2. Fundamentals of SET Effects

SET propagation

- Due to masking effects, only a fraction of gates in a circuit may cause soft errors
  - *Electrical masking (SET suppression)*
  - *Logical masking*
  - *Temporal masking*
- Propagation-induced pulse broadening (PIPB)
  - *The SET pulse may be broadened during propagation through certain paths*
- Propagation-induced SET multiplication
  - *A single SET may result in multiple SETs due to branching*



2. Fundamentals of SET Effects

- **Metrics for quantifying the SET sensitivity of a gate, circuit or system**
  - Critical charge (threshold LET): minimum charge (LET) which causes a voltage pulse with amplitude beyond the half of supply voltage
  - Generated SET pulse width: width of SET pulse generated at the output of a logic gate
  - Propagated SET pulse width: width of SET pulse after propagation through a gate or path
  - Soft Error Rate (SER): number of errors in a given time interval (overall SET sensitivity)

- **SET sensitivity is affected by numerous parameters**
  - Design parameters: target gate type and size, load gate type and size, circuit structure
  - Operating parameters: input logic levels, supply voltage, temperature
  - Radiation parameters: charge (LET), angle and position of particle strike
  - Technology parameters: doping profiles, device geometry
  - Other reliability mechanisms: aging, manufacturing defects, process variations

2. Fundamentals of SET Effects

- **Combinational Soft Error Rate (SER) –** *number of soft errors in a system induced by SETs in a given time interval*

$$SER = \sum_{i=1}^{N} SER_{NOMINAL}(i) \cdot SER_{DERATING}(i)$$

N = number of components in the system

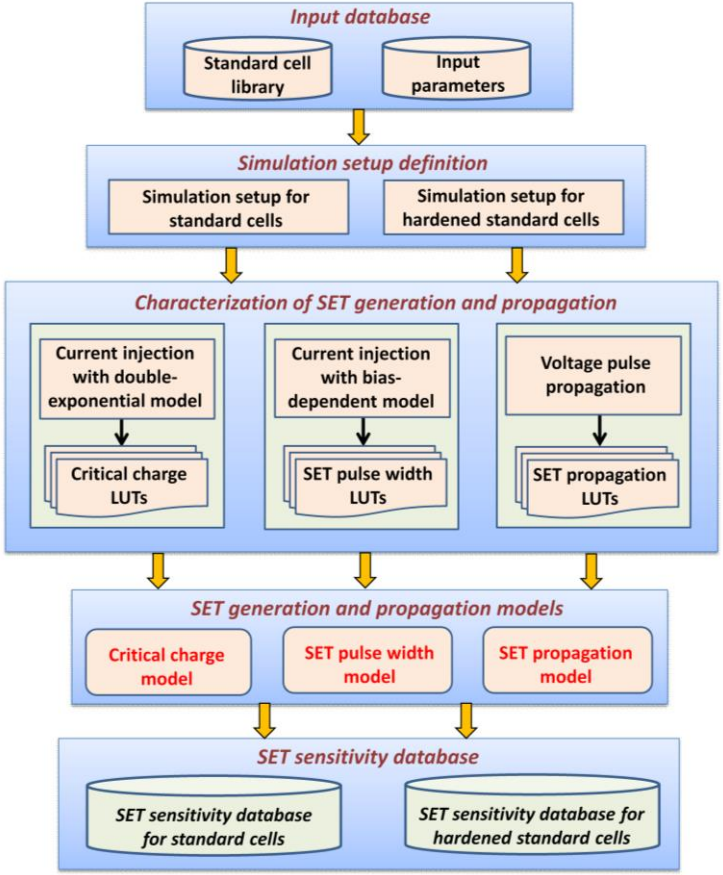
$$SER_{NOMINAL} = k \cdot Flux \cdot Area \cdot e^{-\frac{Q_{CRIT}}{Qs}}$$

$$SER_{DERATING} = Logical_{DER} \cdot Electrical_{DER} \cdot Timing_{DER}$$

Outline

3. SET Characterization Methodology

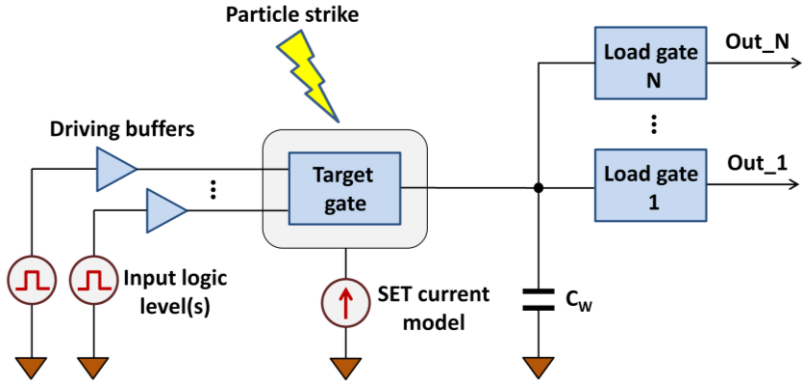
- **Joint characterization of SET sensitivity of <u>standard cells</u> and their <u>hardened variants</u>:**
  - Analysis of the SET sensitivity metrics for standard cells in terms of contributing parameters
  - SPICE-based simulations
    - *Two current models for SET generation*
    - *Voltage pulse model for SET propagation*
  - Fitting models for SET sensitivity metrics based on the sum of contributions
    - *Contribution of each parameter can be assessed*
  - Model parameters (instead of raw simulation data) are stored in LUTs
    - *Reduction in memory size and analysis time*



3. SET Characterization Methodology

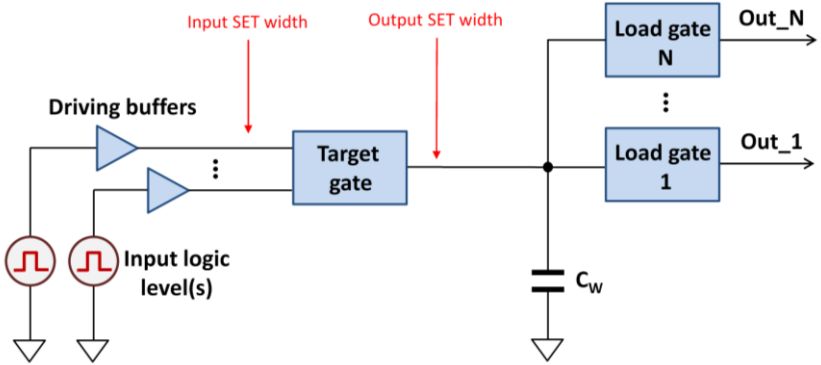
SET generation setup

- Successive injection of current pulse in sensitive nodes of a target gate
- Analysis of critical charge and generated SET pulse width



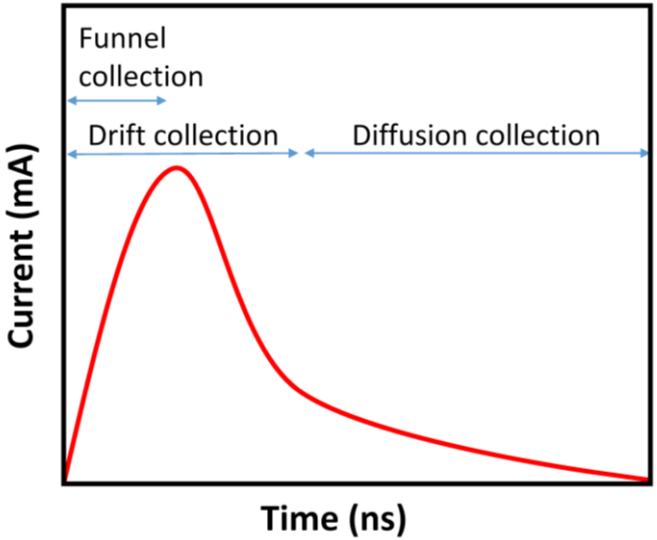
SET propagation setup

- Propagation of voltage pulse through a target gate
- Analysis of the change of pulse amplitude and width



3. SET Characterization Methodology

- **SET current models: Double-exponential current model**
  - Most widely used SET current model
  - Defined with 3 parameters: collected charge, rise time and fall time



$$I_{DEXP}(t) = \frac{Q}{\tau_{fall} - \tau_{rise}} \left(e^{\frac{-t}{\tau_{fall}}} - e^{\frac{-t}{\tau_{rise}}} \right)$$

Q = collected charge $= 1.035 \times 10^{-2} \times l \times LET$

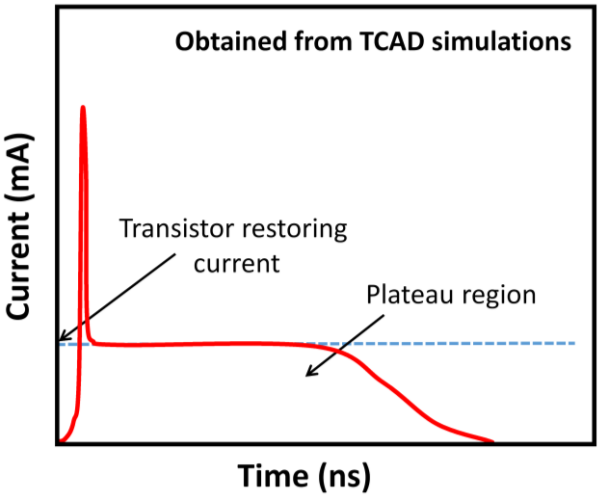
τ_{fall} = fall time of current pulse (tens of ps)

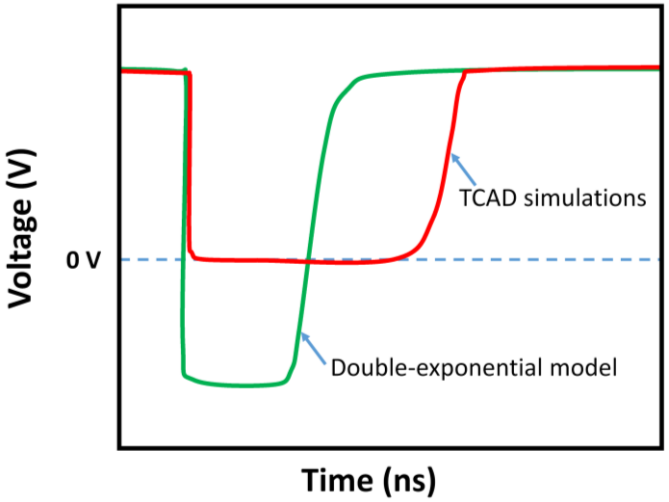
τ_{rise} = rise time of current pulse (hundreds of ps)

l = charge collection depth (several µm)

3. SET Characterization Methodology

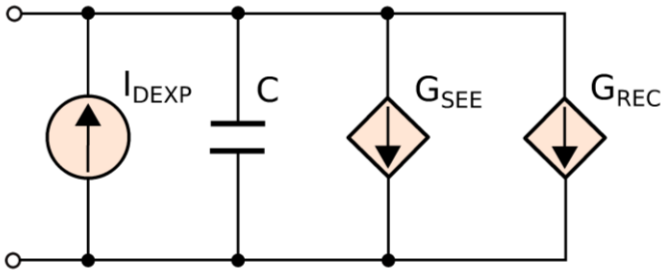
- **SET current models: Limitation of double-exponential current model**
  - Cannot reproduce current pulse with plateau, caused by high charge (LET) values
  - Overdrive effect: results in unrealistic SET voltage pulse for high charge (LET) values, exceeding supply rails





3. SET Characterization Methodology

- **SET current models: Bias-dependent current model**
  - Resolves the overdrive effect inherent in double-exponential current model
  - Good agreement with TCAD simulations
  - Composed of double-exponential current source I_{DEXP} and two voltage-dependent current sources G_{SEE} and G_{REC}



J. S. Kaupilla et al., IEEE TNS, 2009.

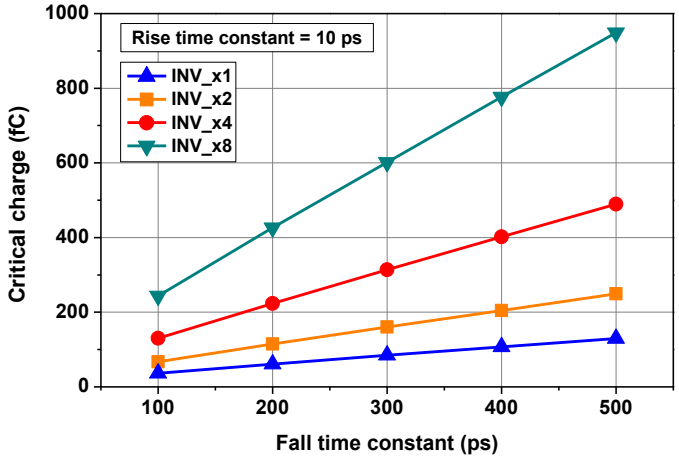
```
**********Bias Dependent SET Model**********
.subckt Bias_Dep_SET n p see_tau1=0.5e-12 see_tau2=70e-12
+ see_start_time=1e-6 see_duration=1.5e-12 see_let=40 see_col_len=1.5e-6
+ see_recomb=1E11
.param F=0.05 CS=1e-9
.param IMAX='(see_let*1.035E-2*see_col_len*1E6*1E-12)/((see_duration +
+ see_tau2 - see_tau1)-(see_tau2-see_tau1)*exp(-1*(see_duration/see_tau1)))'
.param DELAY='see_start_time+see_duration'
* IMAX from equation in Massengill 1993 IEEE NSREC Short Course
*    see_let = LET Value in MeV-cm^2/mg
*    1.035E-2 is constant to go from LET to pC/um
*    see_col_len is the collection length in meters
*    1E6 converts to micro-meters
*    1E-12 converts to Coulombs
*
* The following components represent the items in the schematic representation
*    presented in the above referenced IEEE TNS paper
CHOLD VC 0 'CS'
IEXPSEE 0 VC EXP (0 IMAX see_start_time see_tau1 DELAY see_tau2)
GRECOMB VC 0 CUR='V(VC)*CS*see_recomb'
GSEE VC 0 CUR='V(VC)*(CS/see_tau1)*(1.0/(1.0+exp((V(p)-V(n)+3*F)/F)))'
GSEEP n p CUR='V(VC)*(CS/see_tau1)*(1.0/(1.0+exp((V(p)-V(n)+3*F)/F)))'
.ends Bias_Dep_SET
```

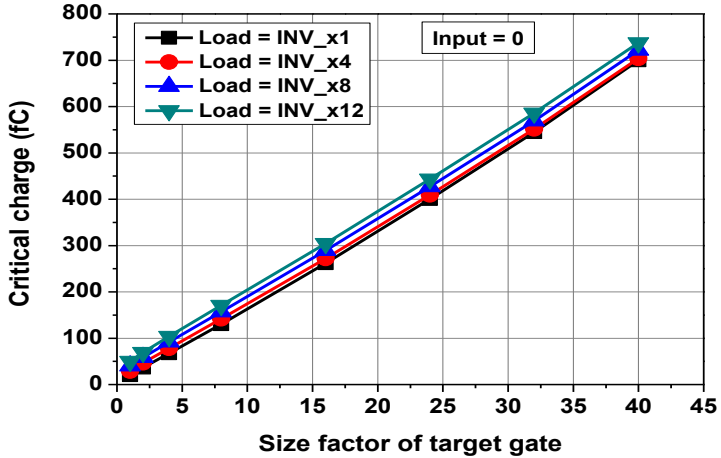
J. S. Kauppila et al., PhD Thesis, Vanderbilt University, 2015.

Outline

4. SET Characterization for 130 nm Standard Cell Library

- **Critical charge Q_{CRIT}** (for INV, input 0)
  - Q_{CRIT} is linearly proportional to timing parameters of current pulse
  - Q_{CRIT} increases (mostly linearly) with the size of target gate and load gate
    - Larger gates have higher driving strength and higher capacitance

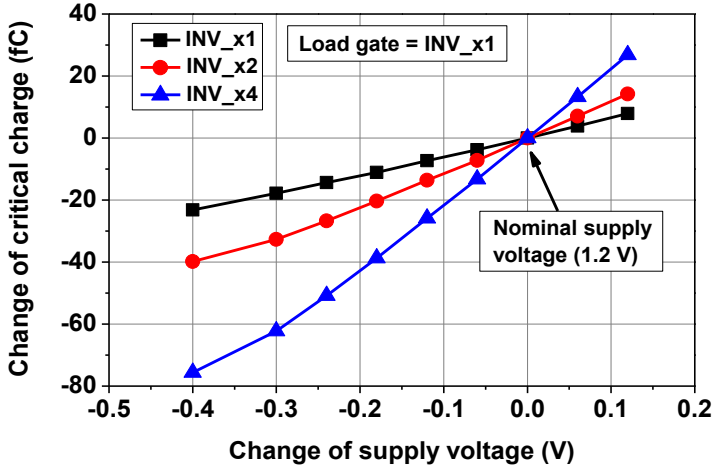


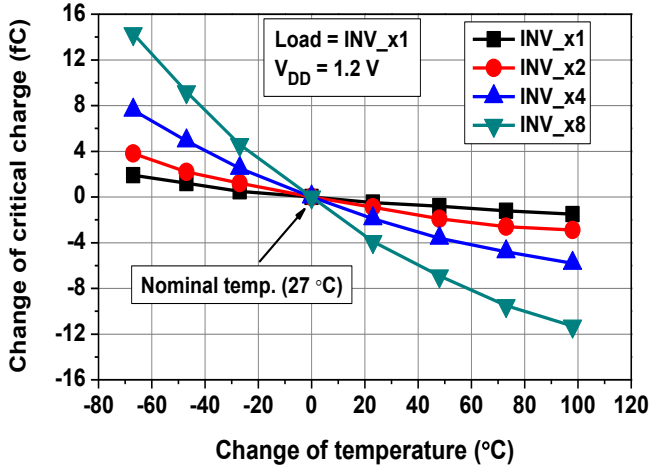


4. SET Characterization for 130 nm Standard Cell Library

- **Critical charge Q_{CRIT}** (for INV, input 0)
  - A gate is more robust to particle strikes for:
    - Higher supply voltage
    - Lower temperature

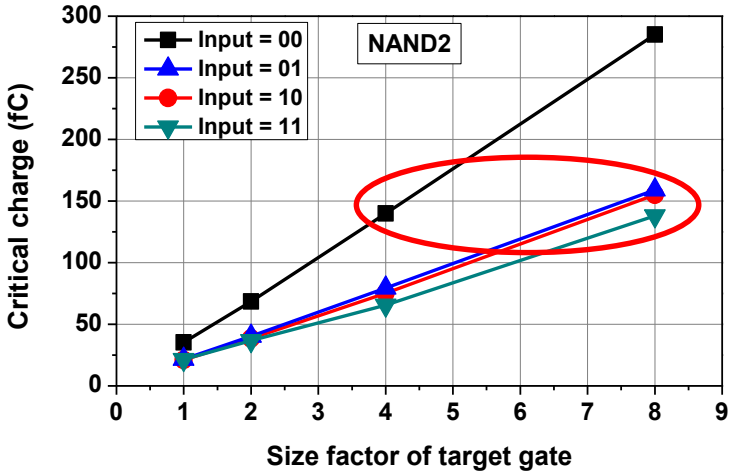
  } Driving current of restoring transistor increases





4. SET Characterization for 130 nm Standard Cell Library

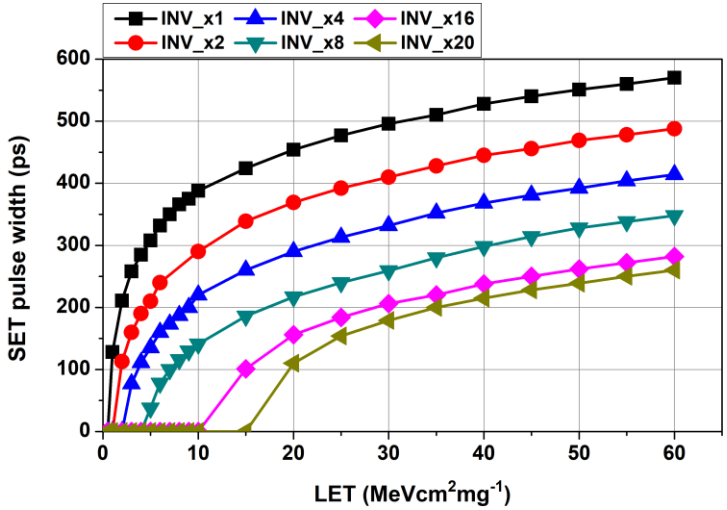
- **Critical charge** (for multi-input gates)
  - Similar qualitative trends like for INV (mostly linear dependence of Q_{CRIT} on size factor)
  - Q_{CRIT} for one input and large size factor may be similar as for lower size factor and another input
  - Q_{CRIT} values can be sorted into several groups (allows for reducing the number of simulations)

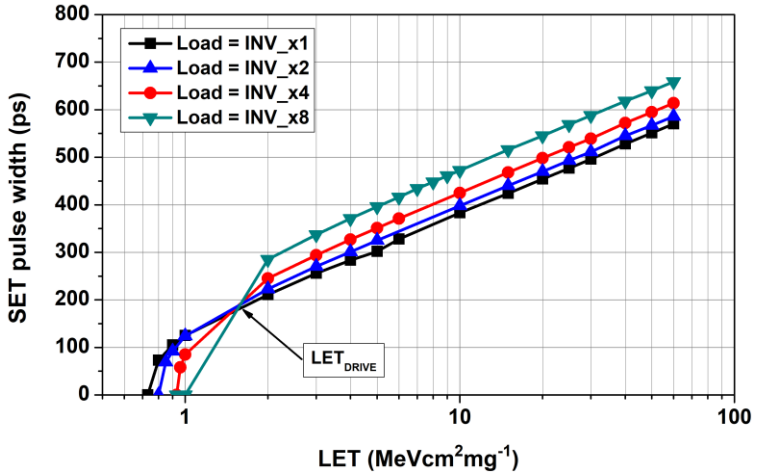


Input levels	Qcrit (fC) for NAND3		
	x0	x1	x2
000	61	111	220
001	46.2	81.2	153.3
010	46.3	80.3	152.8
011	30	49.3	87.5
100	46.9	82.4	154.6
101	31	50.3	90.3
110	31	50.3	89.8
111	26.9	39.3	63.4

4. SET Characterization for 130 nm Standard Cell Library

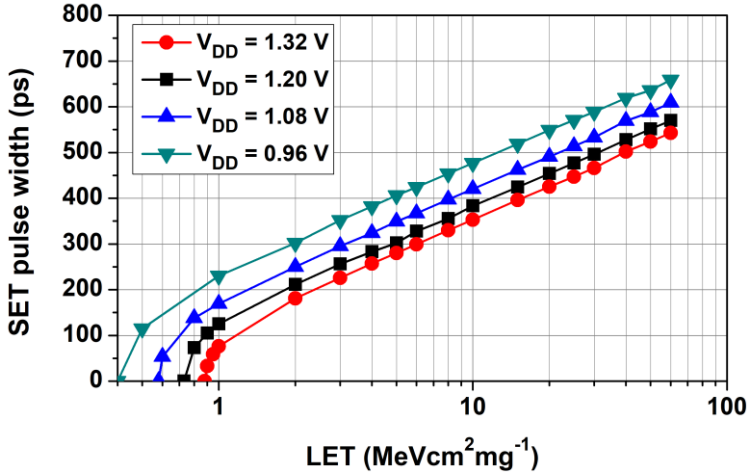
- **Generated SET pulse width** (for INV, input 0)
  - SET pulse width increases with LET (amount of deposited charge)
  - Increase of gate size reduces the SET pulse width
  - Large load increases the SET pulse width for higher LET

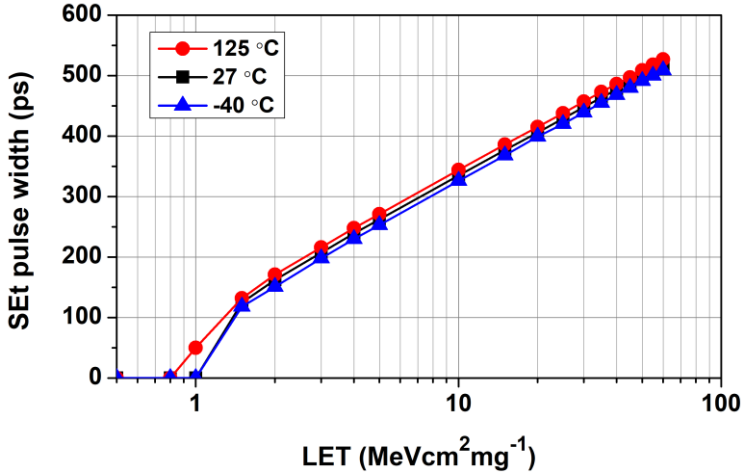




4. SET Characterization for 130 nm Standard Cell Library

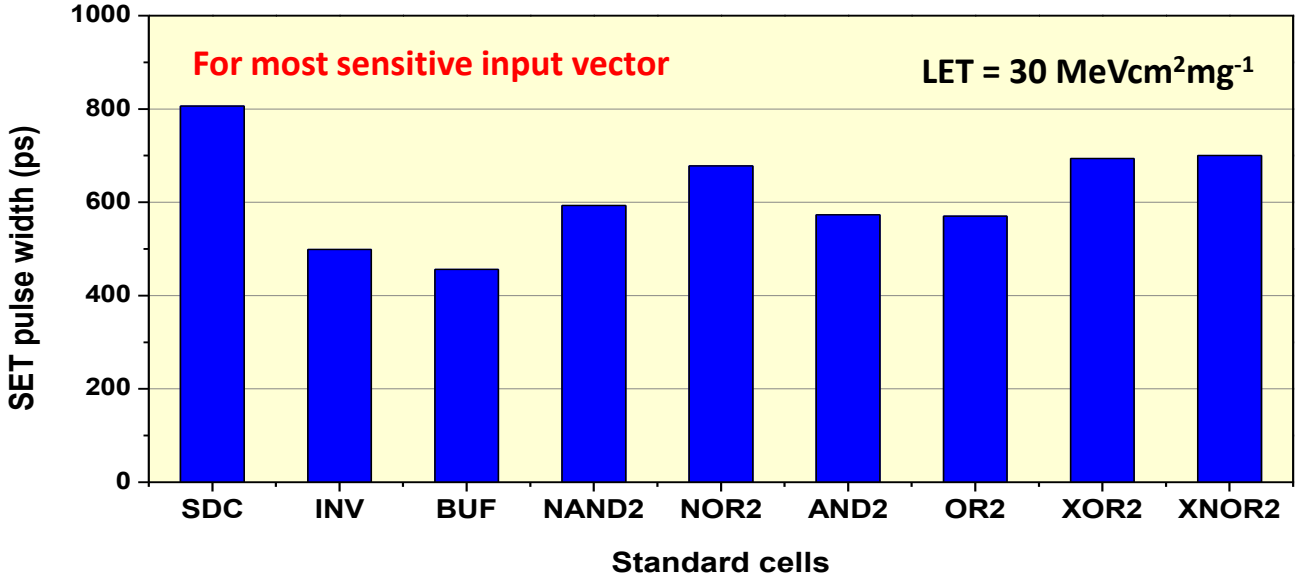
- **Generated SET pulse width** (for INV, input 0)
  - T_{EMP} decrease leads to a decrease of SET pulse width
  - V_{DD} increase leads to a decrease of SET pulse width





4. SET Characterization for 130 nm Standard Cell Library

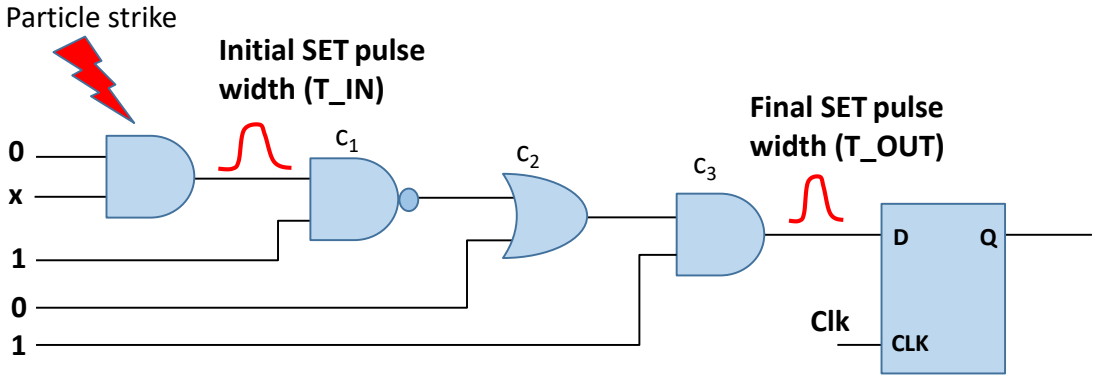
- **Generated SET pulse width - comparison**
  - SET pulse width may vary by at least 2 times depending on gate type
  - Standard delay cells (SDC) based on skew-sized transistors are most sensitive to SETs



4. SET Characterization for 130 nm Standard Cell Library

SET pulse propagation

- An SET will propagate through a gate only if its width is larger than the propagation delay
- An SET will generate a soft error only if its width is larger than the sum of setup and hold times of flip-flop

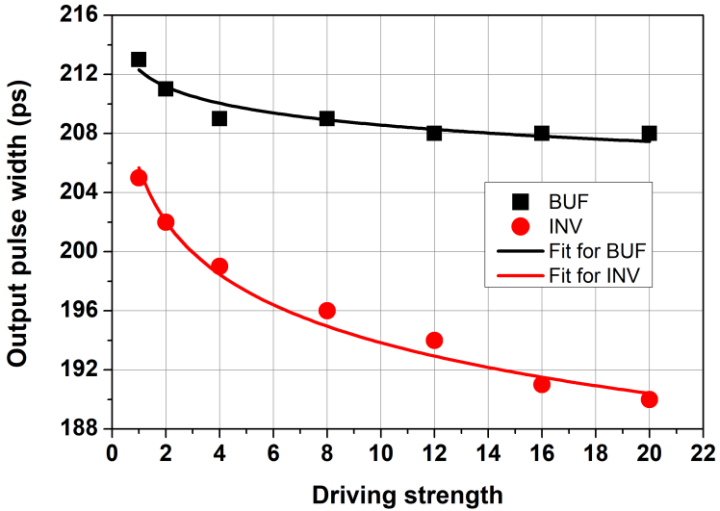


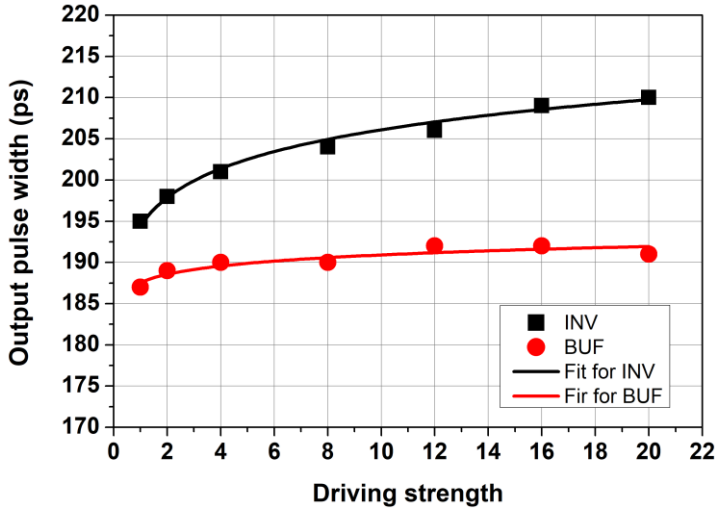
$$T\_OUT = T\_IN + c_1 + c_2 + c_3$$

c_1, c_2 and c_3 denote the impact of each gate on SET propagation

4. SET Characterization for 130 nm Standard Cell Library

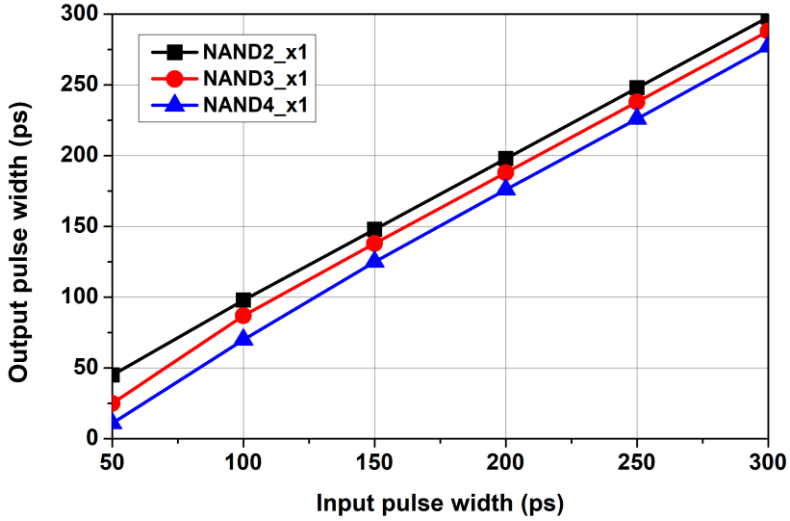
- **SET pulse propagation (through individual cells)**
  - Each cell broadends a pulse with one polarity, and shrinks a pulse with opposite polarity
  - Driving strength influences the pulse broadening/shrinking

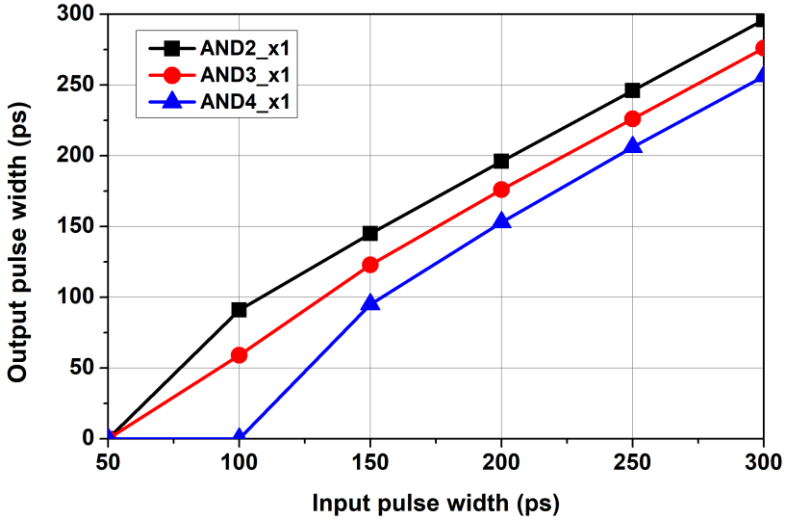




4. SET Characterization for 130 nm Standard Cell Library

- **SET pulse propagation (through individual cells)**
  - More complex gates and gates with more inputs are better SET suppressors





4. SET Characterization for 130 nm Standard Cell Library

- **SET pulse propagation (through combinational paths)**
  - Significant pulse broadening may occur accross very short non-inverting paths
  - Supply voltage and temperature corners may significantly contribute to pulse broadening

10-gate combinational paths (all gates are with x1 size)	Output pulse width (ps)					
	Positive input pulse = 200 ps			Negative input pulse = 200 ps		
	LVT	TVT	HVT	LVT	TVT	HVT
INV	208	206	204	195	196	197
BUF	367	322	293	0	68	108
NAND2	201	201	201	203	204	204
AND2	166	152	134	237	250	268
NOR2	223	216	214	151	176	185
OR2	925	748	645	0	0	0
Alternating OR2 and AND2	542	447	387	0	0	0
Alternating AND3 and OR4	499	416	359	0	0	0
Alternating NAND2 and NOR3	667	563	506	0	0	0
Alternating XNOR3 and NOR2	0	0	0	173	243	252

Outline

5. SET Sensitivity Models and SET Database

- **By fitting the simulation results, predictive SET sensitivity models can be expressed as a sum of contributing functions**

$$\text{SET\_metric} = \text{SET\_metric\_nominal} + \sum_{i=1}^{N} f_i \cdot (K_i - K_{iNOM})$$

f_i = fitting function
K_i = contributing parameter (e.g. size factor)

Critical charge model (8 fitting parameters per cell)

$$Q_{CRIT} = Q_{NOM} + f(S_T) + f(S_L) + f(C_L) + f(V_{DD}) + f(T_{EMP}) + f_{ERROR}$$

Generated SET pulse width model (12 fitting parameters per cell)

$$T_{SET} = f(LET, S_T = 1) + f(S_T = n) + f(S_L, C_L) + f(V_{DD}) + f(T_{EMP})$$

Propagated SET pulse width model (7 fitting parameters per cell)

$$T_{OUT} = T_{IN} \pm \Delta\tau = T_{IN} \pm c_0 \pm f(S_T) \pm f(C_L) \pm f(V_{DD}) \pm f(T_{EMP})$$

Average relative error for each model (with respect to SPICE) is less than 5 %

5. SET Sensitivity Models and SET Database

Optimization of simulations and SET sensitivity database

- Due to similar SET sensitivity for multiple inputs, the number of simulations for SET generation can be reduced by almost 48 %
- By storing the model parameters in LUTs instead of simulation results, the number of stored values is reduced by 2 orders of magnitude

Standard SET sensitivity database

LUT4	Q_{CRIT} (S_T, S_L) for V_{DD4}			
LUT3	Q_{CRIT} (S_T, S_L) for V_{DD3}			
LUT2	Q_{CRIT} (S_T, S_L) for V_{DD2}			
LUT1	Q_{CRIT} (S_T, S_L) for V_{DD1}			
	S_L=1	S_L=2	S_L=4	S_L=8
S_T=1	Q_{CRIT}(1,1)	Q_{CRIT}(1,2)	Q_{CRIT}(1,4)	Q_{CRIT}(1,8)
S_T=2	Q_{CRIT}(2,1)	Q_{CRIT}(2,2)	Q_{CRIT}(2,4)	Q_{CRIT}(2,8)
S_T=4	Q_{CRIT}(4,1)	Q_{CRIT}(4,2)	Q_{CRIT}(4,4)	Q_{CRIT}(4,8)
S_T=8	Q_{CRIT}(8,1)	Q_{CRIT}(8,2)	Q_{CRIT}(8,4)	Q_{CRIT}(8,8)

Model-based SET sensitivity database

Critical charge model LUT				
	Input 1	Input 2	...	Input 2^P - L
Q_{NOM}	$Q_{NOM}(1)$	$Q_{NOM}(2)$	...	$Q_{NOM}(2^P\text{-}L)$
a_0	$a_0(1)$	$a_0(2)$	...	$a_0(2^P\text{-}L)$
a_1	$a_1(1)$	$a_1(2)$	...	$a_1(2^P\text{-}L)$
a_2	$a_2(1)$	$a_2(2)$	...	$a_2(2^P\text{-}L)$
a_3	$a_3(1)$	$a_3(2)$	...	$a_3(2^P\text{-}L)$
a_4	$a_4(1)$	$a_4(2)$	...	$a_4(2^P\text{-}L)$
a_5	$a_5(1)$	$a_5(2)$	...	$a_5(2^P\text{-}L)$
a_6	$a_6(1)$	$a_6(2)$	...	$a_6(2^P\text{-}L)$

5. SET Sensitivity Models and SET Database

- **SET sensitivity of each gate type can be represented with 3 look-up tables**
  - Critical charge LUT
  - Generated SET pulse width LUT
  - Propagated SET pulse width LUT

Critical charge model LUT				
	Input 1	Input 2	...	Input 2^P - L
Q_{NOM}	$Q_{NOM}(1)$	$Q_{NOM}(2)$	...	$Q_{NOM}(2^P\text{-}L)$
a_0	$a_0(1)$	$a_0(2)$	...	$a_0(2^P\text{-}L)$
a_1	$a_1(1)$	$a_1(2)$	...	$a_1(2^P\text{-}L)$
a_2	$a_2(1)$	$a_2(2)$	...	$a_2(2^P\text{-}L)$
a_3	$a_3(1)$	$a_3(2)$	...	$a_3(2^P\text{-}L)$
a_4	$a_4(1)$	$a_4(2)$	...	$a_4(2^P\text{-}L)$
a_5	$a_5(1)$	$a_5(2)$	...	$a_5(2^P\text{-}L)$
a_6	$a_6(1)$	$a_6(2)$	...	$a_6(2^P\text{-}L)$

Generated SET pulse width model LUT				
	Input 1	Input 2	...	Input 2^P - L
LET_{DRIVE}	$LET_{DRIVE}(1)$	$LET_{DRIVE}(2)$	...	$LET_{DRIVE}(2^P - L)$
b_0	$b_0(1)$	$b_0(2)$	...	$b_0(2^P - L)$
b_1	$b_1(1)$	$b_1(2)$	...	$b_1(2^P - L)$
b_2	$b_2(1)$	$b_2(2)$	...	$b_2(2^P - L)$
b_3	$b_3(1)$	$b_3(2)$	...	$b_3(2^P - L)$
b_4	$b_4(1)$	$b_4(2)$	...	$b_4(2^P - L)$
b_5	$b_5(1)$	$b_5(2)$	...	$b_5(2^P - L)$
b_6	$b_6(1)$	$b_6(2)$	...	$b_6(2^P - L)$
b_7	$b_7(1)$	$b_7(2)$	...	$b_7(2^P - L)$
b_8	$b_8(1)$	$b_8(2)$	...	$b_8(2^P - L)$
b_9	$b_9(1)$	$b_9(2)$	...	$b_9(2^P - L)$

Propagated SET pulse width model LUT				
	Input 1	Input 2	...	Input P
c_0	$c_0(1)$	$c_0(2)$	...	$c_0(P)$
c_1	$c_1(1)$	$c_1(2)$	...	$c_1(P)$
c_2	$c_2(1)$	$c_2(2)$	...	$c_2(P)$
c_3	$c_3(1)$	$c_3(2)$	...	$c_3(P)$
c_4	$c_4(1)$	$c_4(2)$	...	$c_4(P)$
c_5	$c_5(1)$	$c_5(2)$	...	$c_5(P)$
c_6	$c_6(1)$	$c_6(2)$	...	$c_6(P)$

Outline

6. Conclusions

- **Characterization of SET effects in standard cells is initial step in the rad-hard design**
- **SET sensitivity of a logic gate in a given technology is strongly influenced by a combined impact of design, operating and irradiation parameters**
- **SET models are essential for simplifying the SER computation for a target circuit**
- **Major contributions:**
  - Joint characterization of standard cells and their hardened variants
  - SET sensitivity models considering explicitly the parameters relevant for the design process, with the possibility to identify the impact of each parameter
  - Reduction of number of simulations and SET database
- **Future work:**
  - Further improvement of SET models by considering additional parameters and effects
  - Inclusion of SET models in a reliability-aware design flow

Thank you for your attention!

Marko Andjelkovic

IHP – Innovations for High Performance Microelectronics
Im Technologiepark 25
15236 Frankfurt (Oder)
Germany
Phone: +49 (0) 335 5625 527
Fax: +49 (0) 335 5625 413
Email: andjelkovic@ihp-microelectronics.com

https://elicsir.elfak.rs/

innovations for high performance microelectronics

Leibniz Association

www.ihp-microelectronics.com

A10