RADFET: Wafer to Finished Product

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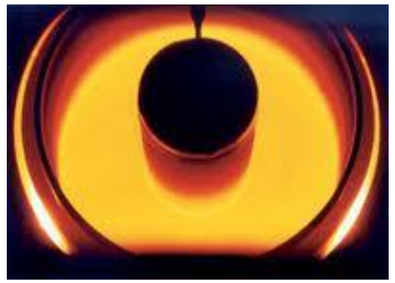
elicsir
UNIVERSITY OF NIS FACULTY OF ELECTRONIC ENGINEERING
Tyndall National Institute Institiúid Náisiúnta
ihp innovations for high performance microelectronics
UNIVERSITAS GRANATENSIS 1531 UNIVERSIDAD DE GRANADA

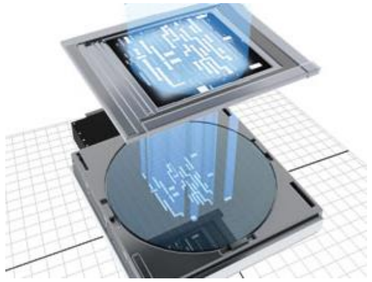
SAND to RADFET

Silicon

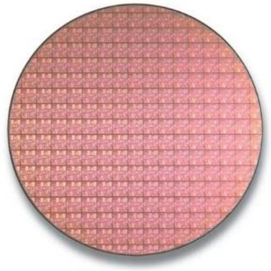


Purified into ingot

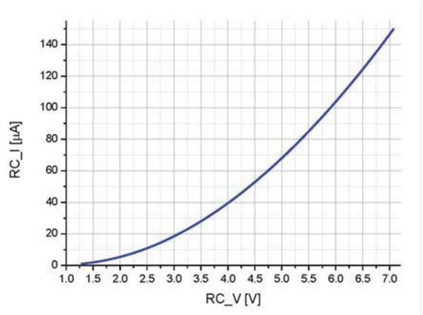
Ingot sawn into 100mm wafers



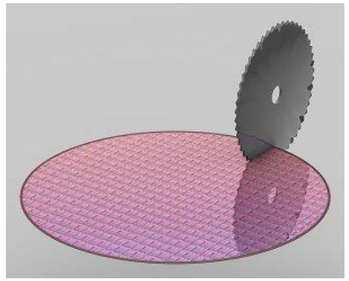
Tyndall Fabrication Facility



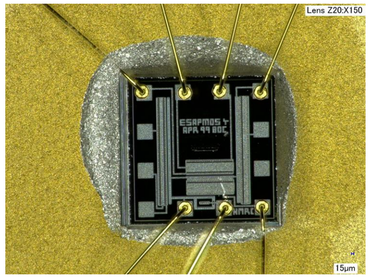
Completed wafer with many RADFET die



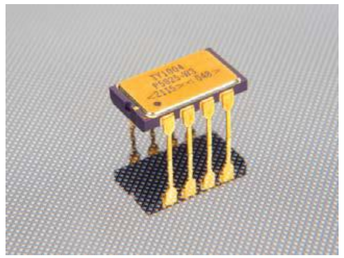
Wafer Electrical Testing



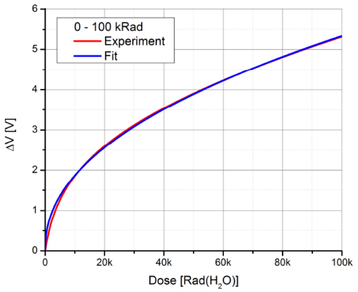
Wafer Dicing into die



Wire Bonding

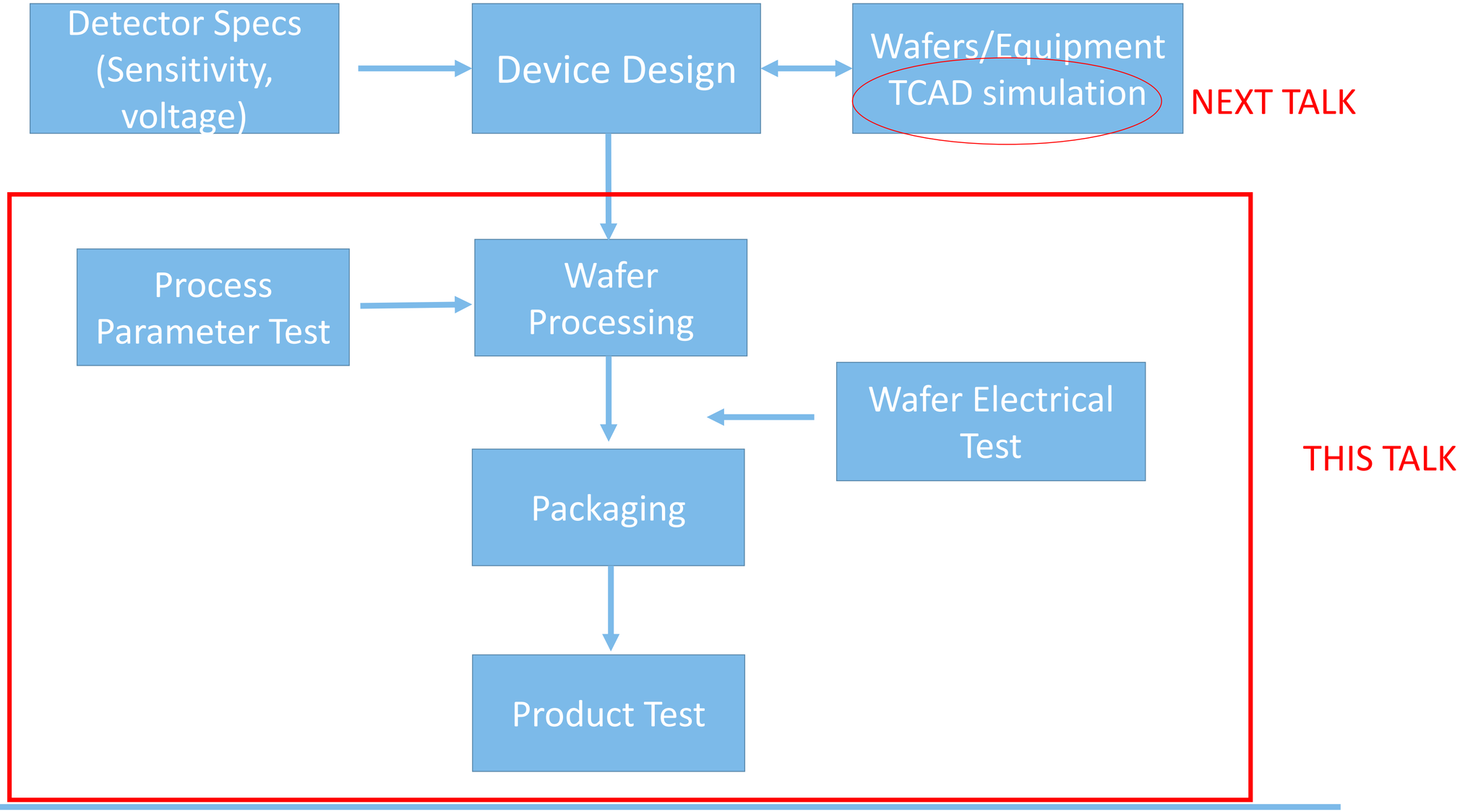


Packaged RADFET

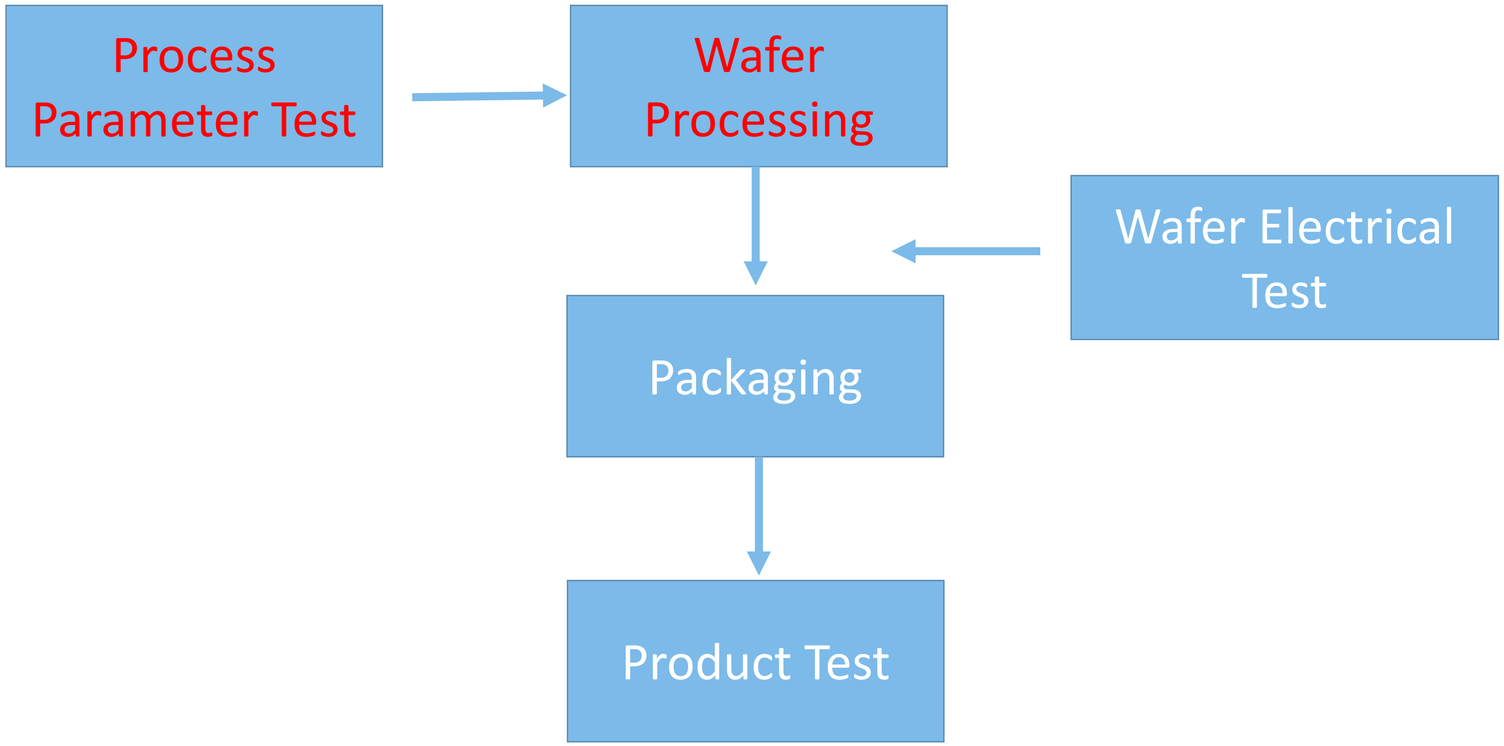


Product Test

Detector Fabrication



Outline


Process Parameter Test
Wafer Processing
Wafer Electrical Test
Packaging
Product Test

Tyndall Fabrication Facilities

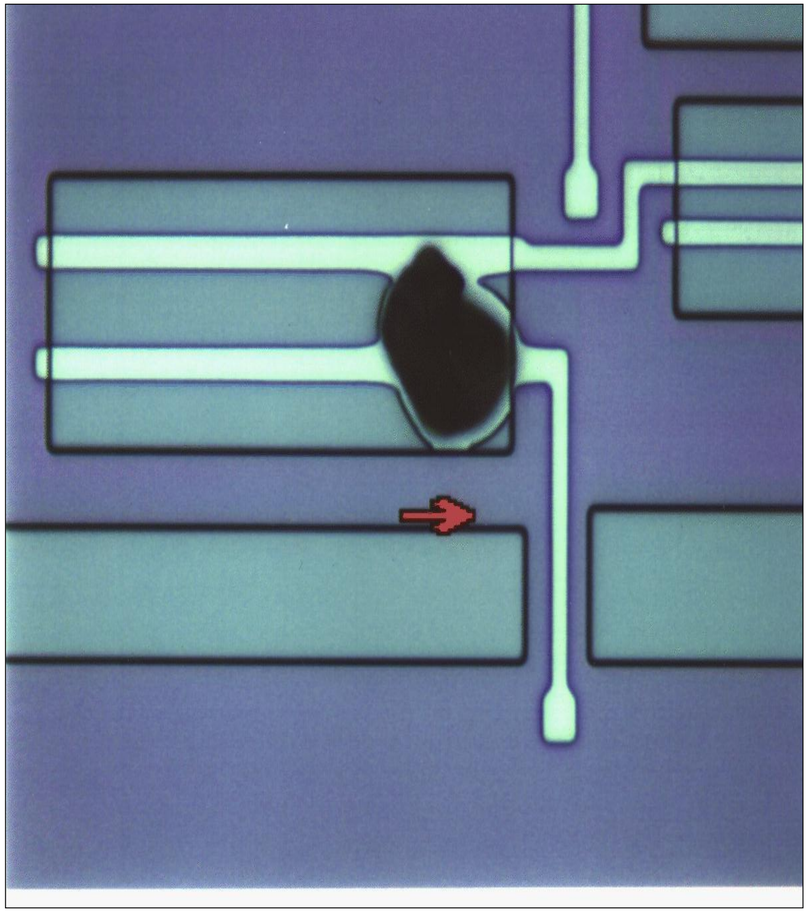
- Wafer diameters from 50mm to 200mm
- Range of fabrication clean-rooms for different applications
  - Class 1000 (ISO 6) or lower

ISO 14644-1 Cleanroom Standards

www.portafab.com/cleanrooms.html

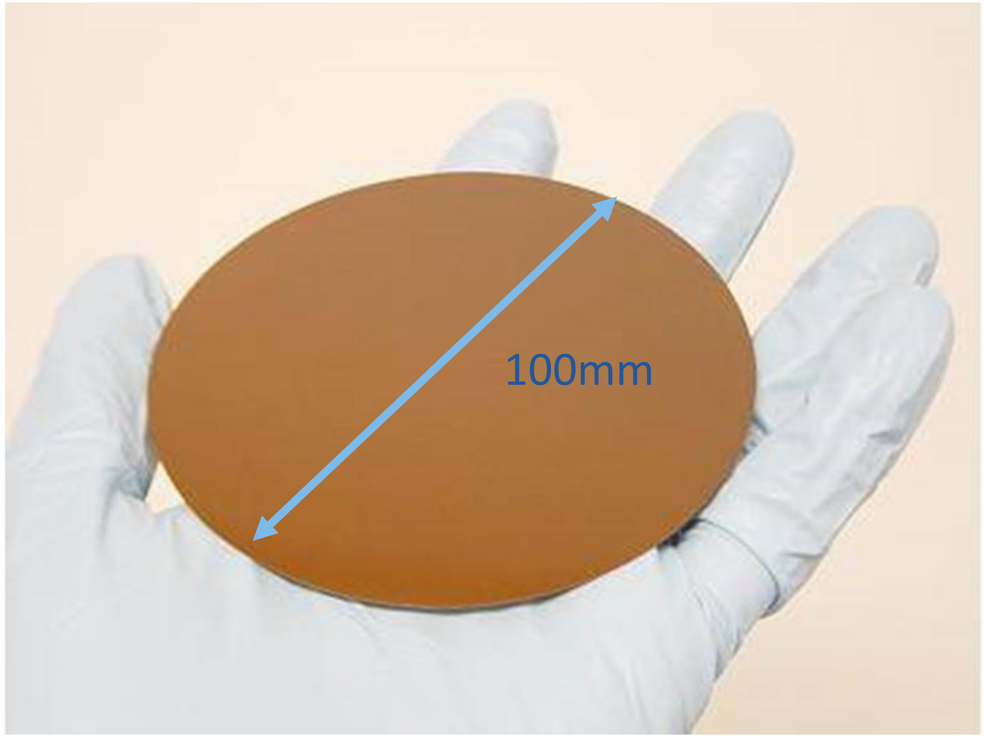
Class	maximum particles/m³						FED STD 209E equivalent
	≥0.1 µm	≥0.2 µm	≥0.3 µm	≥0.5 µm	≥1 µm	≥5 µm	
ISO 1	10	2.37	1.02	0.35	0.083	0.0029	
ISO 2	100	23.7	10.2	3.5	0.83	0.029	
ISO 3	1,000	237	102	35	8.3	0.29	Class 1
ISO 4	10,000	2,370	1,020	352	83	2.9	Class 10
ISO 5	100,000	23,700	10,200	3,520	832	29	Class 100
ISO 6	1.0×10^{6}	237,000	102,000	35,200	8,320	293	Class 1,000
ISO 7	1.0×10^{7}	2.37×10^{6}	1,020,000	352,000	83,200	2,930	Class 10,000
ISO 8	1.0×10^{8}	2.37×10^{7}	1.02×10^{7}	3,520,000	832,000	29,300	Class 100,000
ISO 9	1.0×10^{9}	2.37×10^{8}	1.02×10^{8}	35,200,000	8,320,000	293,000	Room air

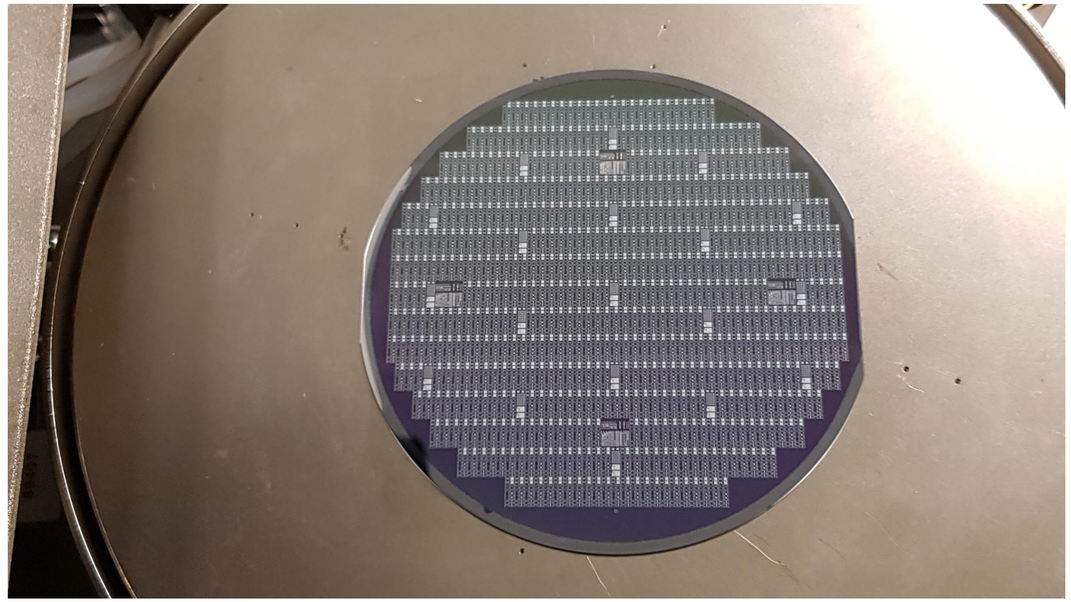
Cleanliness important



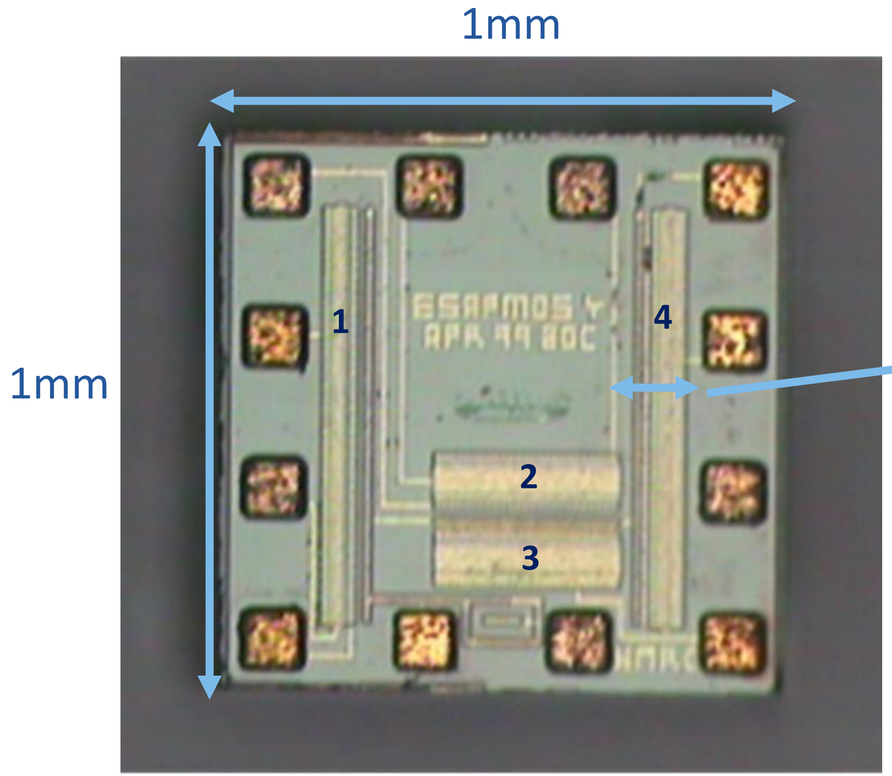
Particle causing a Metal Short

100mm RADFET Wafer

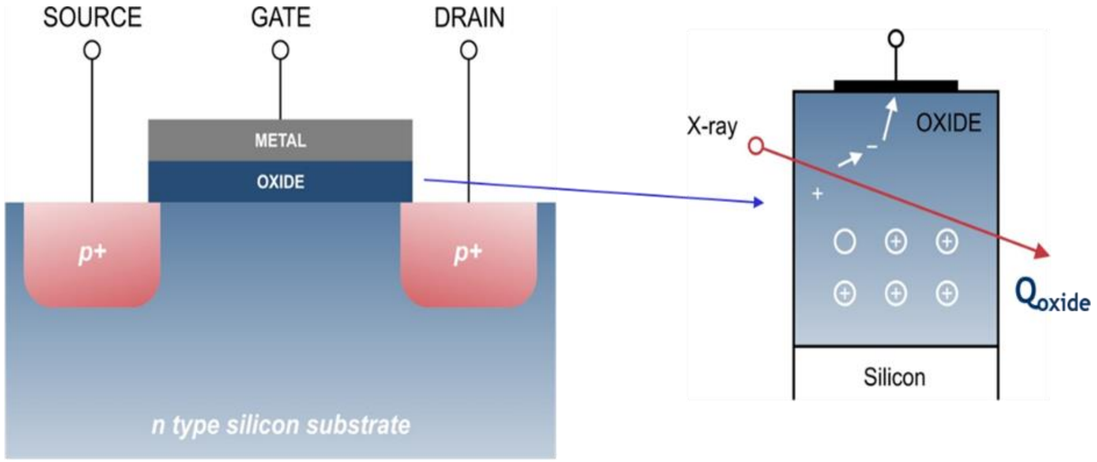




RADFET transistor Cross-Section

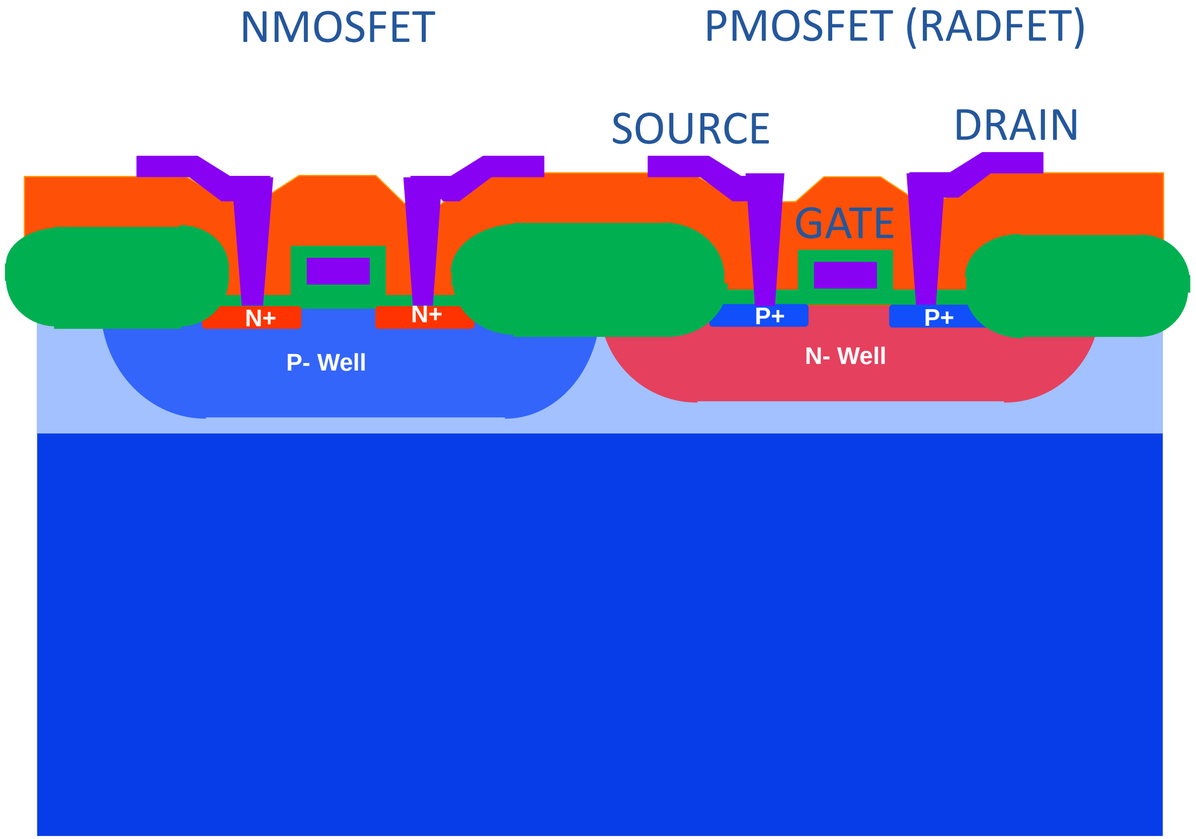


RADFET Die Design



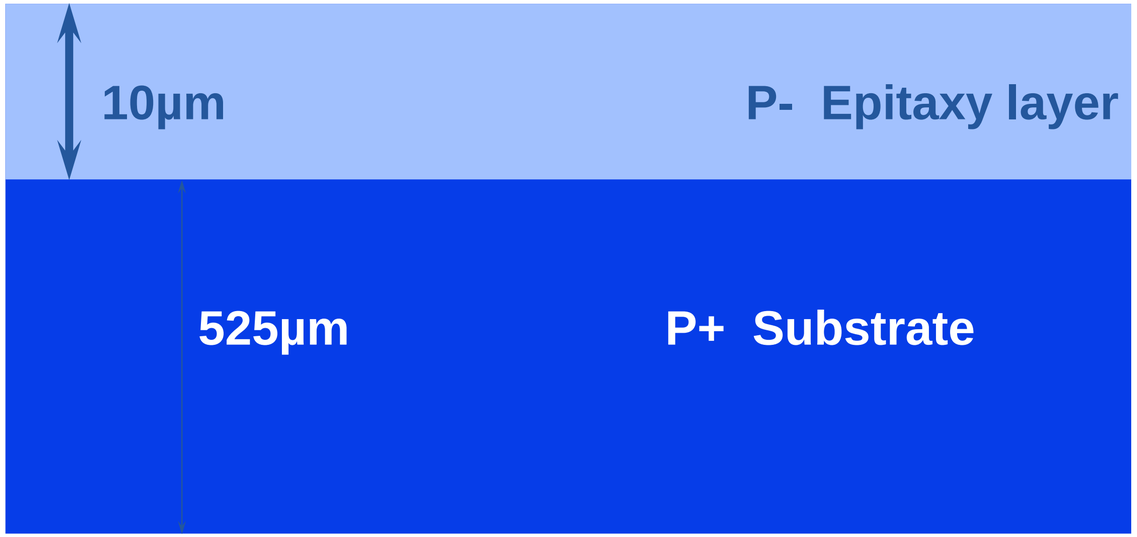
Sensitivity: $\Delta V_{threshold} = Q_{oxide}/C_{sensor}$

CMOS transistor Cross-Section

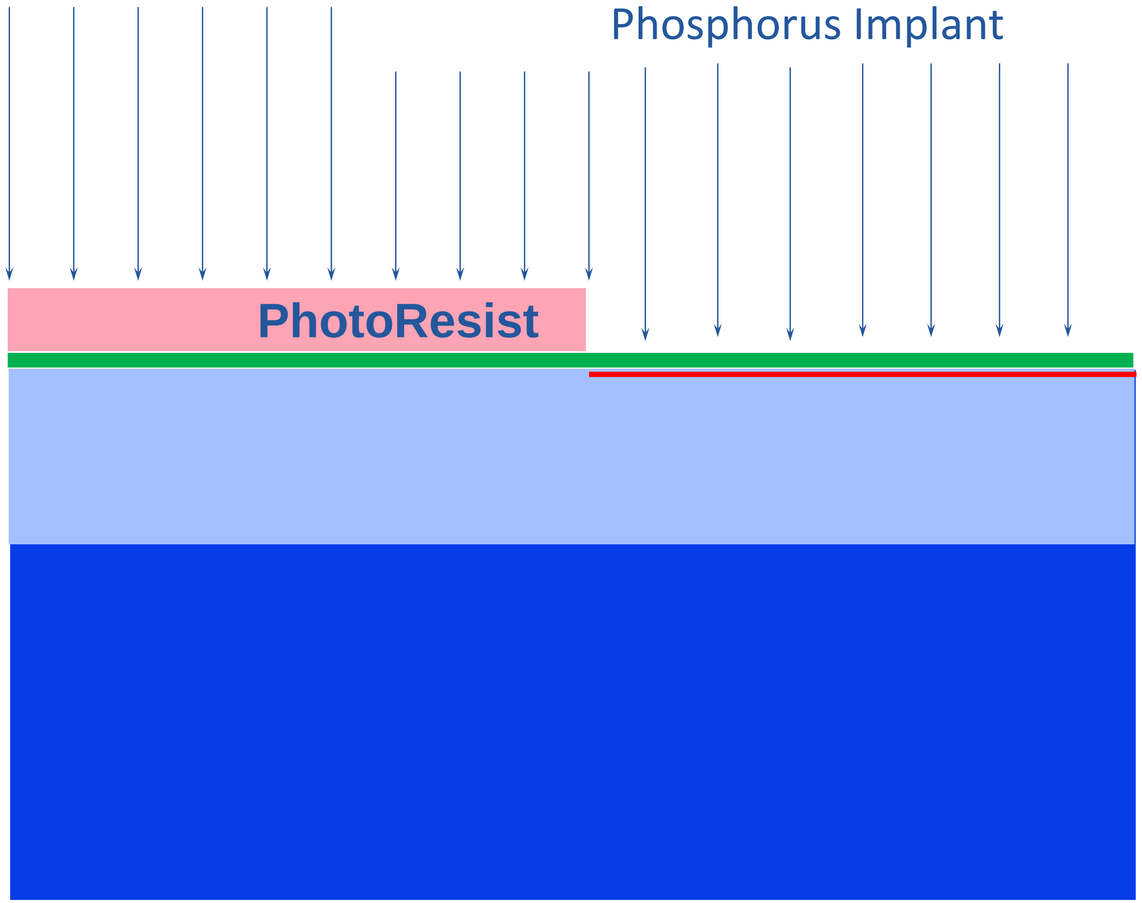


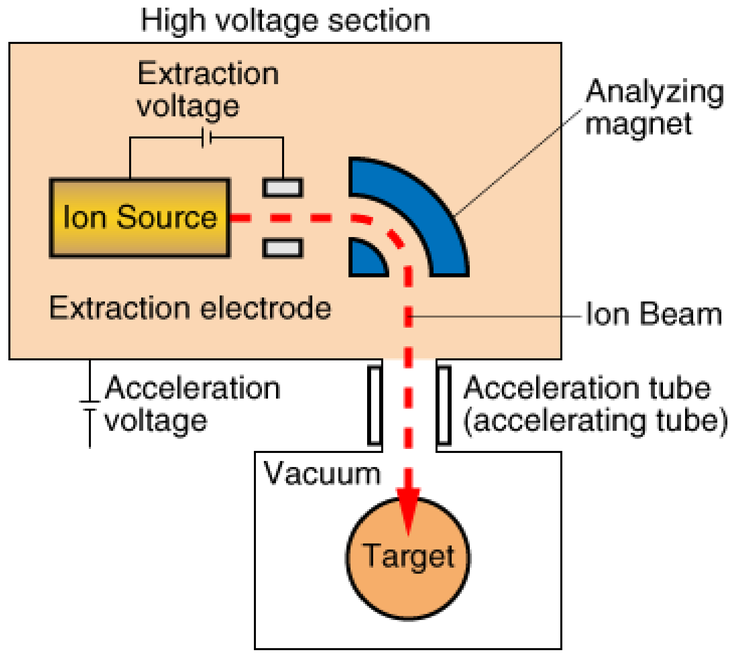
- Integrate RADFET in our CMOS line
- More than 100 process steps

Silicon Wafer



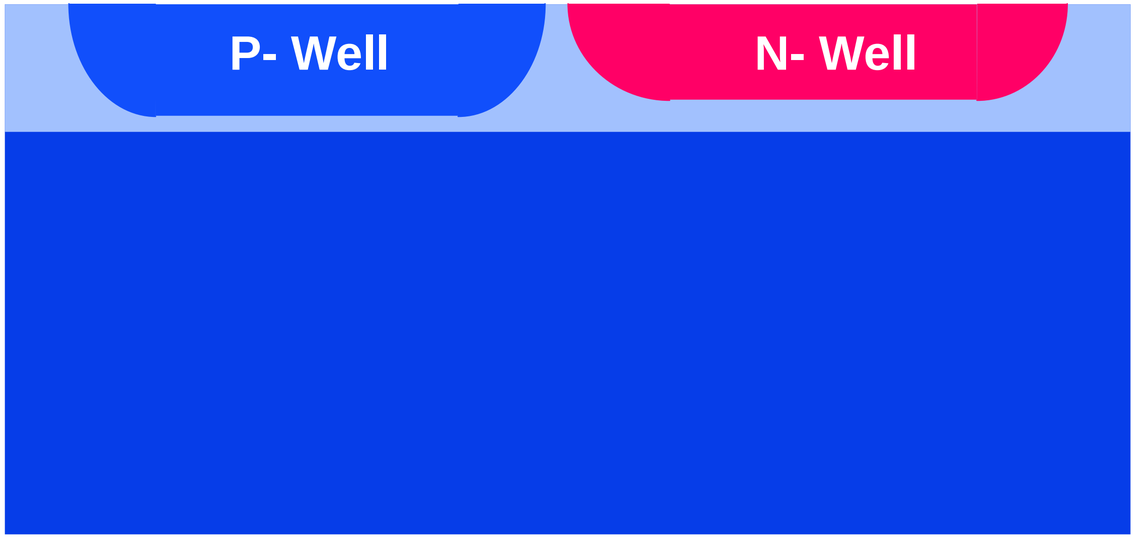
NWell Mask and Implant

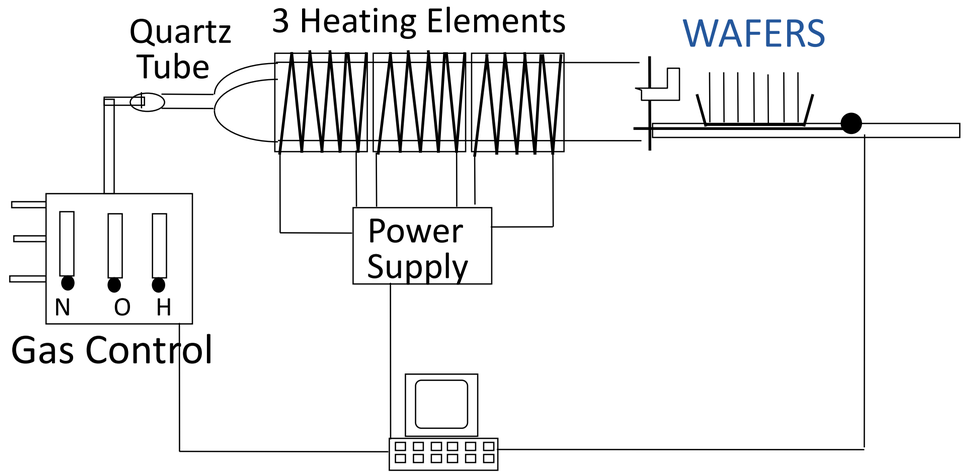




- Ion Dose: 4e12/cm^2
- Ion Energy: 170keV

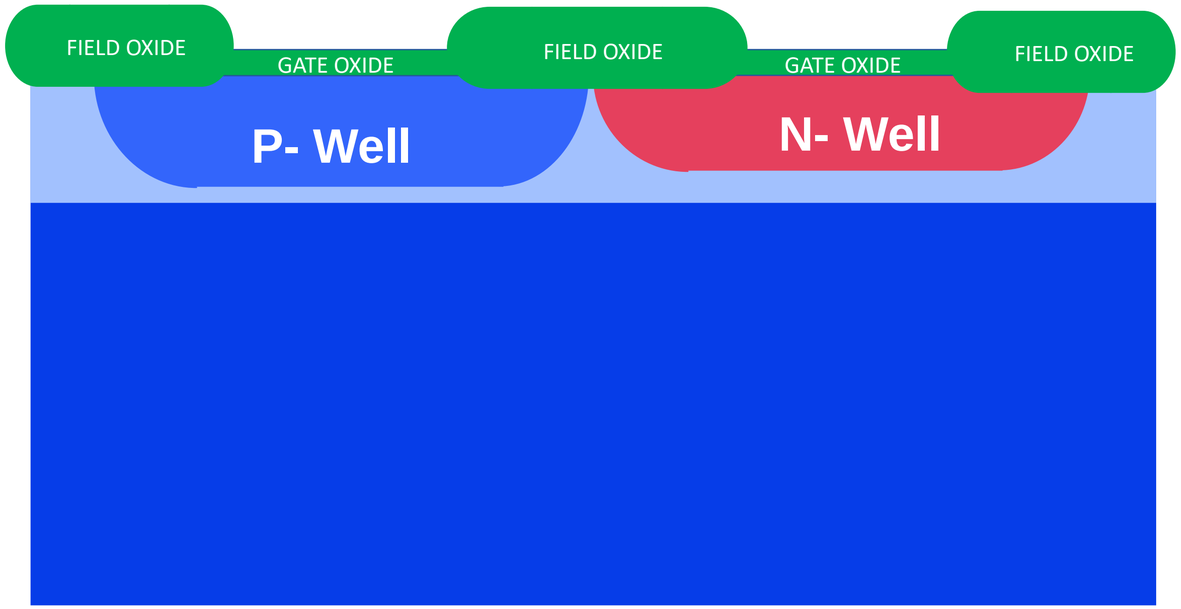
Well Drive-in





- Furnace Temperature: 1100^{o}C
- Time: 22 Hours in N_2 ambient

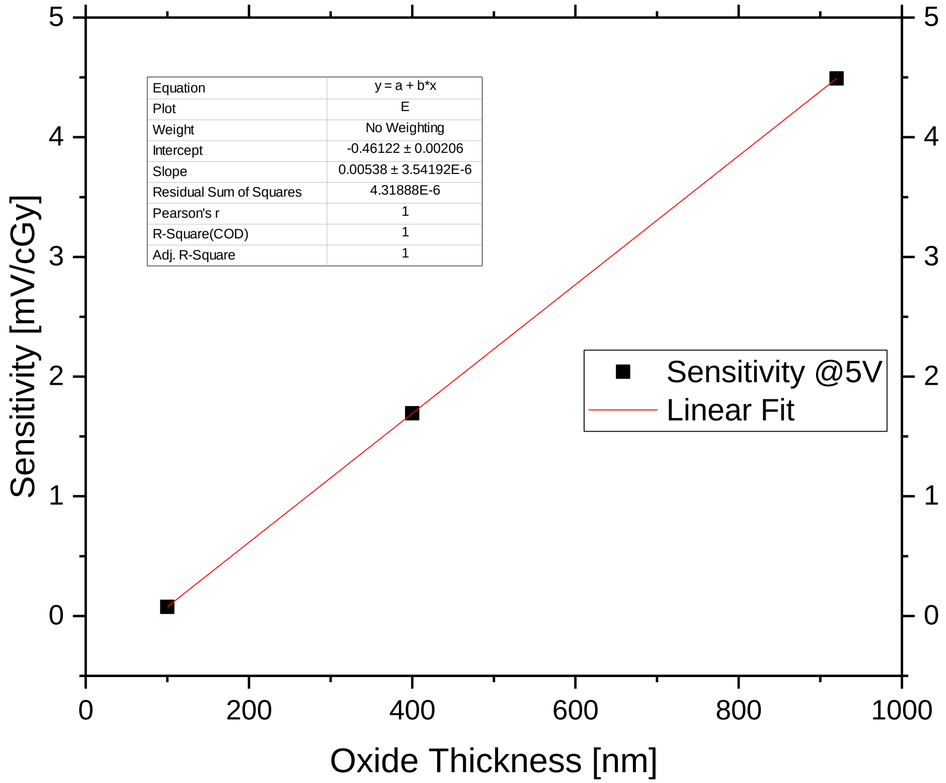
Gate Oxidation

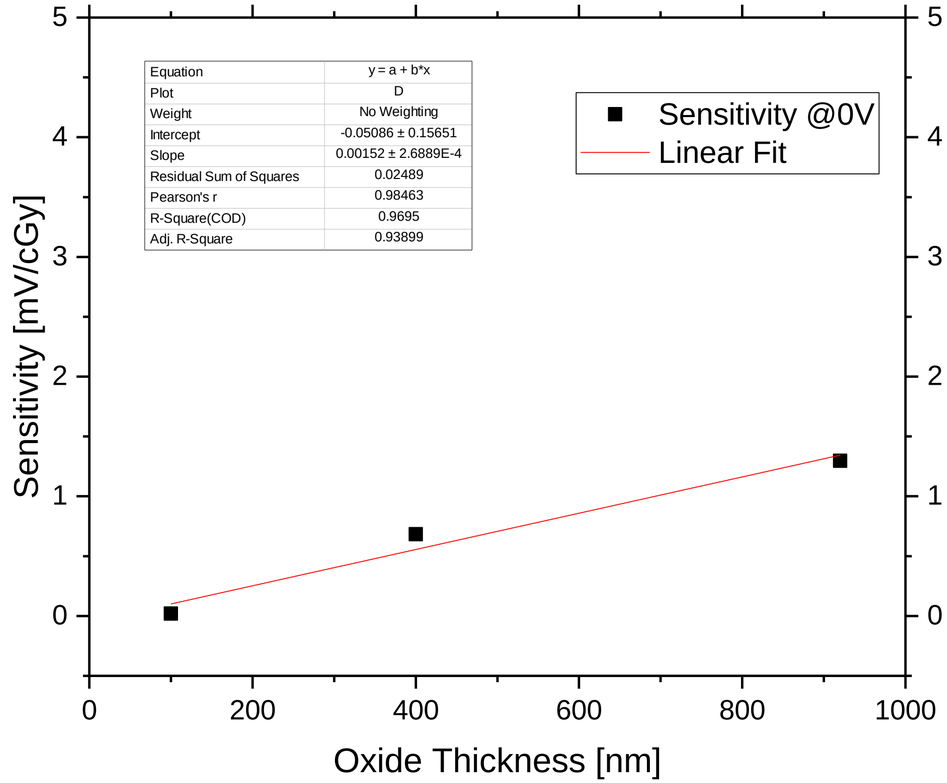


- 100nm, 400nm, 1μm thicknesses
- Grown in Furnace at high temperatures in an oxygen environment

$$Si + O_2 = SiO_2$$

Sensitivity vs Oxide Thickness



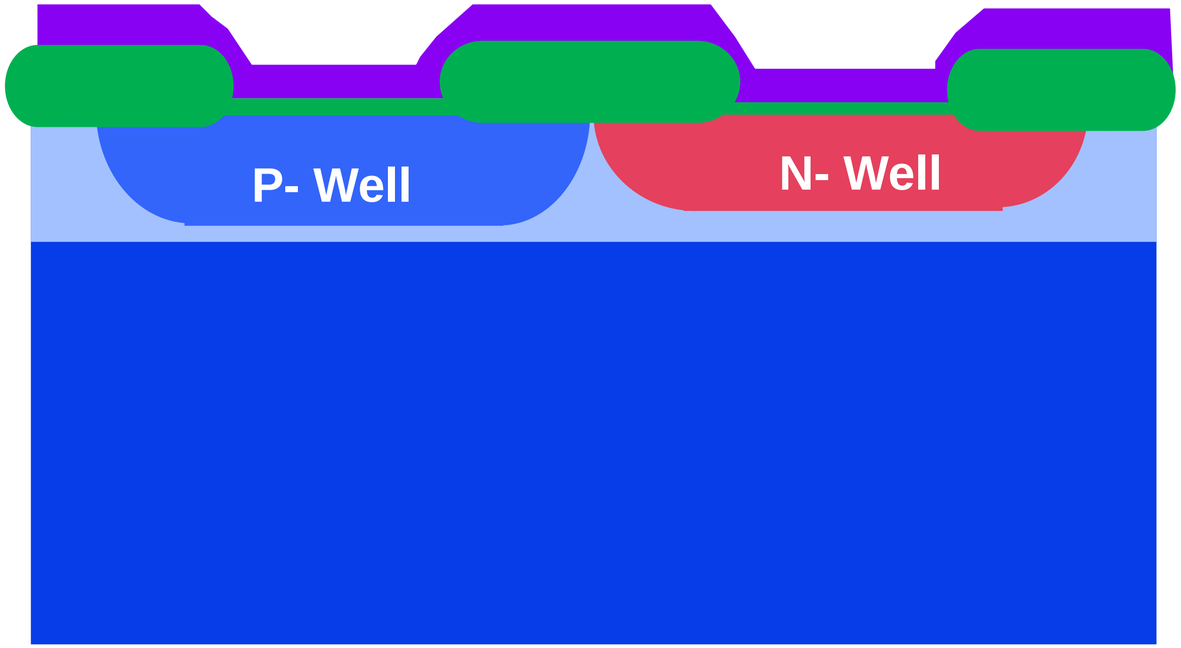


Measurement of Gate Oxide

NanoSpec Optical Measurement Tool

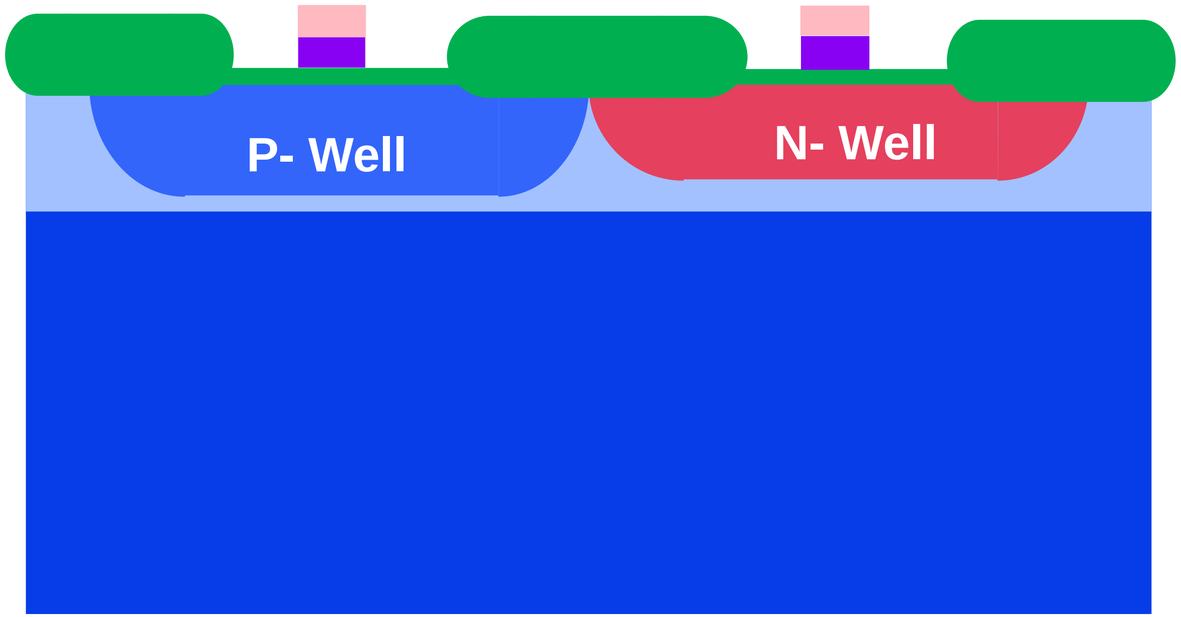
Design	400nm
Specification	400 ± 20 nm
Measured (13 points)	394 ± 5 nm

Polysilicon Gate Deposition



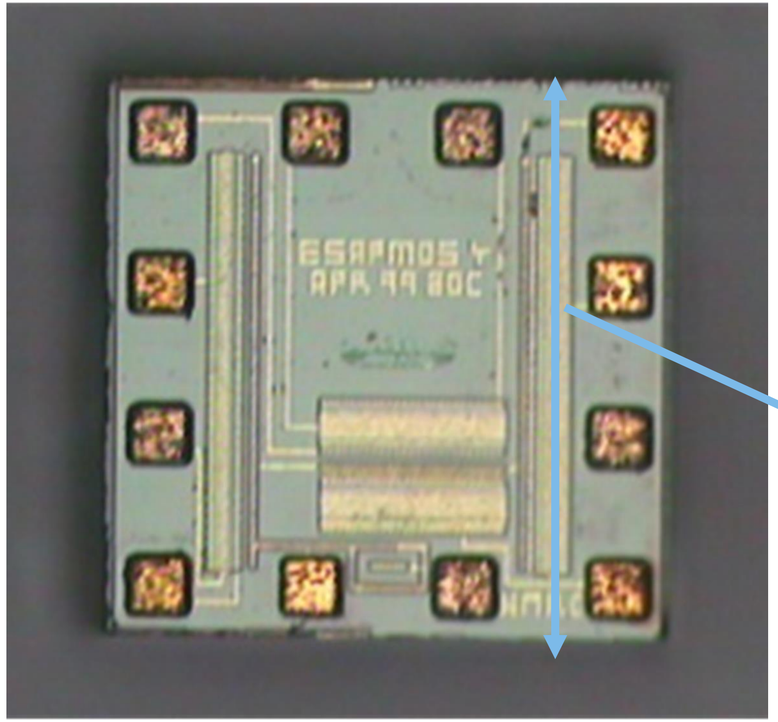
- Chemical Vapour Deposition
- 450nm Polysilicon
- Temperature: 620^{o}C
- Time: 50min

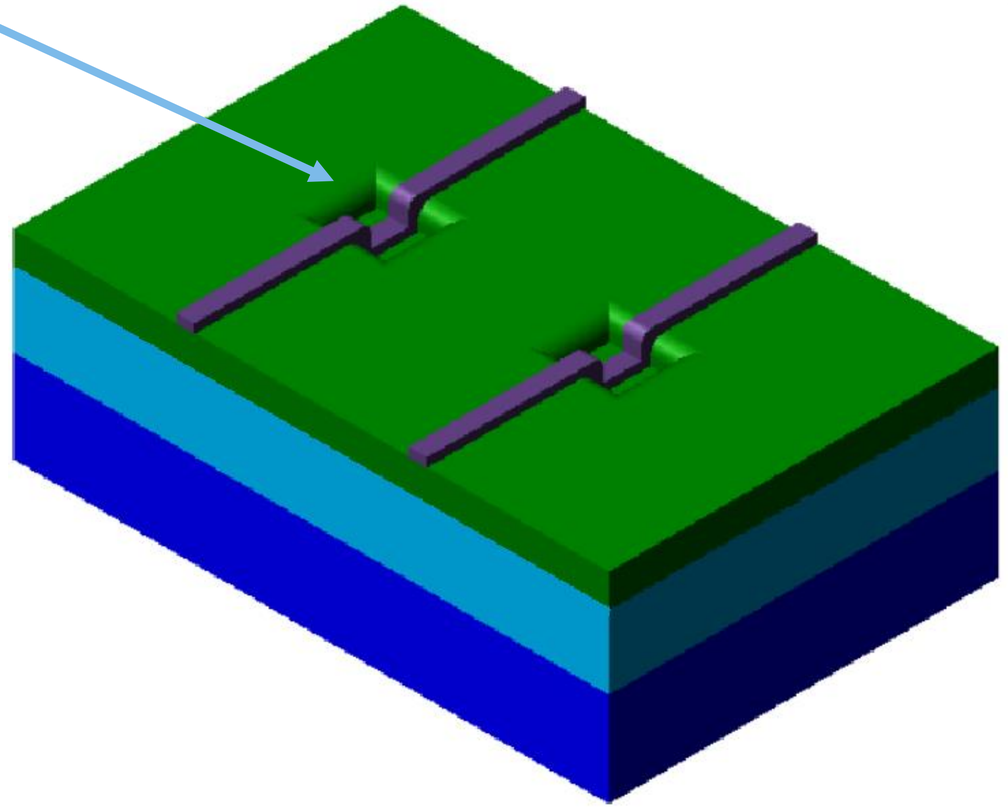
Etch Polysilicon Gate

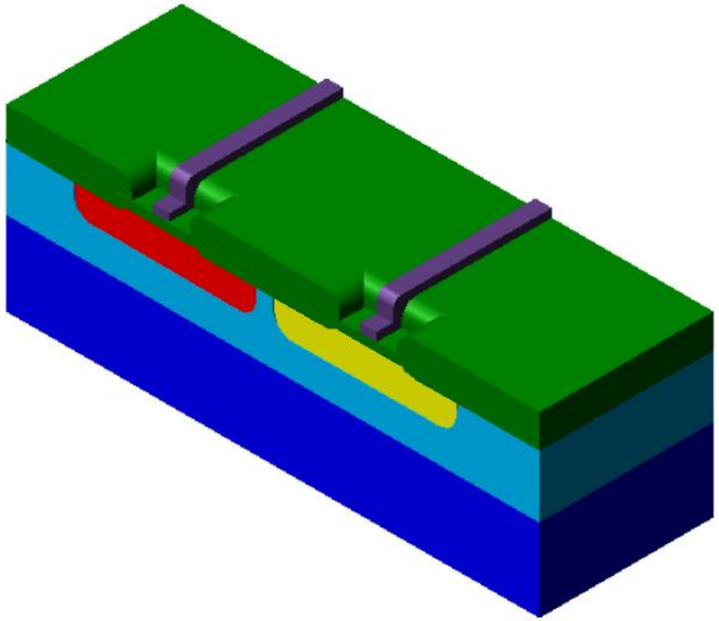


- Photoresist is deposited and patterned
- Etch the polysilicon
- Strip the resist

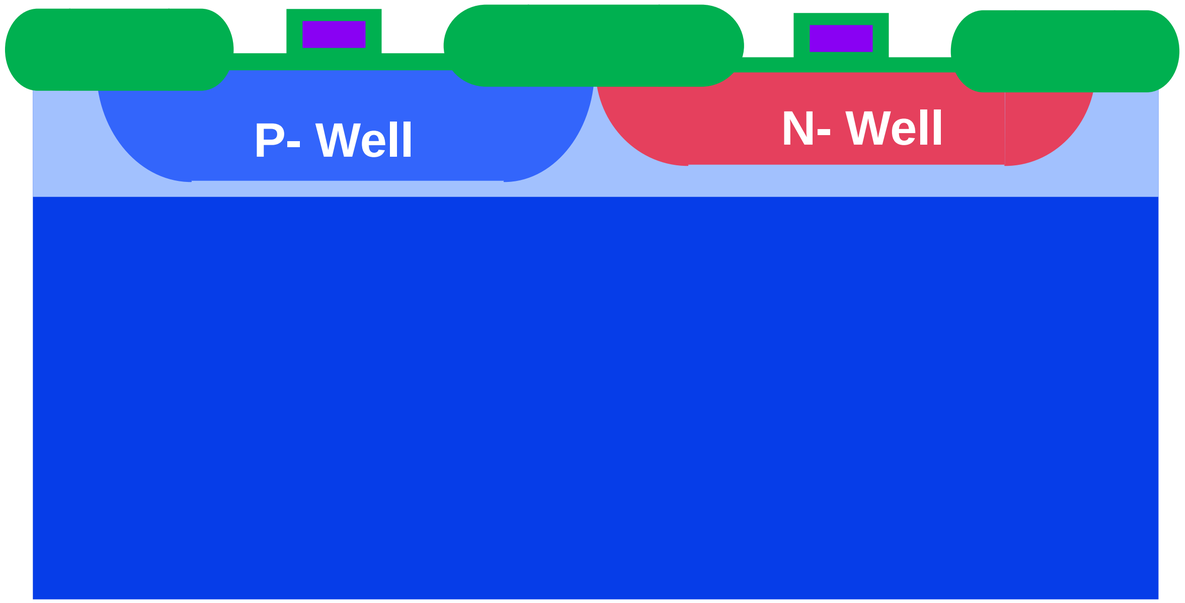
3-D View





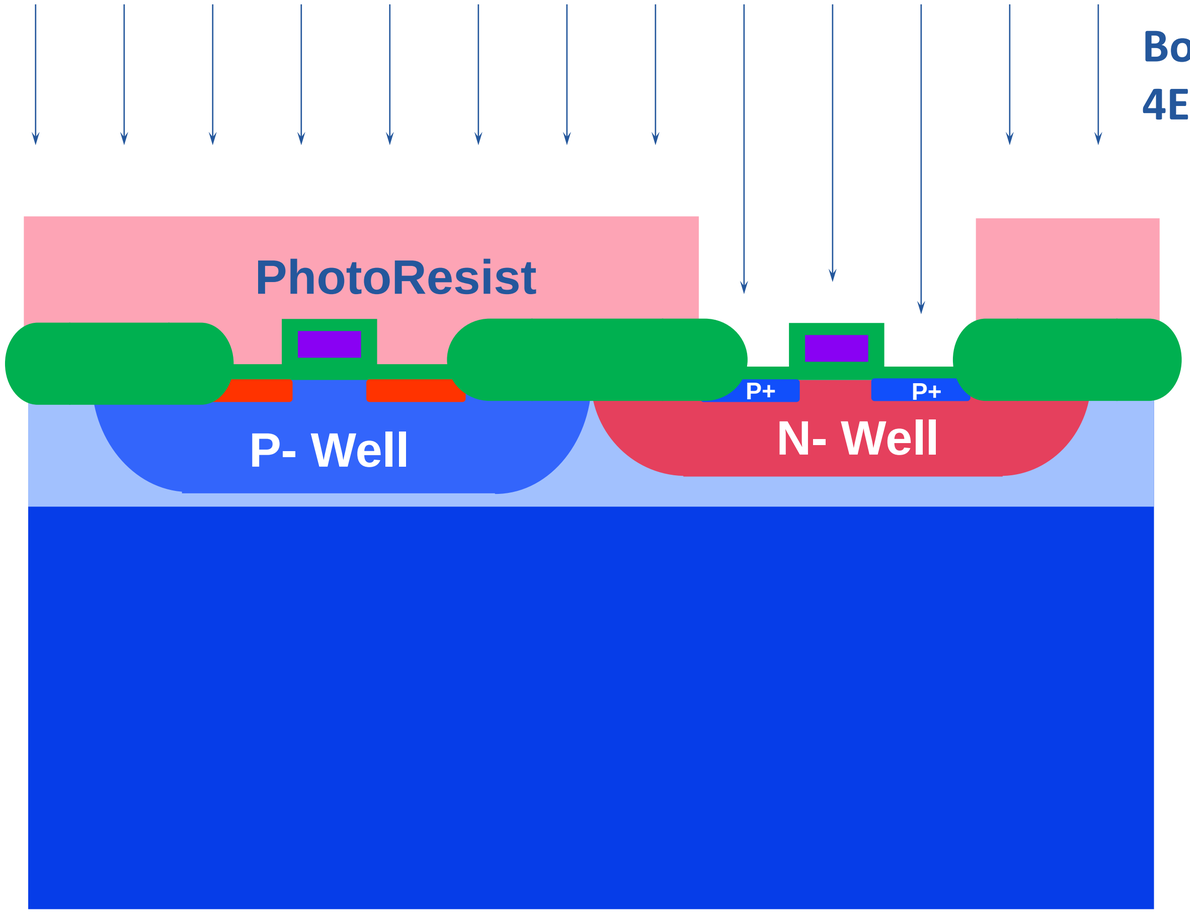


Poly Oxidation



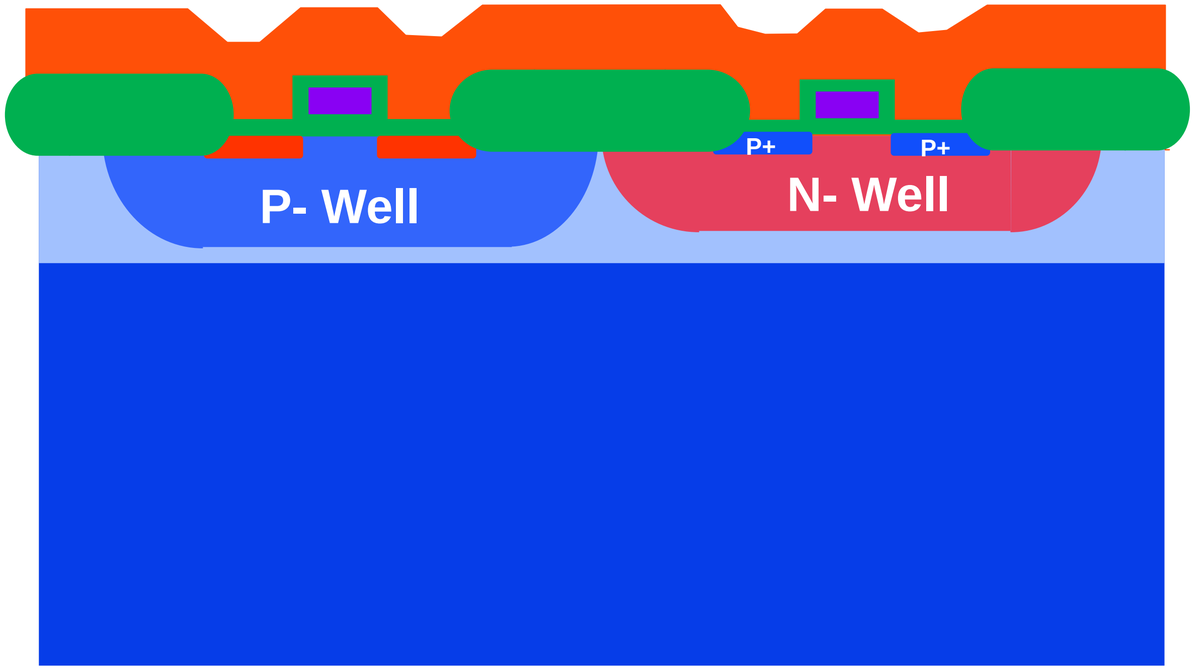
- Temperature: 900^{o}C
- Time: 105min O_2

P+ Source/Drain Mask and Implant



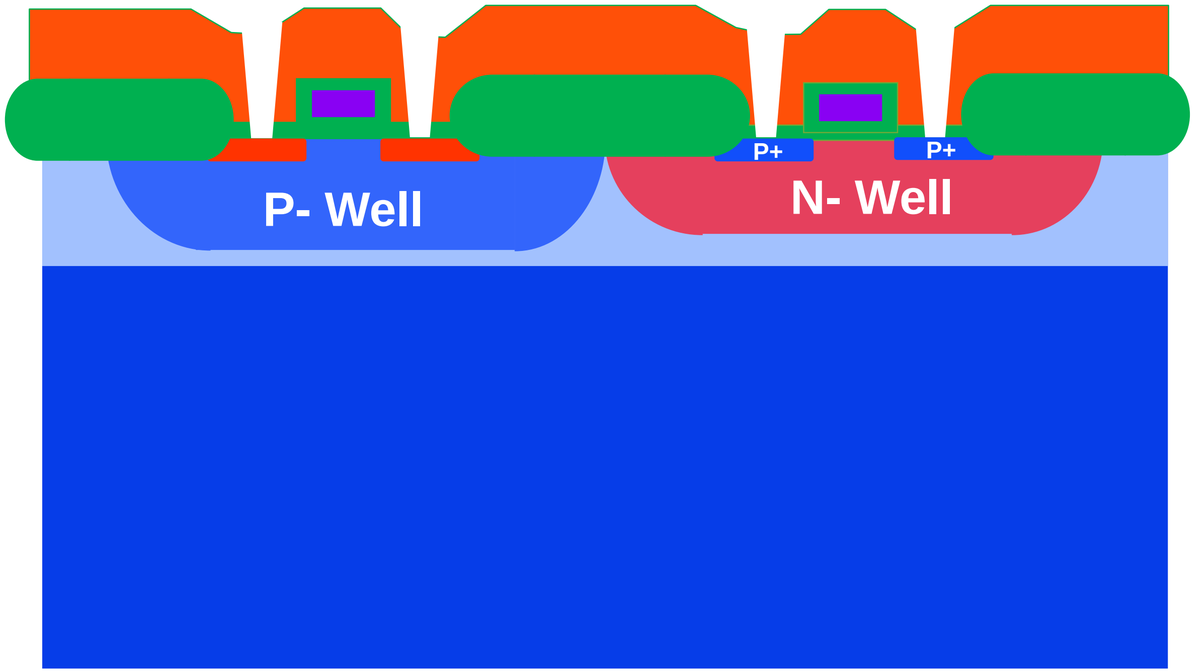
- Boron is implanted into the P+ S/D regions
- Followed by High Temperature Furnace Anneal

Deposit Dielectric



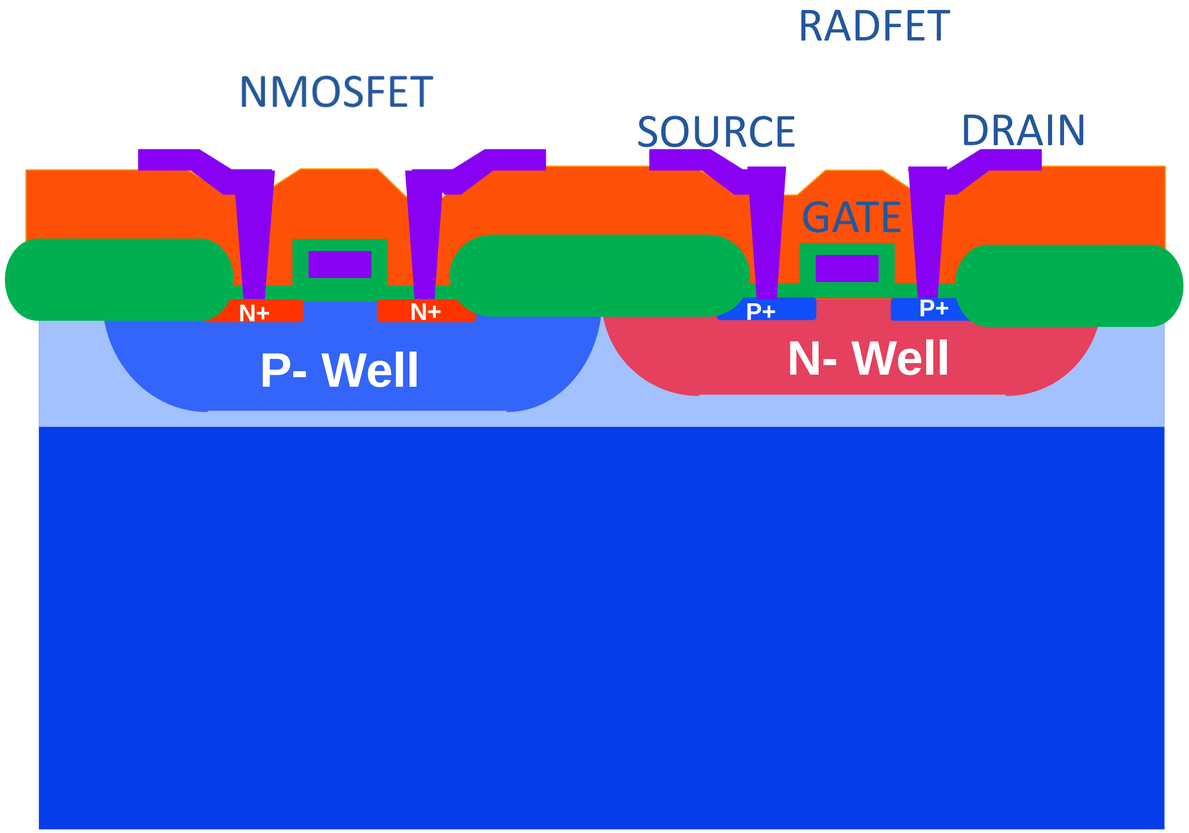
- Planarise surface prior to metal deposition

Contact Holes



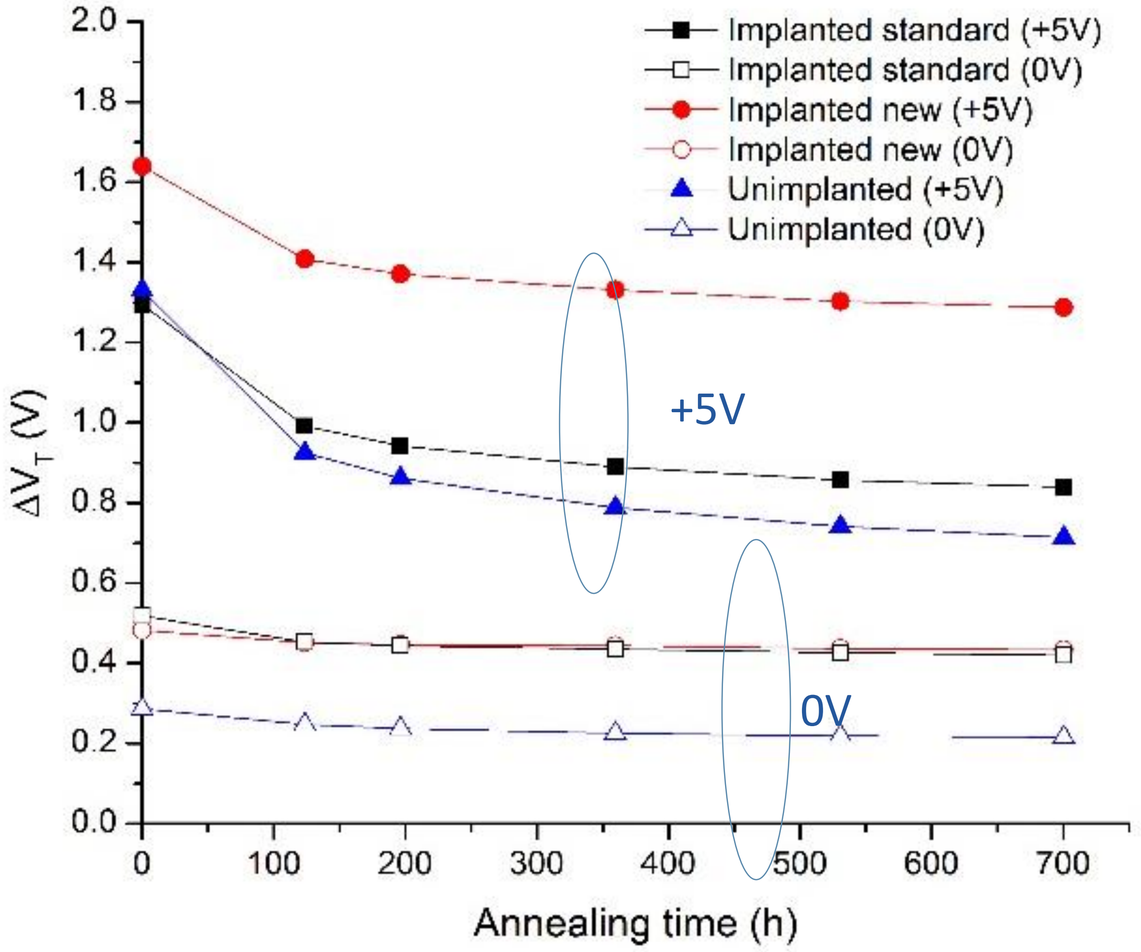
- Contact holes are etched through to the Source and Drain diffusions and the polysilicon gates

Metal Pattern

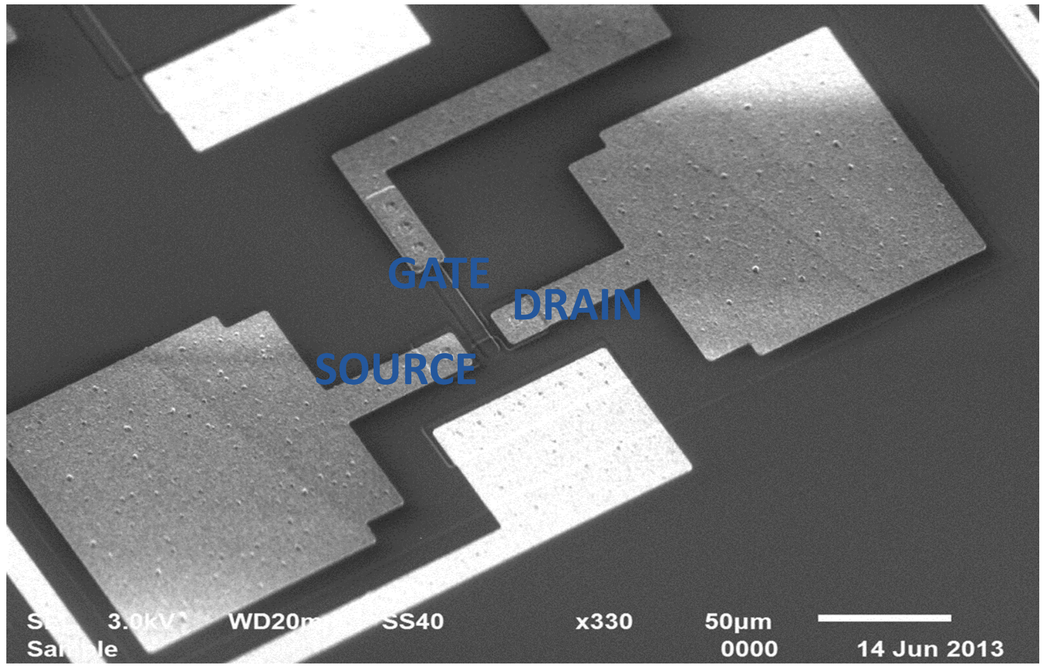


- 0.5µm thick Metal
  - Aluminium/0.5% Silicon Alloy
- Patterned and then etched to form electrodes

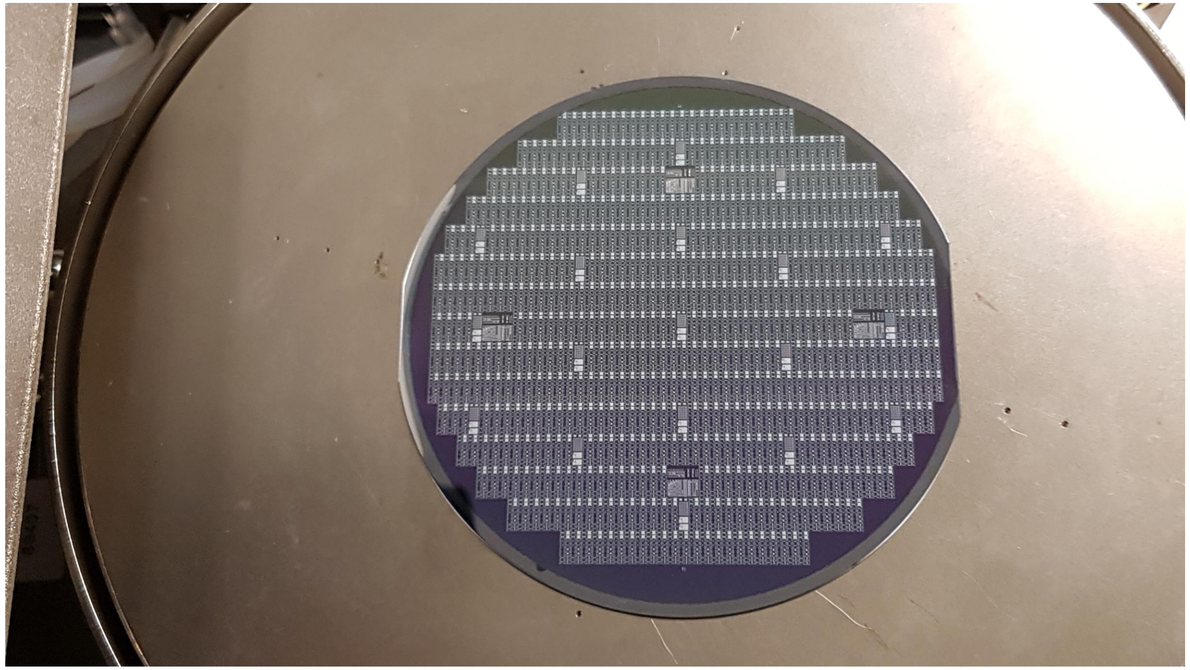
Processing Temperature



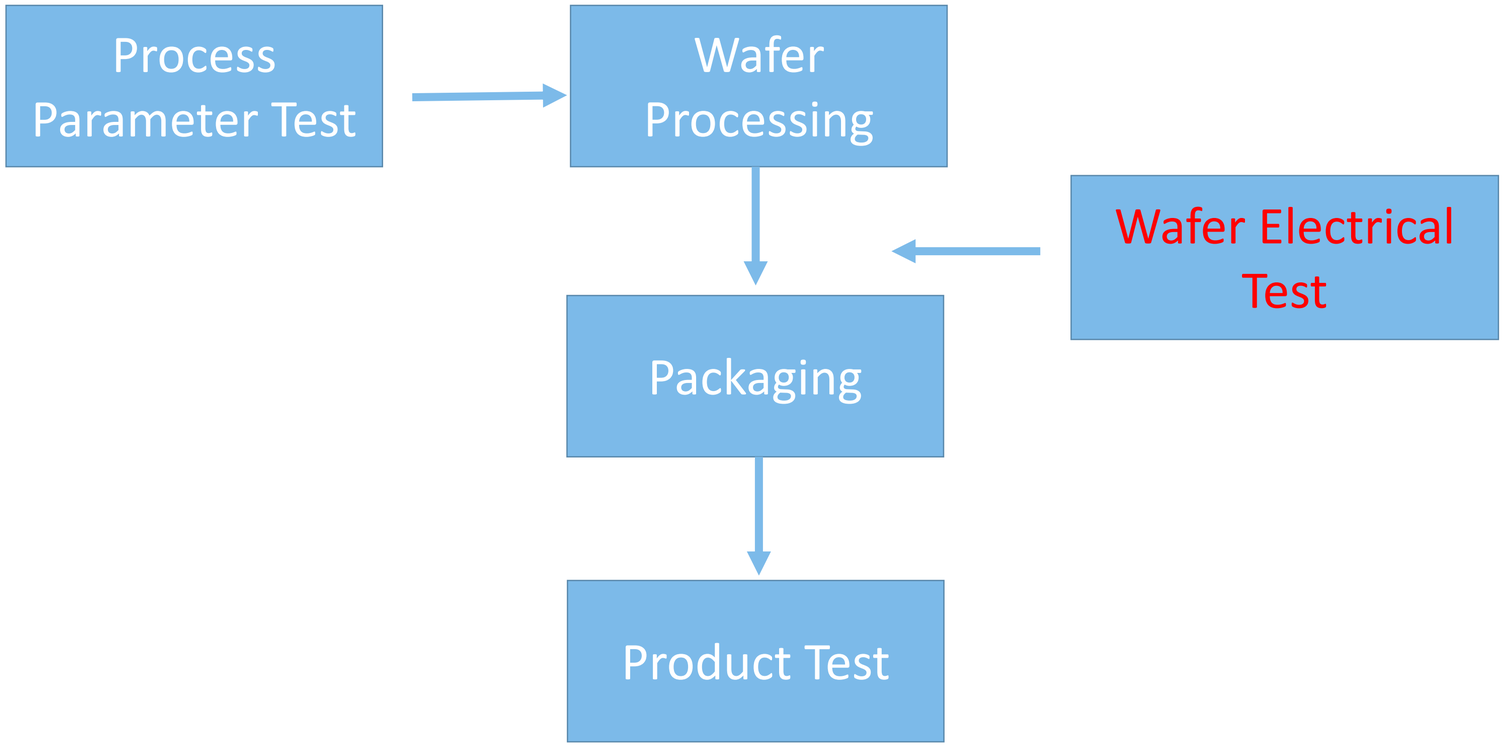
PMOS Transistor



Finished Wafer



Outline

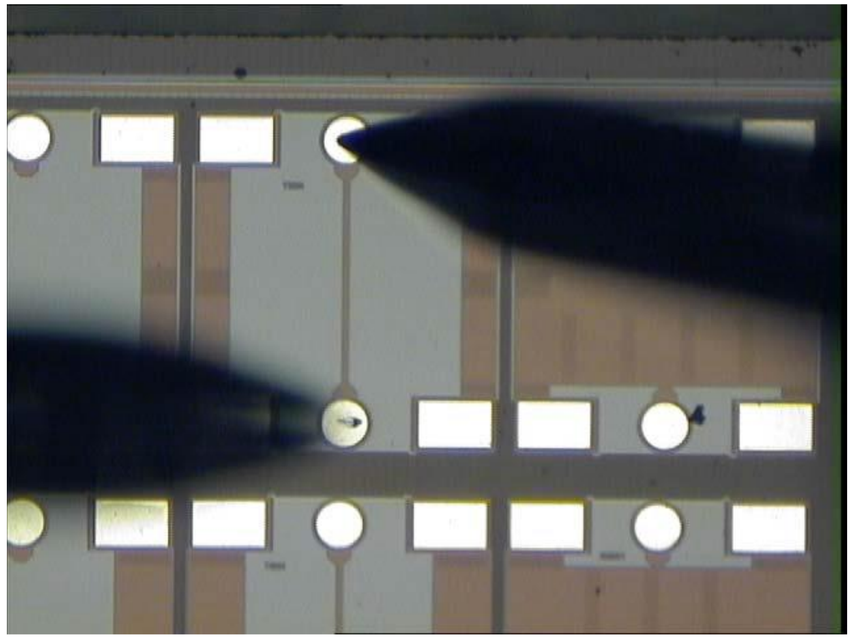

Process Parameter Test
Wafer Processing
Wafer Electrical Test
Packaging
Product Test

Wafer Testing

Cascade Semi-automatic Probe Station

Probe Needles positioned above Microchamber

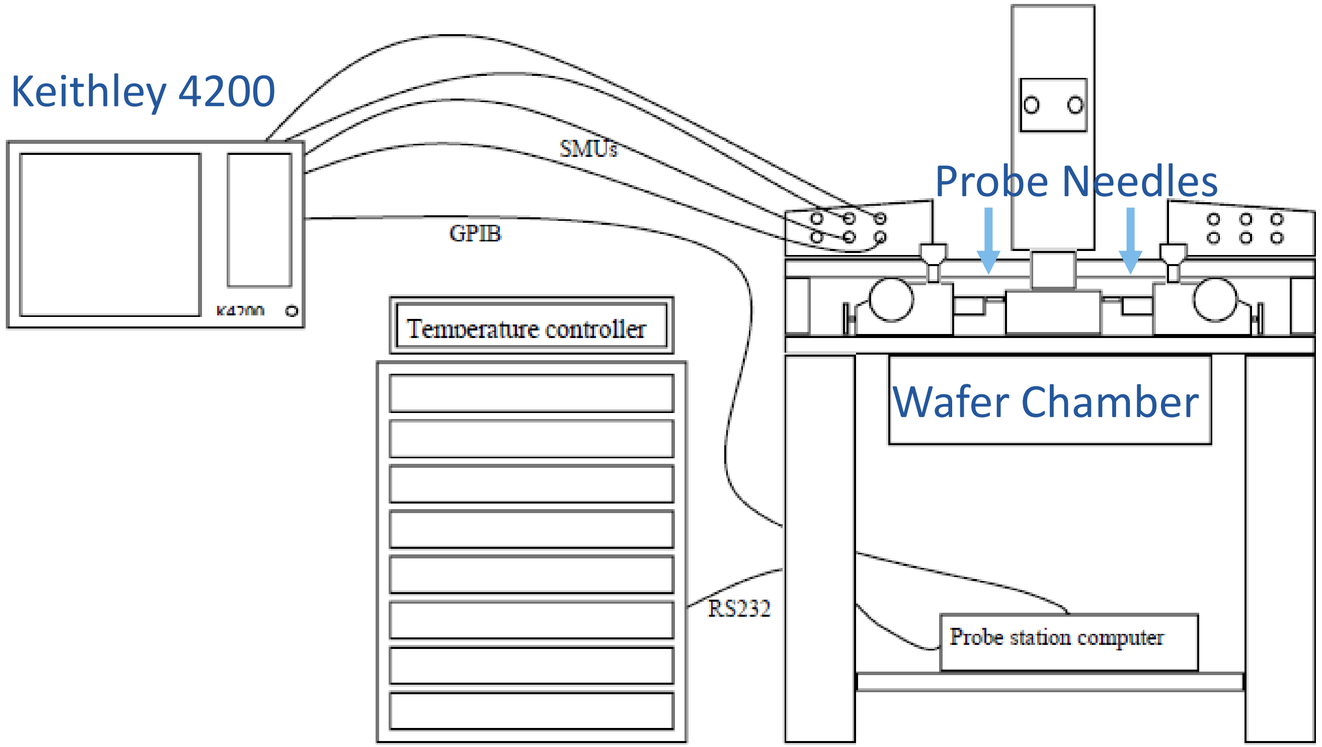
Wafer Loading into MicroChamber



Tungsten Probe Needles touching 100um*100um Metal Pads

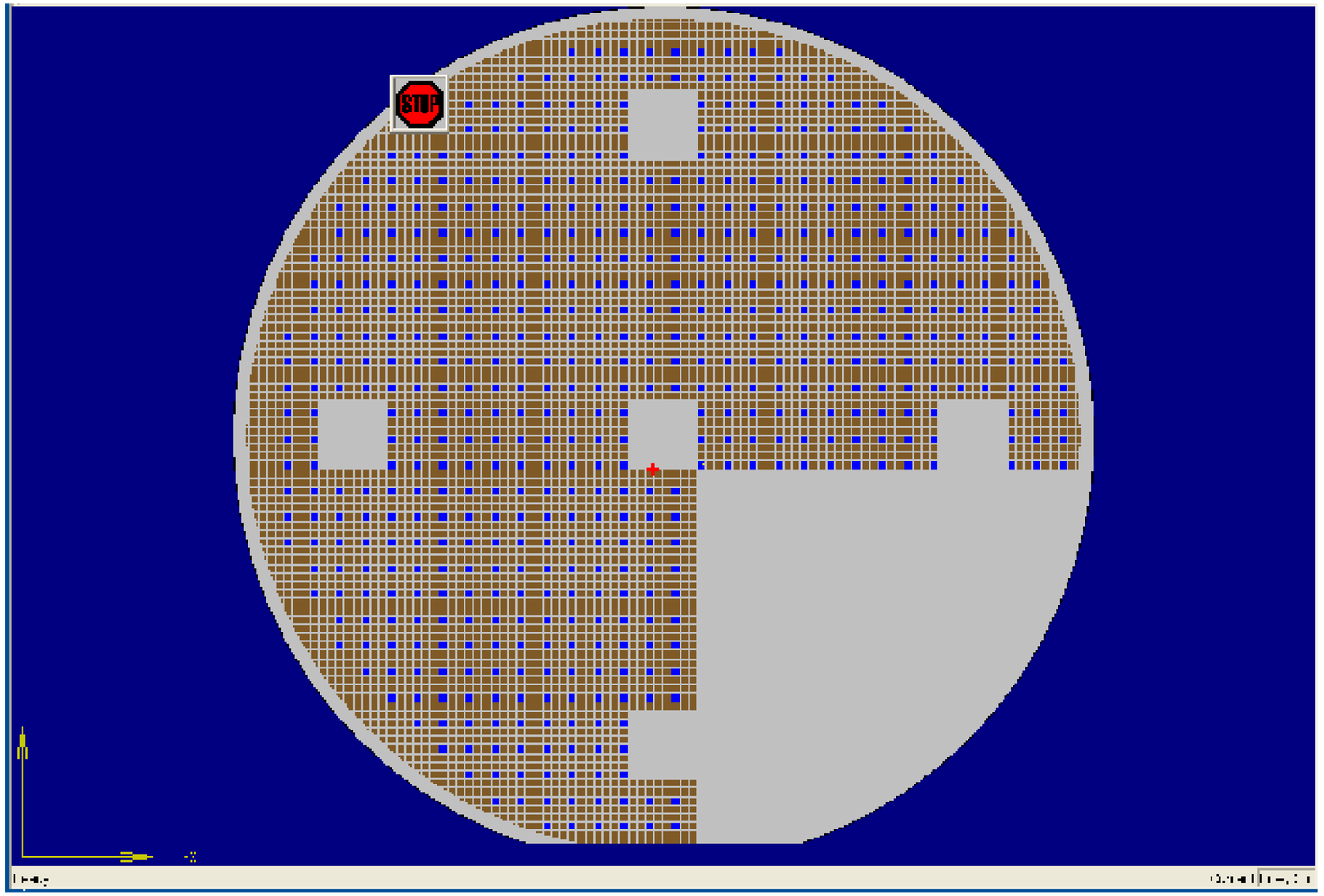
Measurement System

- Keithley 4200 Parameter Analyzer
  - Electrical Source-Measure Units (SMU)
- Keithley 4200 controls probe station
  - Wafer movement
  - Wafer Temperature



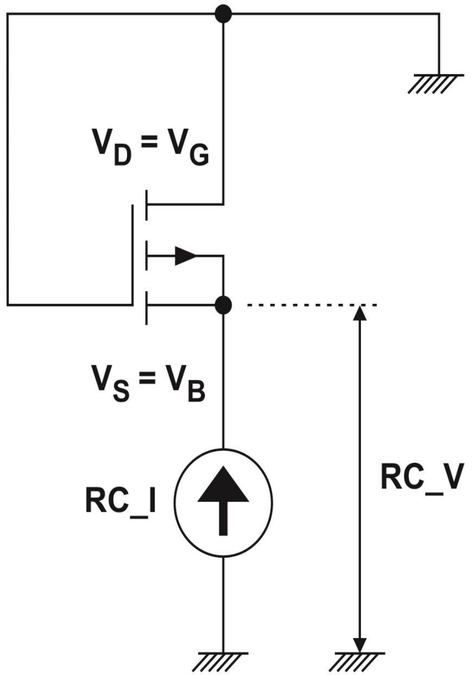
Probe Station

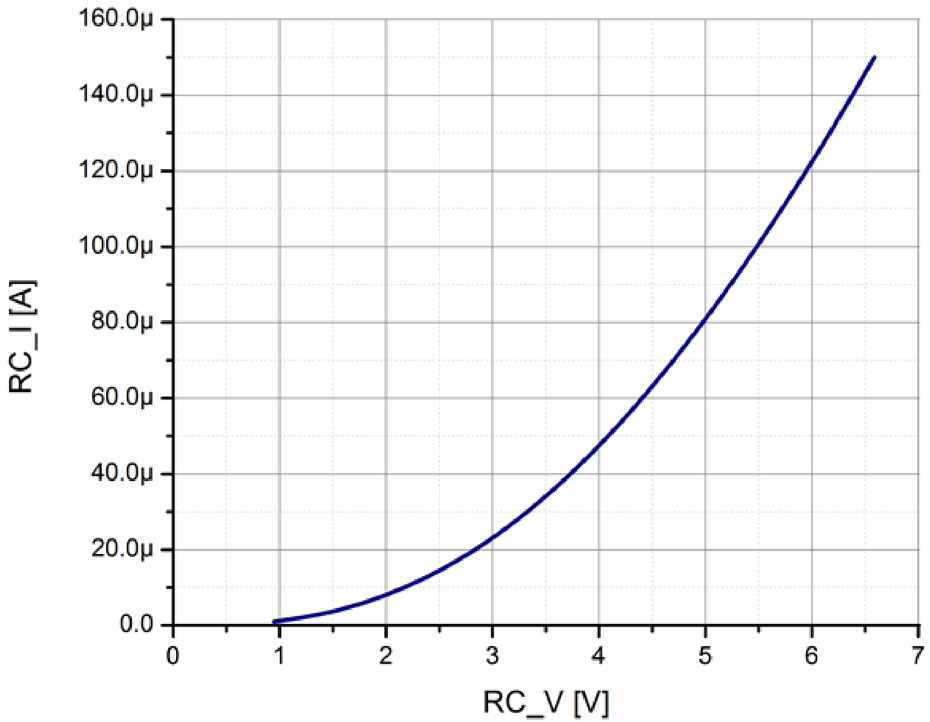
Typical Wafer Map



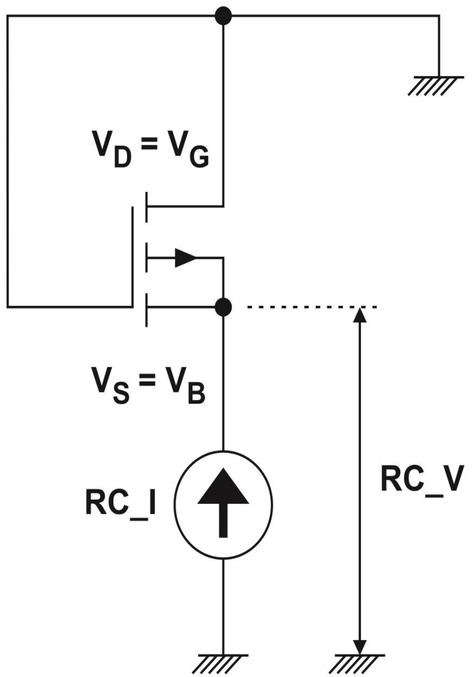
~200 chips tested out of >4,000/wafer

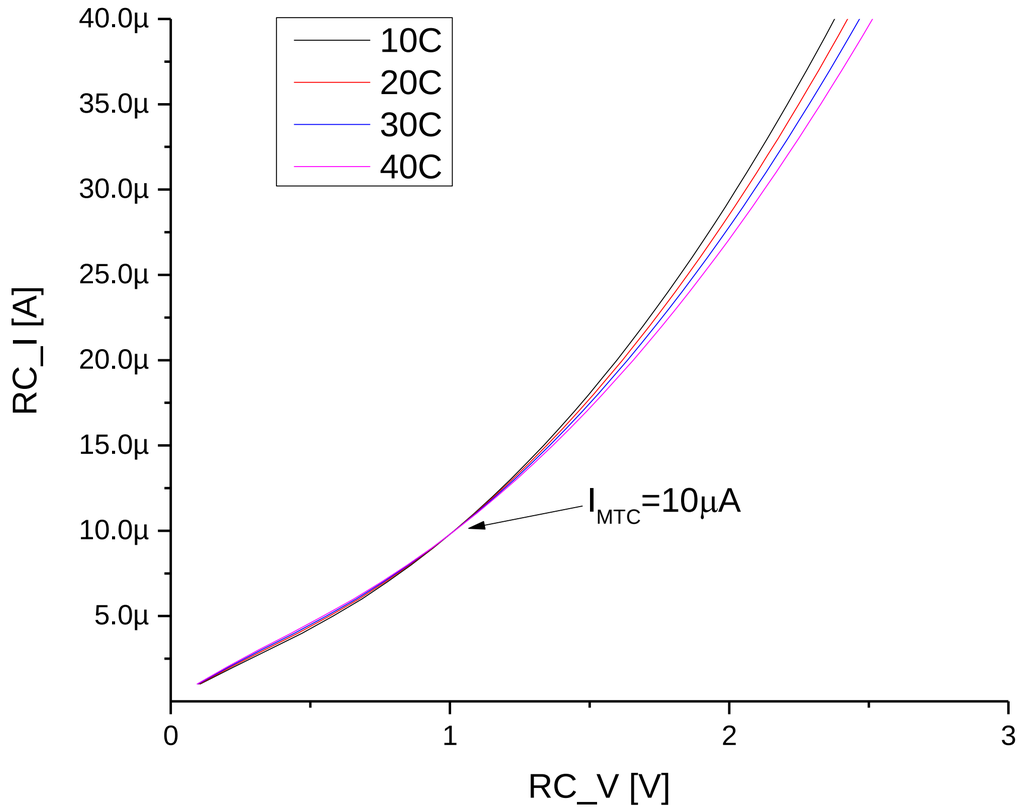
RADFET Current-Voltage Characteristics



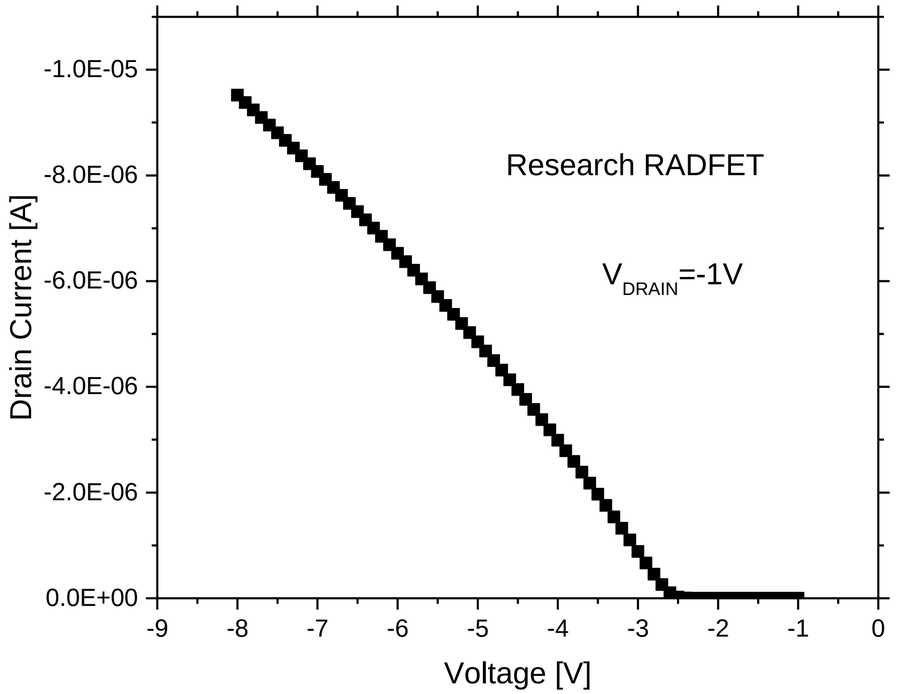


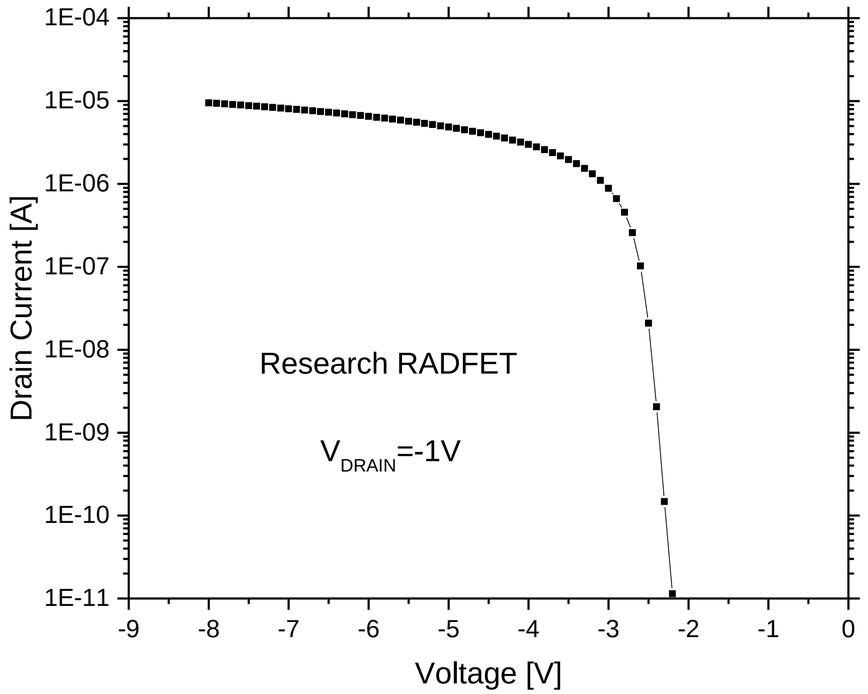
RADFET Temperature





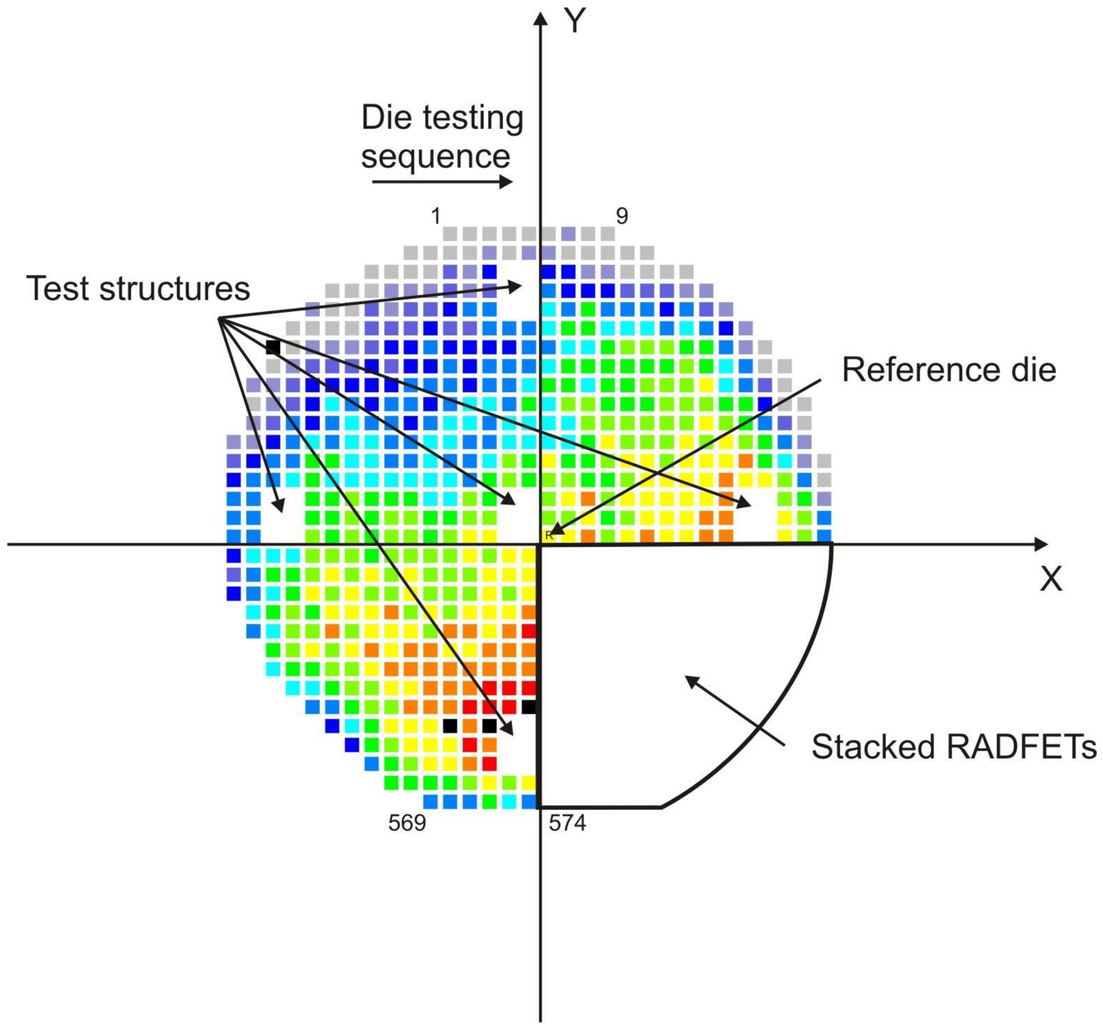
RADFET Current-Voltage Characteristics



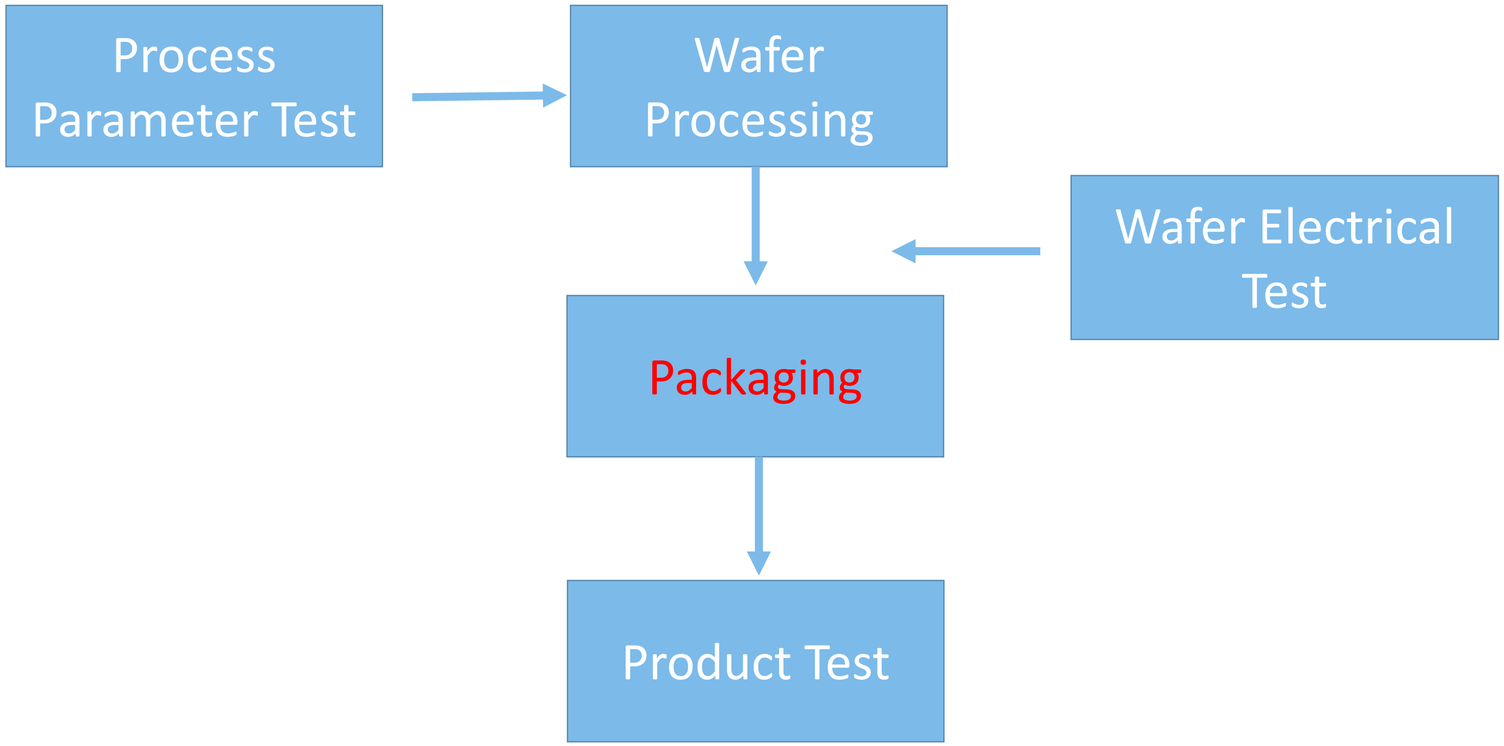


Electrical Parameters across Wafer

- Colour Map of electrical parameters
- Select areas of wafer for chip dicing and packaging



Outline


Process Parameter Test
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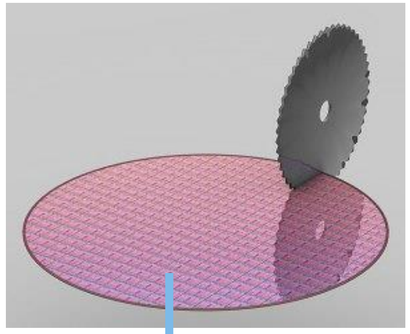
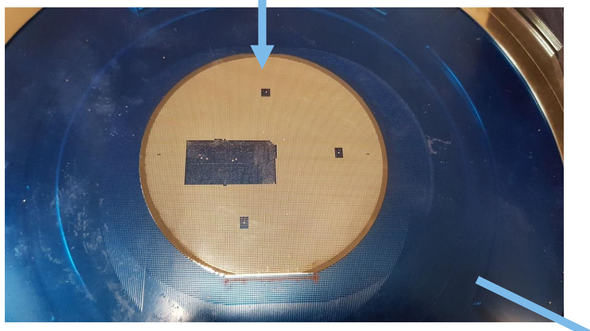
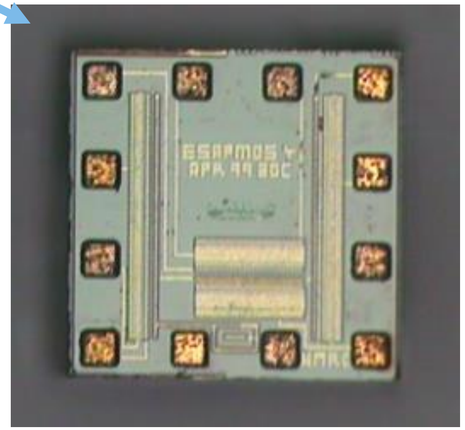
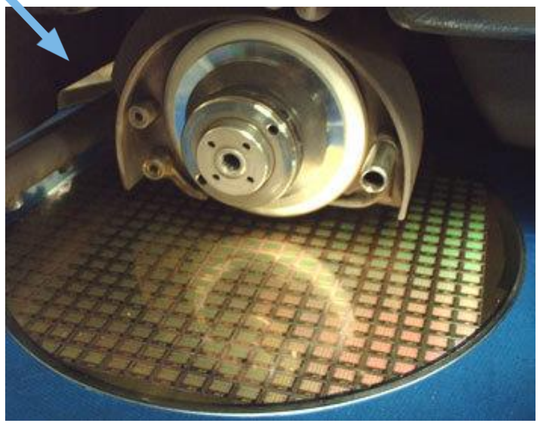
Dicing of Wafer



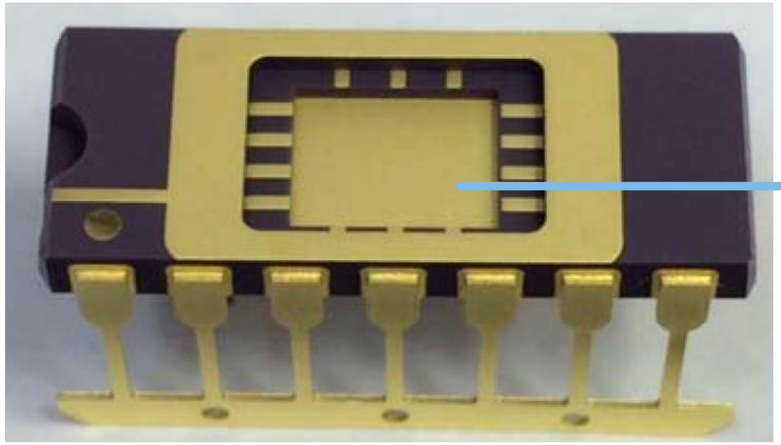


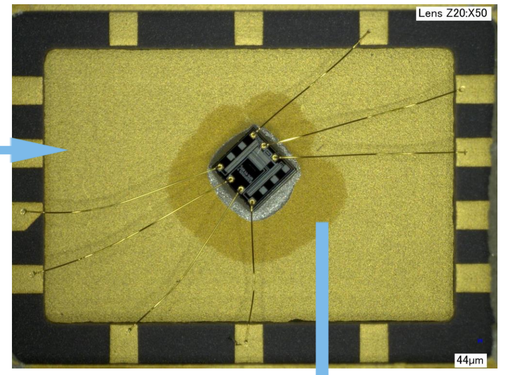


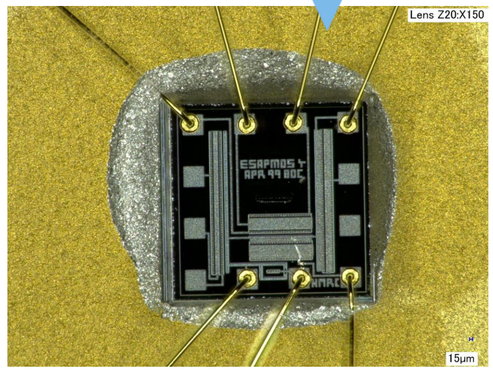


Packaging Process

- Ceramic Dual in Line Packaging Types
- Gold wire bonds
- Thermo-compression



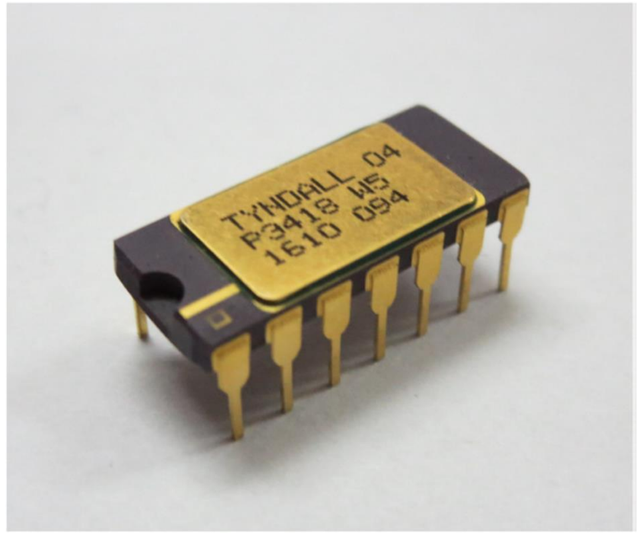




TPT Semi-automatic Wire-bonder

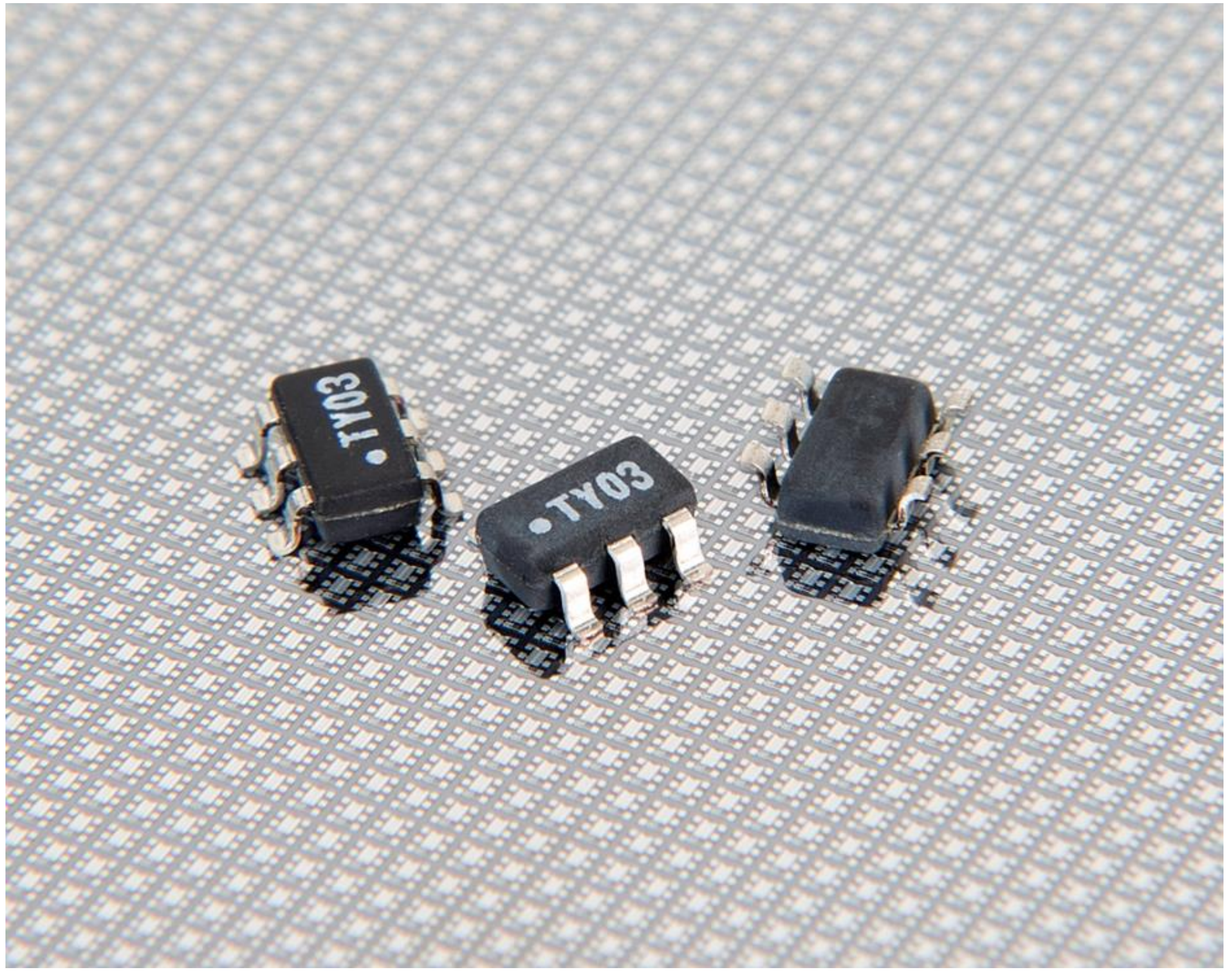
Ceramic Packaging Lids

- Kovar Lids are attached to package
  - Same process as used for die attach
  - 125°C maximum temperature
- Hermetic sealing subcontracted
  - 300°C maximum temperature
- Package Dimension (LxWxH)
  - 13mm*8mm*3mm

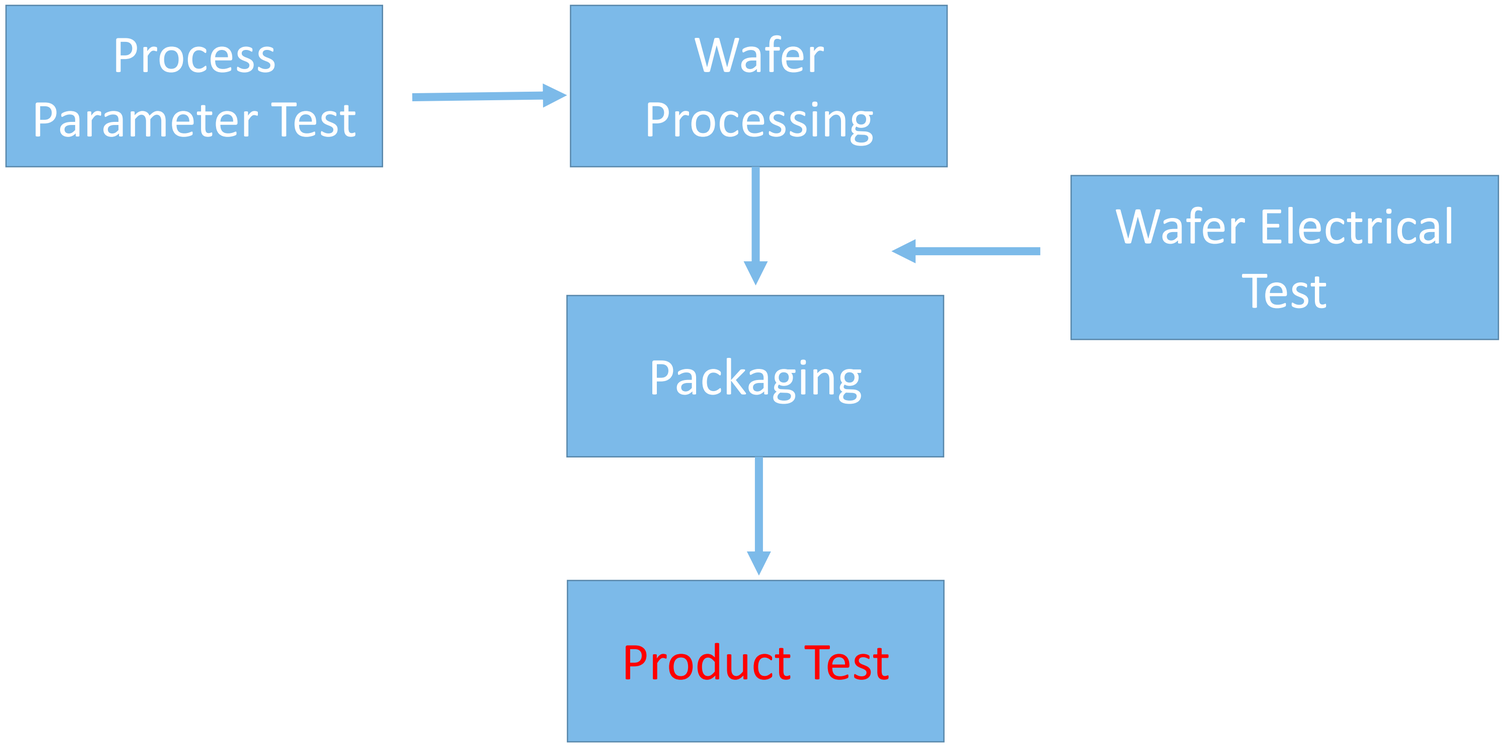


Plastic Packaging

- SOT23 plastic package
  - 3mm*3mm*1mm (LxWxH)
  - 175C maximum temperature
- Thinning of silicon wafer required to fit into package
  - 525µm thinned to 200µm



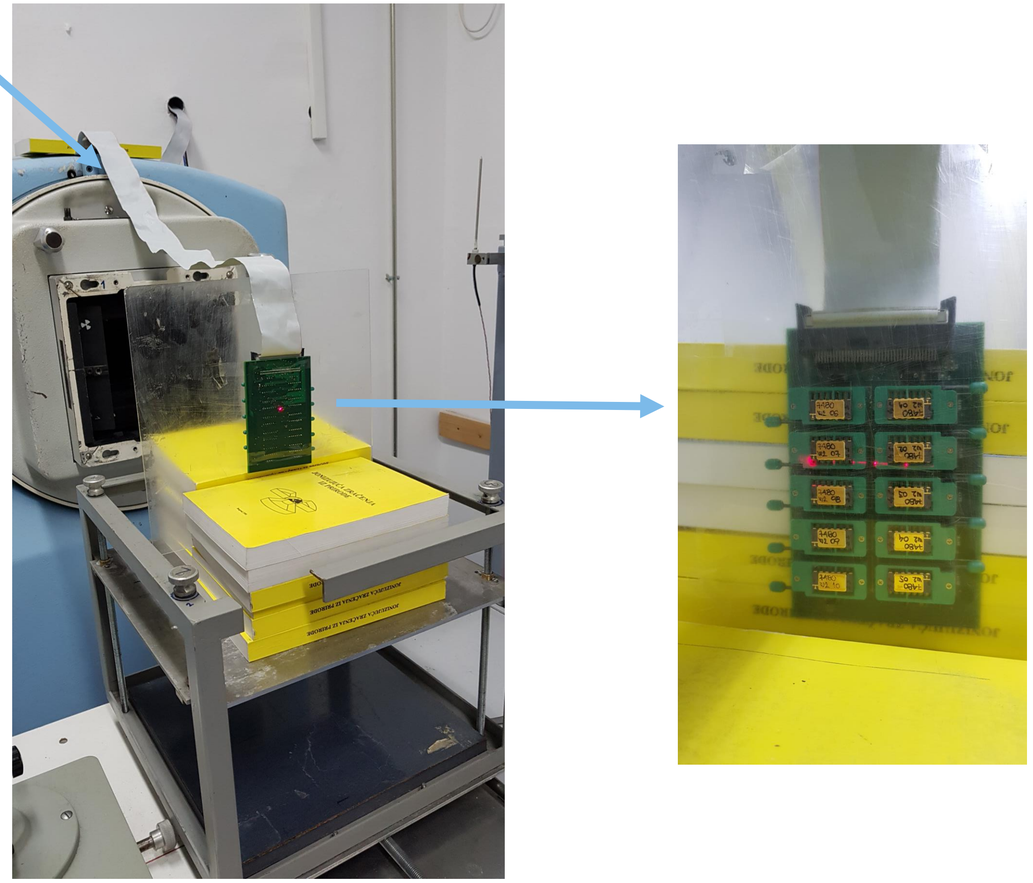
Outline


Process Parameter Test
Wafer Processing
Wafer Electrical Test
Packaging
Product Test

Product Testing

- All products are first electrically tested using Keithley 4200 + test fixture
- Number of samples irradiated with Co60 source in Vinca, Serbia
- Automatic reader used to characterise a number of RADFETs simultaneously

Flex Cable to Automatic Readout System

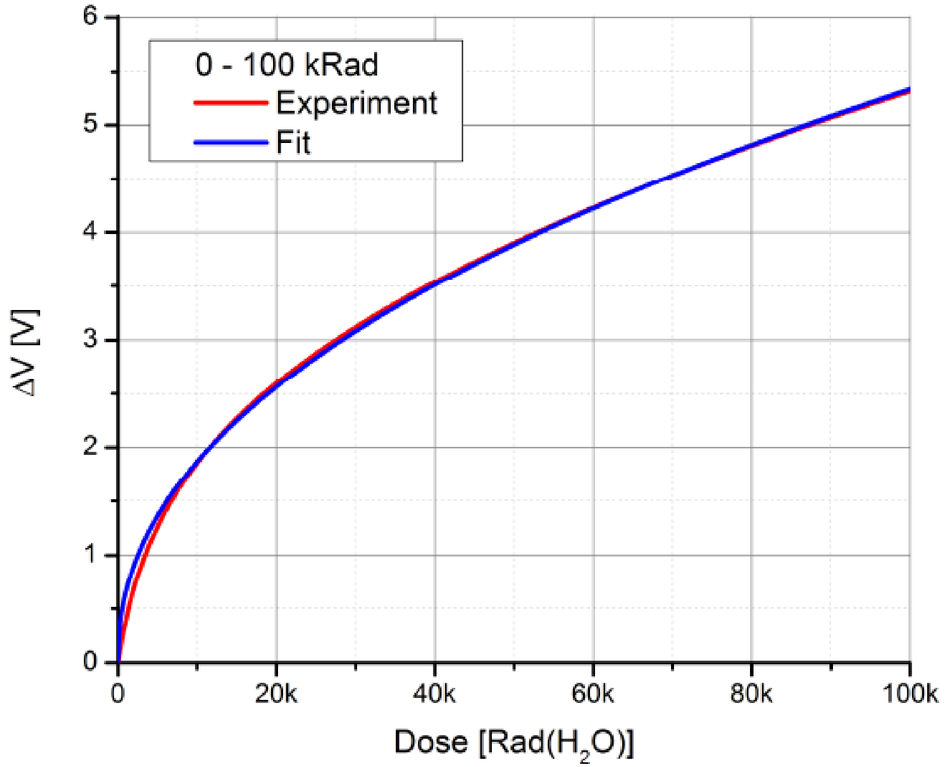


Sensitivity Curve

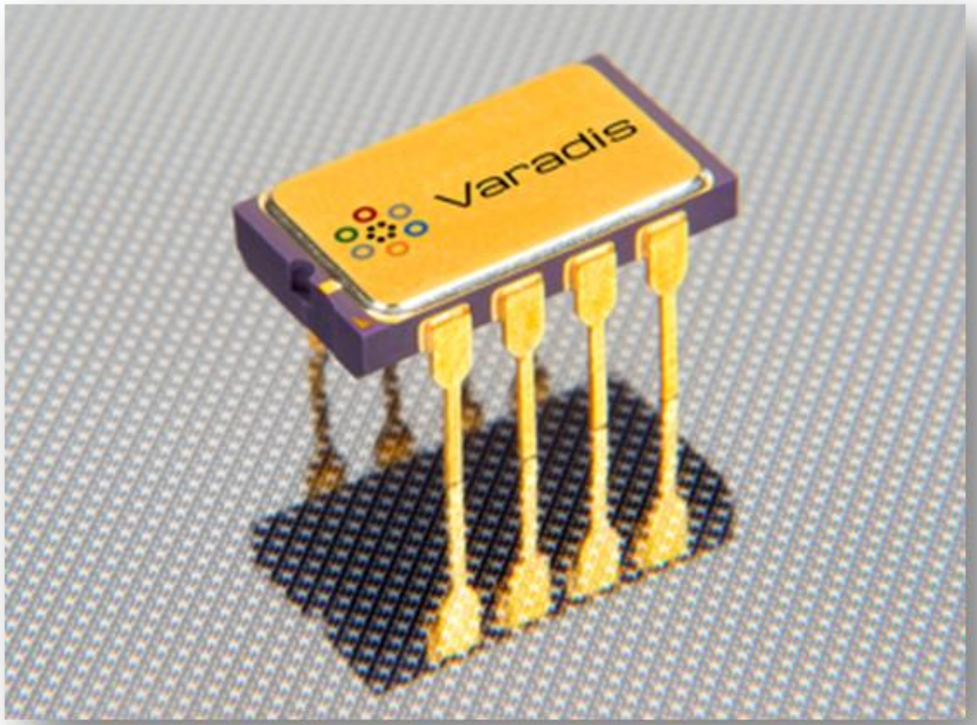
- Mean Sensitivity Curve constructed from statistical data
- Parabolic Model fitted to Sensitivity Curve

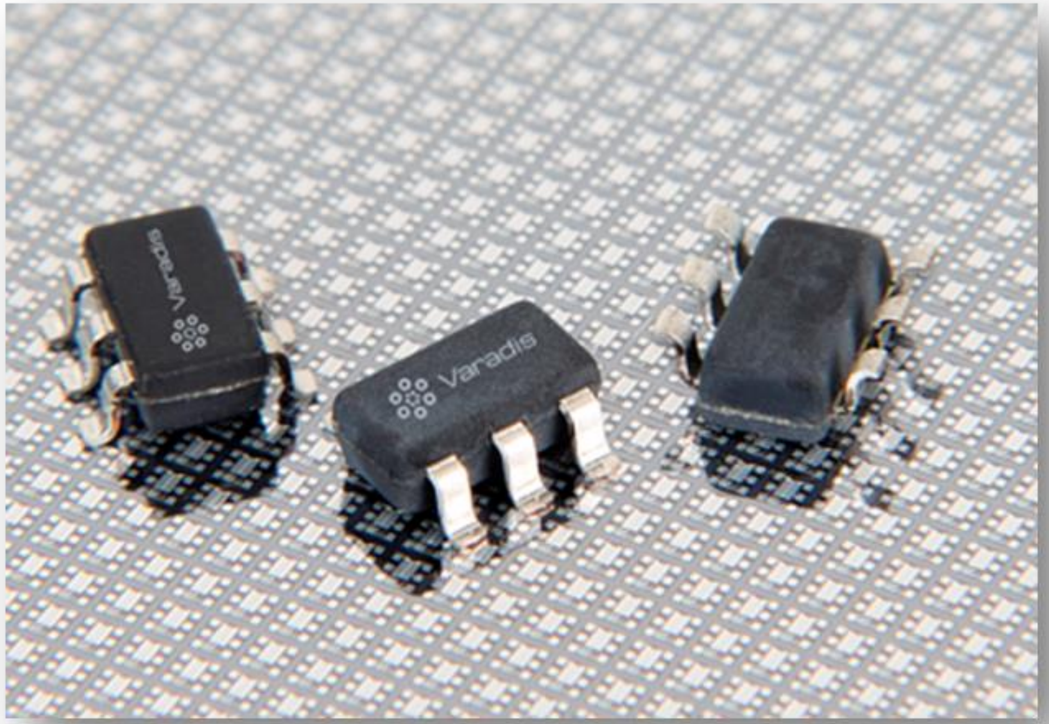
$$\Delta V_T = A \times Dose^B$$

- Model Fits sent to customer with product



Varadis Spin-out Company





http://www.varadis.com

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Rialtas na hÉireann Government of Ireland
Tionscadal Éireann Project Ireland 2040
Ireland's European Structural and Investment Funds Programmes 2014-2020
Co-funded by the Irish Government and the European Union
European Union
European Structural and Investment Funds