



Design of Radiation Hardened RADFET Readout System for Space Applications

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innovations
for high
performance

microelectronics



Agenda

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- 3 RADFET Dosimetry
- 4 Rad-hard Readout System Design
- 5 Analog Signal Conditioner
- 6 Self-Adaptive Multiprocessor System-on-Chip
- 7 Conclusion

- **The concept outlined in this presentation has been accepted for publication at Euromicro Conference on Digital Systems Design (DSD), 2020**

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“Design of Radiation Hardened RADFET Readout System for Space Applications”

1. Motivation

■ Space radiation environment

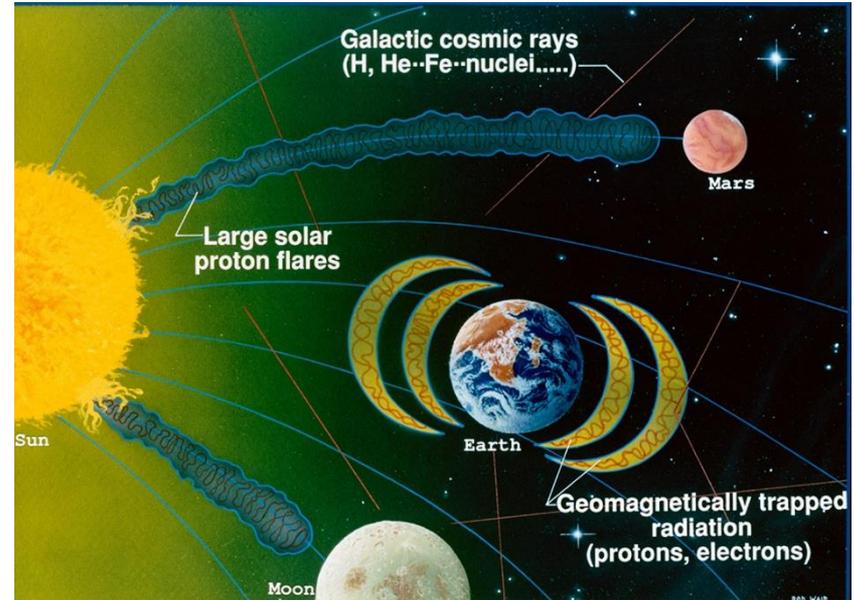
- Complex (wide range of sources and energies)
- Dynamic (variable radiation intensity)

■ Radiation effects

- Lethal for humans
- Source of failures in electronics
 - ❖ Total Ionizing Dose (TID) effects
 - ❖ Single Event Effects (SEEs)

■ Space mission requirements

- Radiation dosimetry – *adsorbed dose and dose rate measurement*
- Radiation-hardened electronics – *robust to TID and SEEs*



[Illustration from <https://www.nasa.gov>]

1. Motivation

■ Common radiation dosimeters in space applications

- Diodes – *measure dose rate in terms of radiation-induced current*
- RADFETs – *measure absorbed dose in terms of threshold voltage shift*

■ RADFET's advantages

- Operation in passive mode (without bias)
- Storage of dosimetric information

■ Limitations of existing RADFET readout solutions

- Measuring only absorbed dose – *other sensors required for dose rate monitoring*
- Static radiation hardening – *not optimal under dynamic radiation conditions*

2. Contribution



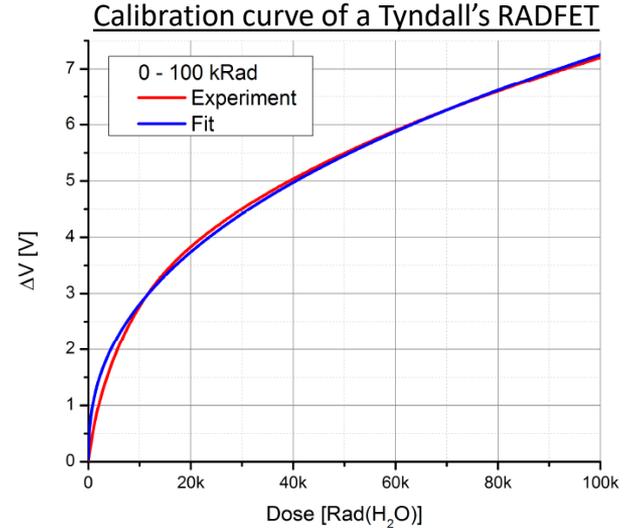
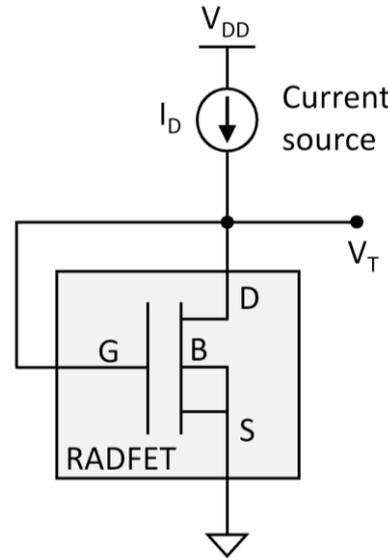
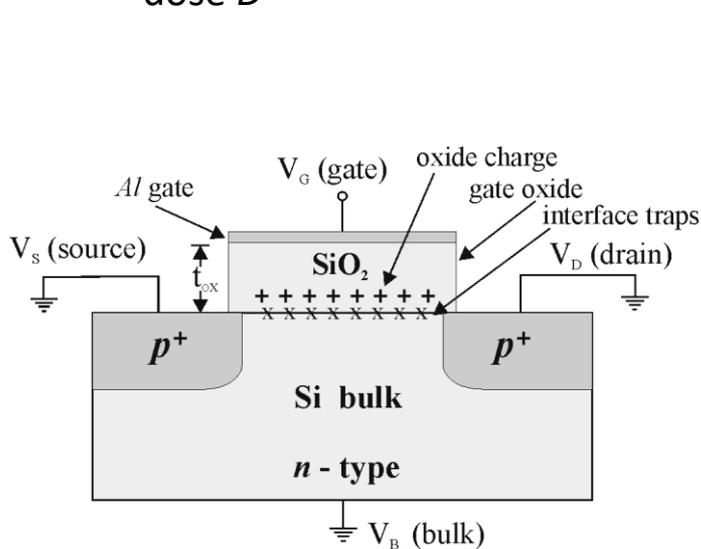
- **Proposed solution: A RADFET readout system for real-time measurement of absorbed dose and dose rate with a self-adaptive multiprocessing system-on-chip**
- **Measurement of absorbed dose and dose rate with a single RADFET**
 - No need for additional radiation sensors
 - Simplified and cheaper design
- **Self-adaptive fault-tolerant multiprocessing platform**
 - Provides fault tolerance only when required
 - Can perform additional onboard functions
 - Enables high level of integration

3. RADFET Dosimetry

Absorbed Dose Measurement

- Radiation results in charge accumulation in oxide layer
- Threshold voltage shift ΔV_T increases with dose D

$$\Delta V_T = a - \frac{a}{1 + b \cdot D^c}$$



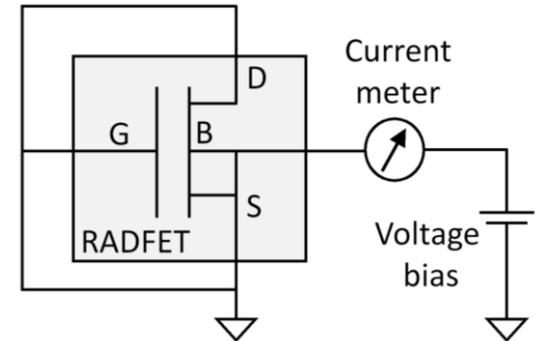
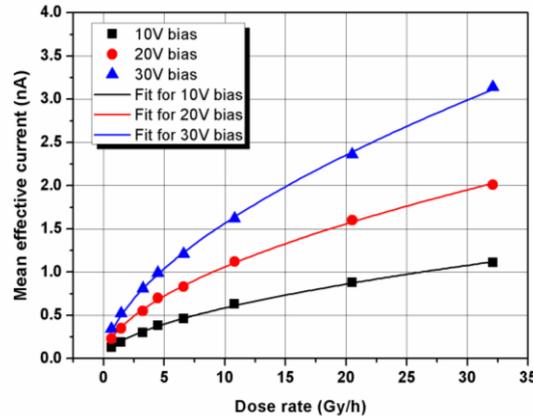
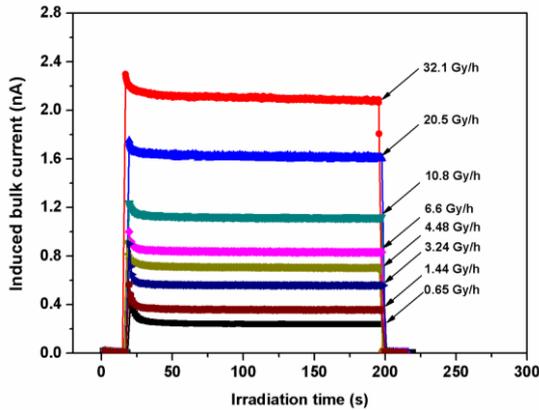
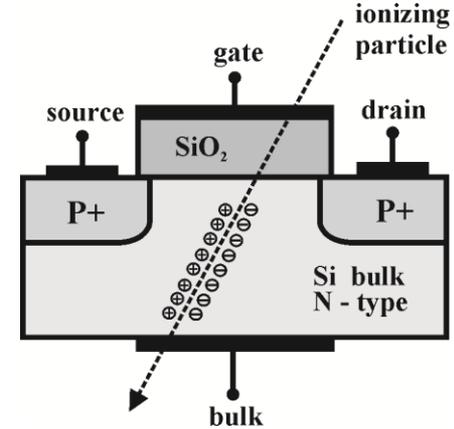
3. RADFET Dosimetry

■ Dose Rate Measurement

- Radiation generates stable bulk current at medium and high dose rates (e.g. 0.65 – 32 Gy/h)

$$I = k \cdot V_{BIAS} \cdot D_R^m$$

- At lower dose rates, pulsed current is induced

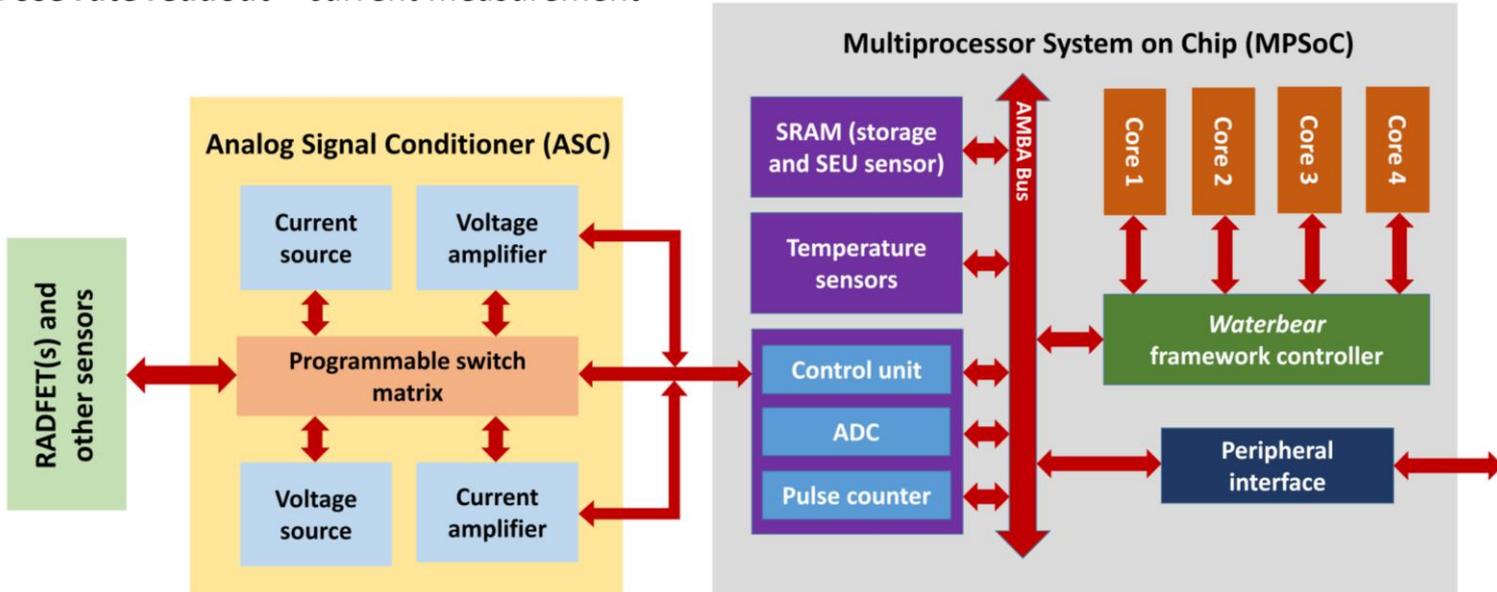


4. Rad-hard Readout System

Operating modes

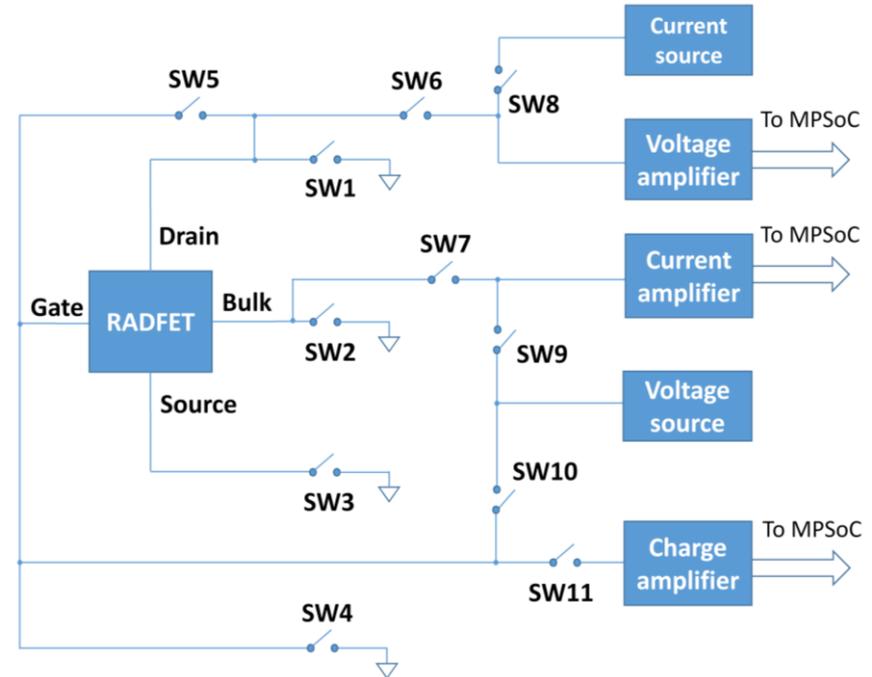
- **No readout** – RADFET operates in passive mode
- **Absorbed dose readout** – voltage measurement
- **Dose rate readout** – current measurement

Universal architecture
(can be applied to other sensors)



5. Analog Signal Conditioner

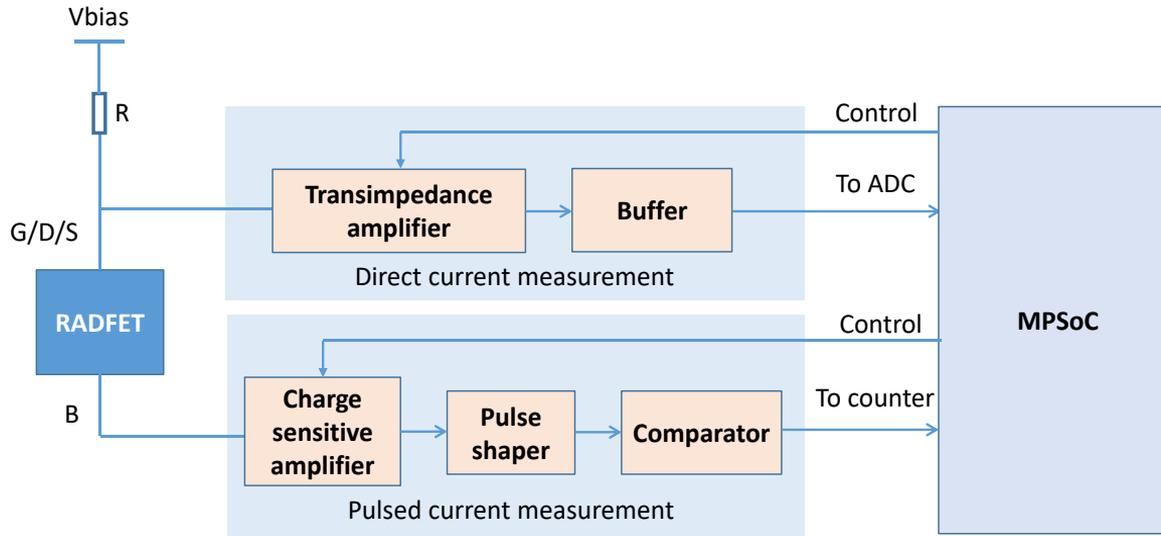
- **Voltage and current measurement**
 - Standard voltage amplifier for threshold voltage measurement
 - Transimpedance amplifier for direct current measurement
 - Charge amplifier for pulsed current measurement
- **Switching between operating modes**
 - Controlled by MPSoC
- **Can be implemented with commercial radiation-tolerant components**



5. Analog Signal Conditioner

■ Direct and pulsed current measurement

- Open issues to be addressed:
 - ❖ *Possible interference between the two current readout modes*
 - ❖ *Possible overlapping of the direct and pulsed current ranges*



6. Multiprocessor System-on-Chip (MPSoC)



■ Main functions in readout system

- A/D conversion of DC voltage from ASC
- Counting of voltage pulses from ASC
- Control of switching matrix and amplifier gain in ASC

■ IHP's framework controller

- Dynamic selection of operating modes
- Trade-off between performance, fault tolerance and power consumption
- Flexible – can be applied to an arbitrary number of processing cores

■ Radiation hardness / fault tolerance

- IHP's 130 nm CMOS technology resistant to TID effect and Single Event Latchup (SEL)
- Core-level fault tolerance enabled with embedded SRAM acting as a particle monitor

6. Multiprocessor System-on-Chip (MPSoC)

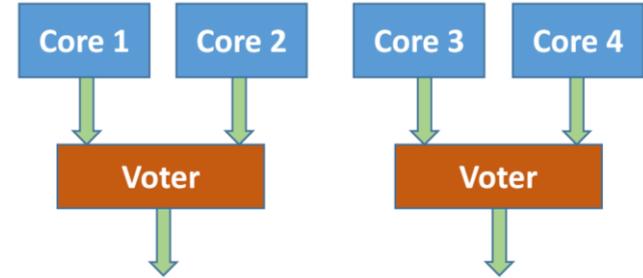
■ Self-adaptive quad-core processing platform

- Dynamic selection of operating modes
 - ❖ *De-stress mode* : some cores are switched off
 - ❖ *Fault tolerant mode*: cores are set into various fault-tolerant configurations
 - ❖ *High performance mode*: parallel processing

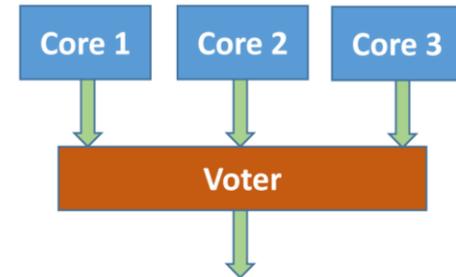
■ Core-level fault-tolerance

- Common configurations
 - ❖ *Supply voltage / frequency scaling*
 - ❖ *Dual Modular Redundancy (DMR)*
 - ❖ *Triple Modular Redundancy (TMR)*
- **Use of existing on-chip resources for fault-tolerance**

2 DMR processing units



1 TMR processing unit



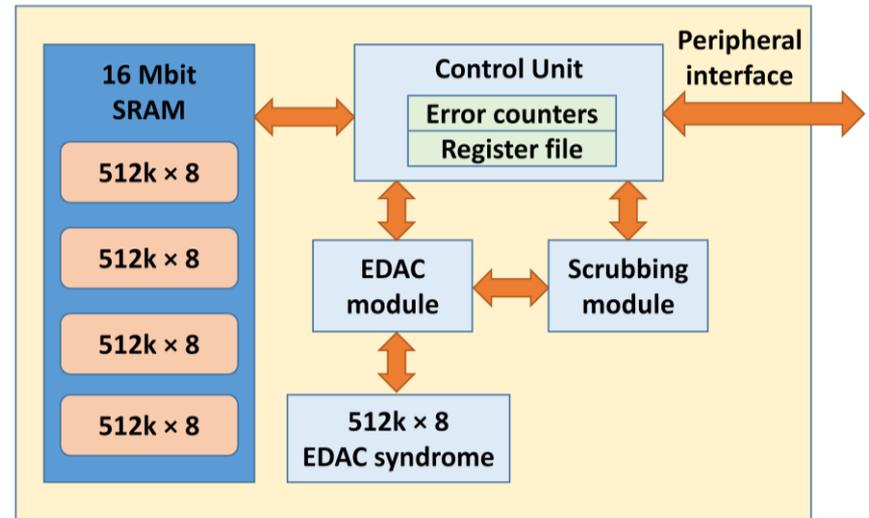
6. Multiprocessor System-on-Chip (MPSoC)

■ Embedded SRAM as Particle Detector

- On-chip data storage memory used also as a particle detector
- Provides information on the particle flux for triggering the fault-tolerant modes
- Flux is proportional to the number of bit errors in SRAM
- Error detection and correction (EDAC) and scrubbing logic used to detect and correct errors
- Counters store the information on the number of detected errors

Main advantage over standard SRAM-based particle monitors:

❖ Negligible area and power overhead



7. Conclusion

■ Possible further work

- Validation of simultaneous measurement of direct and pulsed current
- Implementation of a complete rad-hard readout system with commercial components



Thank you for your attention!

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